Texas Instruments

ADSDeSer-50EVM

Evaluation Module

User's Guide

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High-Speed Converter Products

SBAU091

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the specified input and output ranges described in the EVM User's Guide.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60°C. The EVM is designed to operate properly with certain components above 60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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Preface

Read This First

About This Manual

This manual describes the ADSDeSer-50EVM evaluation fixture and how to use it. Throughout this document, the abbreviation EVM and the term *evaluation module* are synonymous with the ADSDeSer-50EVM.

Related Documentation From Texas Instruments

The following documents provide information regarding Texas Instruments integrated circuits used in the assembly of the ADSDeSer-50EVM. These documents are available from the TI web site. The last character of the literature number corresponds to the document revision, which is current at the time of the writing of this User's Guide. To obtain a copy of the following TI documents, visit our website at http://www.ti.com/ or call the Texas Instruments Literature Response Center at (800) 477−8924 or the Product Information Center at (972) 644−5580. When ordering, identify the document by both title and literature number.

Data sheet	**Literature number**
ADS5270/71 Data Sheet	SBAS293
ADS5275/76 Data Sheet	SBAS300

If You Need Assistance

If you have questions regarding either the use of this evaluation module or the information contained in the accompanying documentation, please contact the Texas Instruments Product Information Center at (972) 644−5580 or visit the TI web site at www.ti.com.

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This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

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Tables

Chapter 1

Overview

The ADSDeSer-50EVM is an evaluation fixture designed for the ADS527x family of data converters. It is an eight-channel LVDS deserializer.

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1.1 Introduction

The ADSDeSer-50EVM is designed to interface to the TI low voltage differential signal (LVDS) output data converters with an operating frequency of up to 50MHz and up to eight simultaneous data channels. The ADSDeSer-50EVM provides an easy way to examine the serialized data output from the serialized LVDS data converters by deserializing the data and converting to a standard parallel data port. Since there is no clock embedded, a synchronous clock output is provided separately, along with the eight channels of data.

The ADSDeSer-50EVM evaluation board will support the analog-to-digital converter (ADC) models listed in Table 1−1.

Table 1−1. A/D Converter Models Supported by the ADSDeSer-50EVM

Model	Features	LVDS Channel Data Rate
ADS5270	12-bit, 40MSPS, 8-Channel	480MBPS
ADS5271	12-bit, 50MSPS, 8-Channel	600MBPS
ADS5275	10-bit, 40MSPS, 8-Channel	480MBPS
ADS5276	10-bit, 50MSPS, 8-Channel	600MBPS

1.2 Features

- ❑ Deserialize up to eight simultaneous channels of 10- and 12-bit data.
- ❑ Operates with LVDS output data converters up to 50MSPS.
- ❑ Clock signal is synchronous with data output.

1.3 Power Supply

The ADSDeSer-50EVM requires two supplies for operation: a +3.3V supply for the main board power, and a +1.8V to +3.3V supply for the output driver supply. An onboard regulator supplies +1.5V to power the FPGA.

1.4 Indicators

There are two LEDs on the board. DS1 is used to show the board has power applied. DS2 is used to indicate when the PROM has finished downloading the stored program to the FPGA.

Chapter 2

Board Configuration

This chapter describes the inputs, controls, and circuit design of the ADSDeSer-50EVM in detail.

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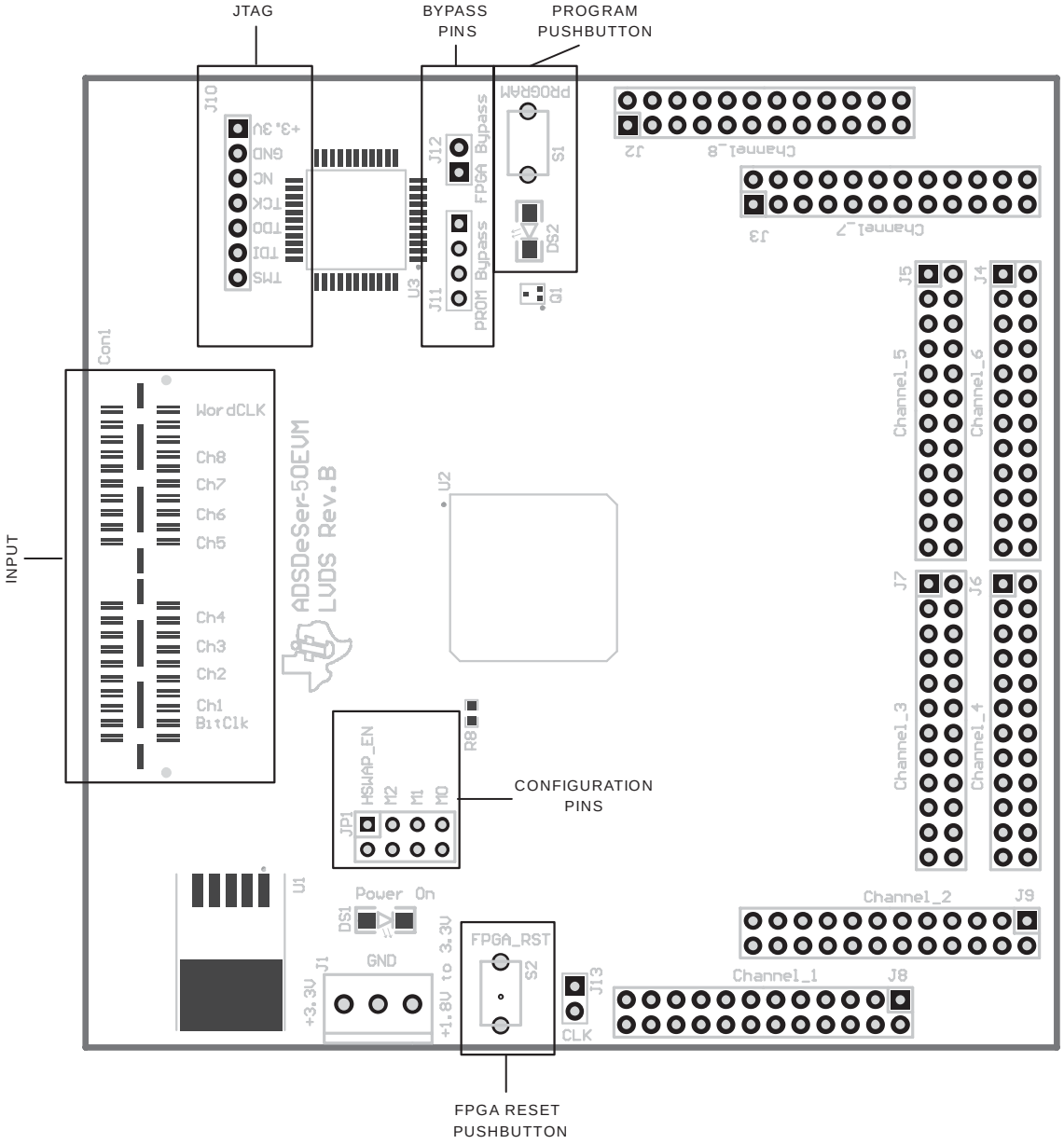
2.1 I/O Connectors

The positions and functions of the ADSDeSer-50EVM connectors are discussed in the following sections.

Figure 2−1. ADSDeSer-50EVM Overview



2.1.1 Input

The input connector (Con1) is used to connect one of the ADS527xEVM LVDS output converter boards to the DeSer-50EVM.

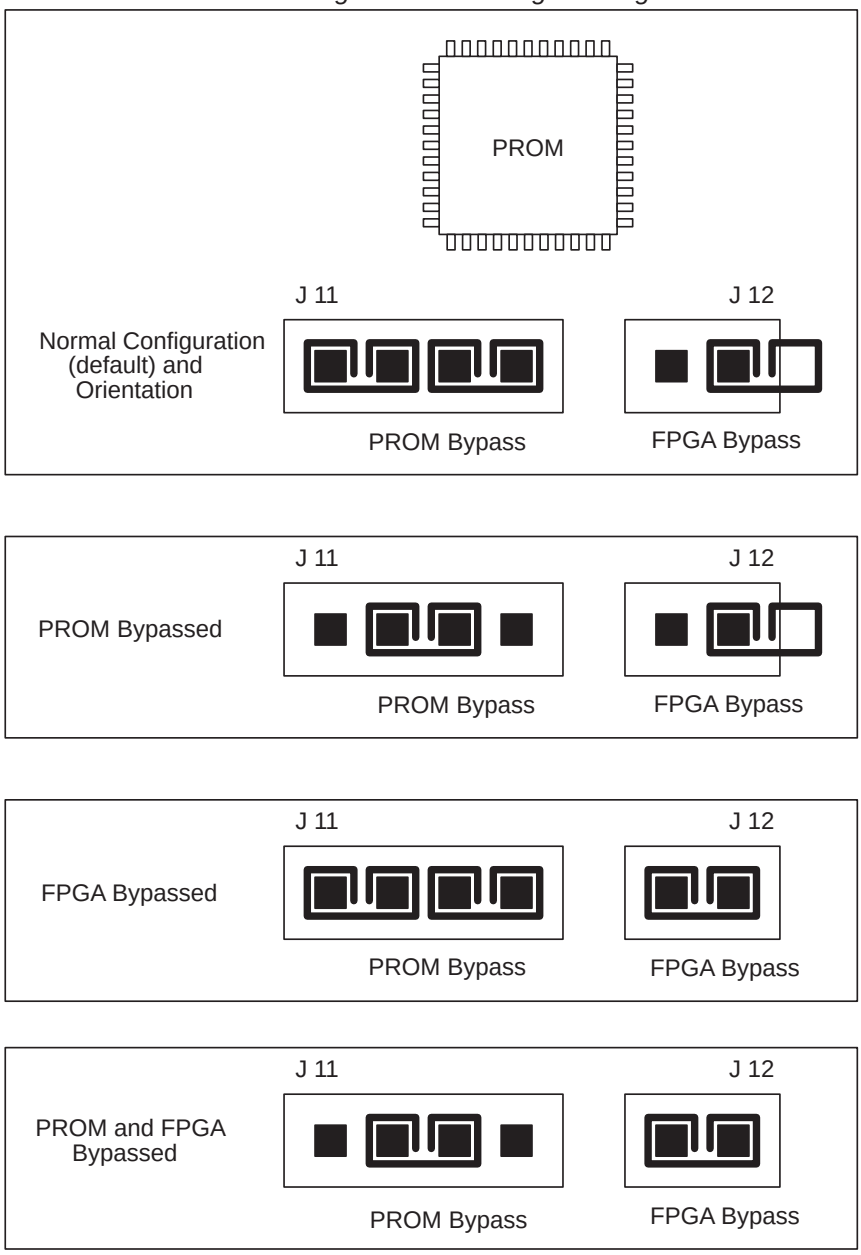
2.1.2 JTAG

J10 is the JTAG port. This connection is used to program the onboard PROM and access the FPGA directly by using J11 and J12.

2.1.3 FPGA and PROM Bypass and Configuration

J11 and J12 can be used to bypass the PROM and/or bypass the FPGA when programming. The following diagram shows the default and different configurations for programming.

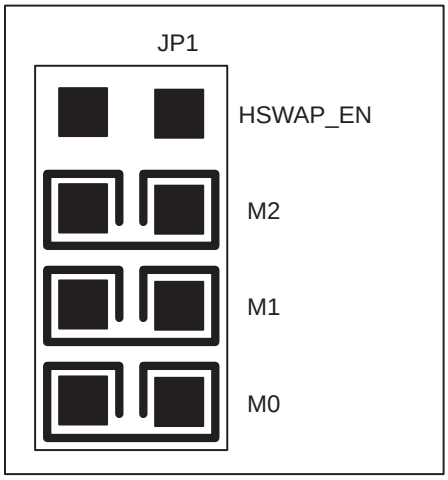
Figure 2−2. Default and Alternate Configurations for Programming the ADSDeSer-50EVM



2.1.4 FPGA Configuration Pins

JP1 is used to program the FPGA. The following diagram shows the default configuration. Further information on the different modes is available in the Xilinx Virtex II Handbook.

Figure 2−3. Default Configurations for FPGA Pins on the ADSDeSer-50EVM



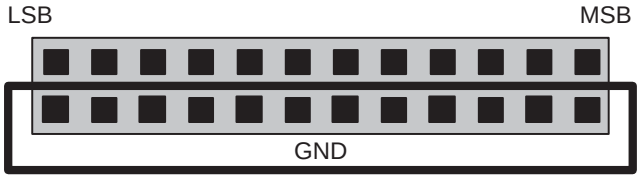
2.1.5 Pushbuttons

The ADSDeSer-50EVM has two pushbuttons. **S1** (PROGRAM) is used to download from the PROM to the FPGA. When the program is finished downloading, indicator DS2 will turn on. **S2** (FPGA_RST) is used to reset the downloaded program in the FPGA.

2.1.6 Output Connectors

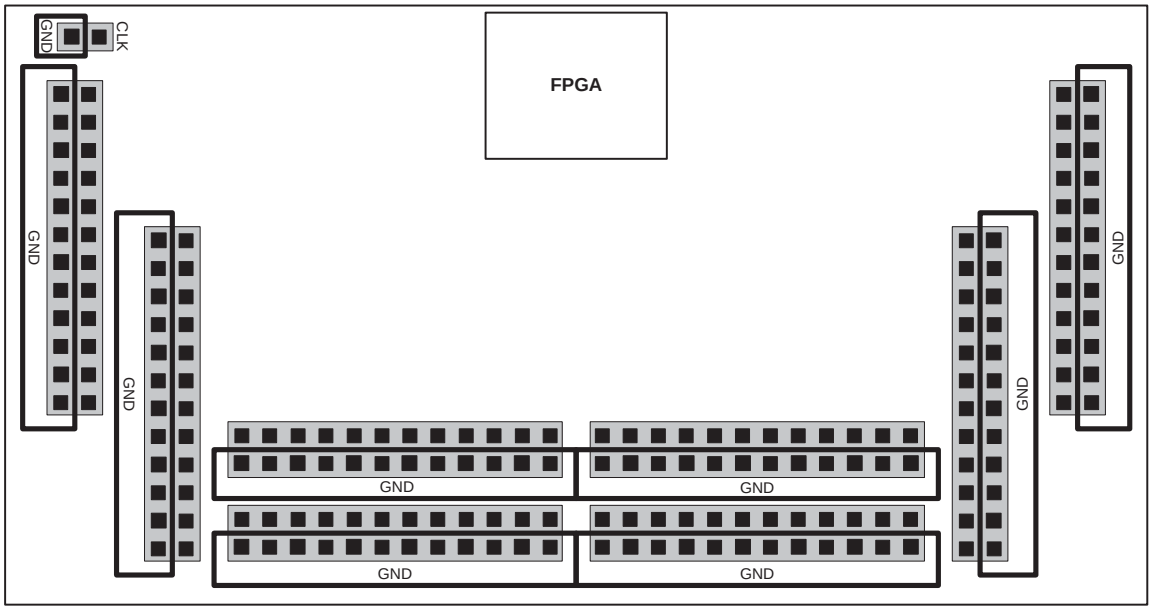
The outputs from the FPGA are not labeled for LSB and MSB. This is because of the capability of the ADS527x data converters to switch between *MSB first* or *LSB first* for the output data. This configuration is accessed in the internal registers of the ADS527x through a serial interface. Refer to the respective ADS527x datasheet and the ADS527xEVM for more details. If the standard configuration for the data converter is used, then the following diagram can be used for capturing the data.

Figure 2−4. Output Connectors for the ADSDeSer-50EVM



The next diagram shows the orientation of the ground connections with respect to the board layout.

Figure 2−5. Orientation of Ground Connections for the ADSDeSer-50EVM



2.2 Start-up Sequence

The startup sequence for the ADSDeSer-50EVM is as follows:

Step 1: Connect the ADC board to the input connector (Con1).

Step 2: Connect the clock and data outputs to a data capture system (analyzer).

Step 3: Apply power to the ADSDeSer-50EVM board and look for the Power On (DS1) LED and DS2 LED to illuminate. If DS2 does not illuminate, press the Program (S1) pushbutton. If no LEDs illuminate, contact TI customer support for help.

Step 4: Read data from ADSDeSer-50EVM.

If during operation a condition occurs that is unexplainable, press FPGA_RST (S2) to restart the FPGA program. If the condition still persists, contact TI customer support for further assistance.

Chapter 3

Schematic and Layout

This chapter contains the complete printed circuit board (PCB) layout, schematic diagram, and bill of materials for the ADSDeSer-50EVM.

Note:

Board layouts are not to scale. These are intended to show how the board is laid out; they are not intended to be used for manufacturing ADSSer-50EVM PCBs.

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3.1 Board Layout

Figure 3−1. ADSDeSer-50EVM—Layer 1 (Top)

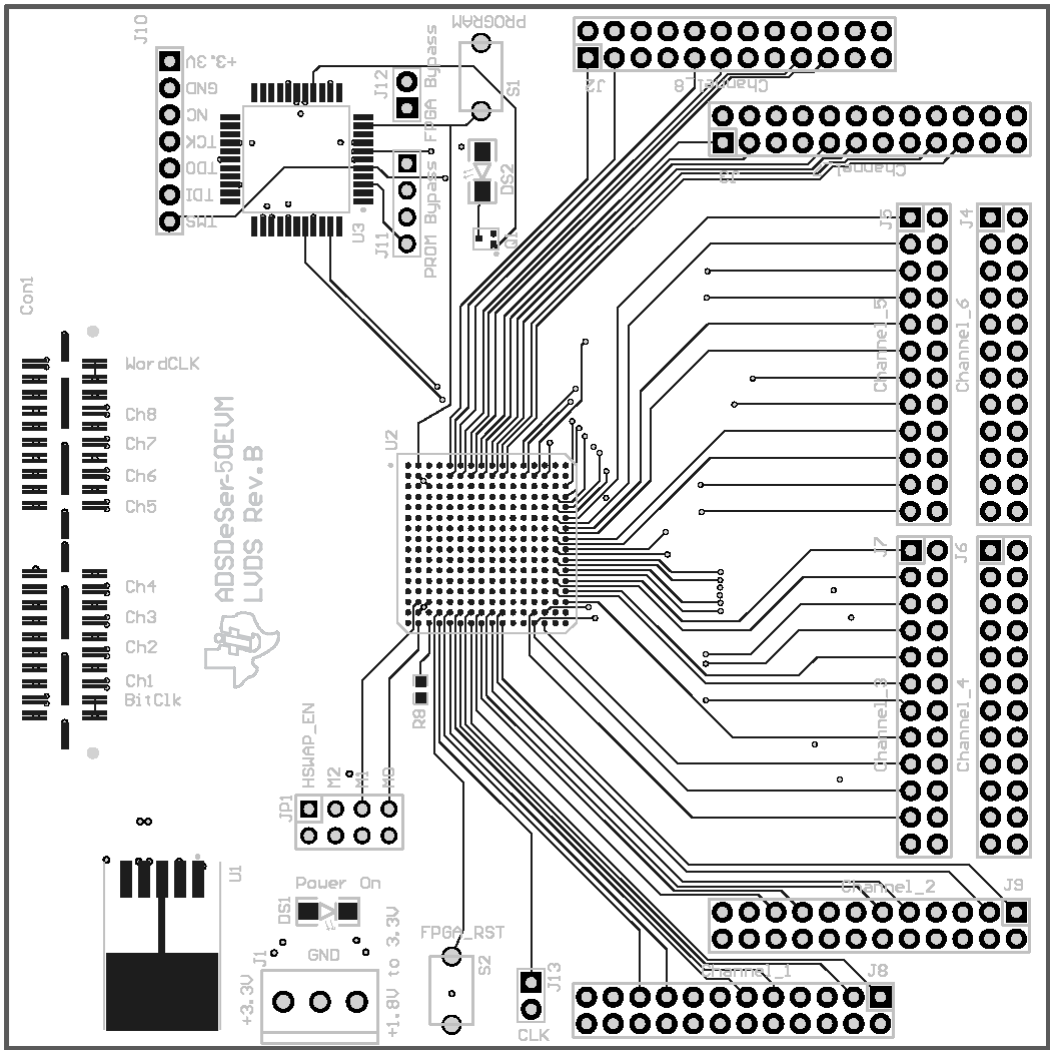


Figure 3−2. ADSDeSer-50EVM—Layer 2 (Power)

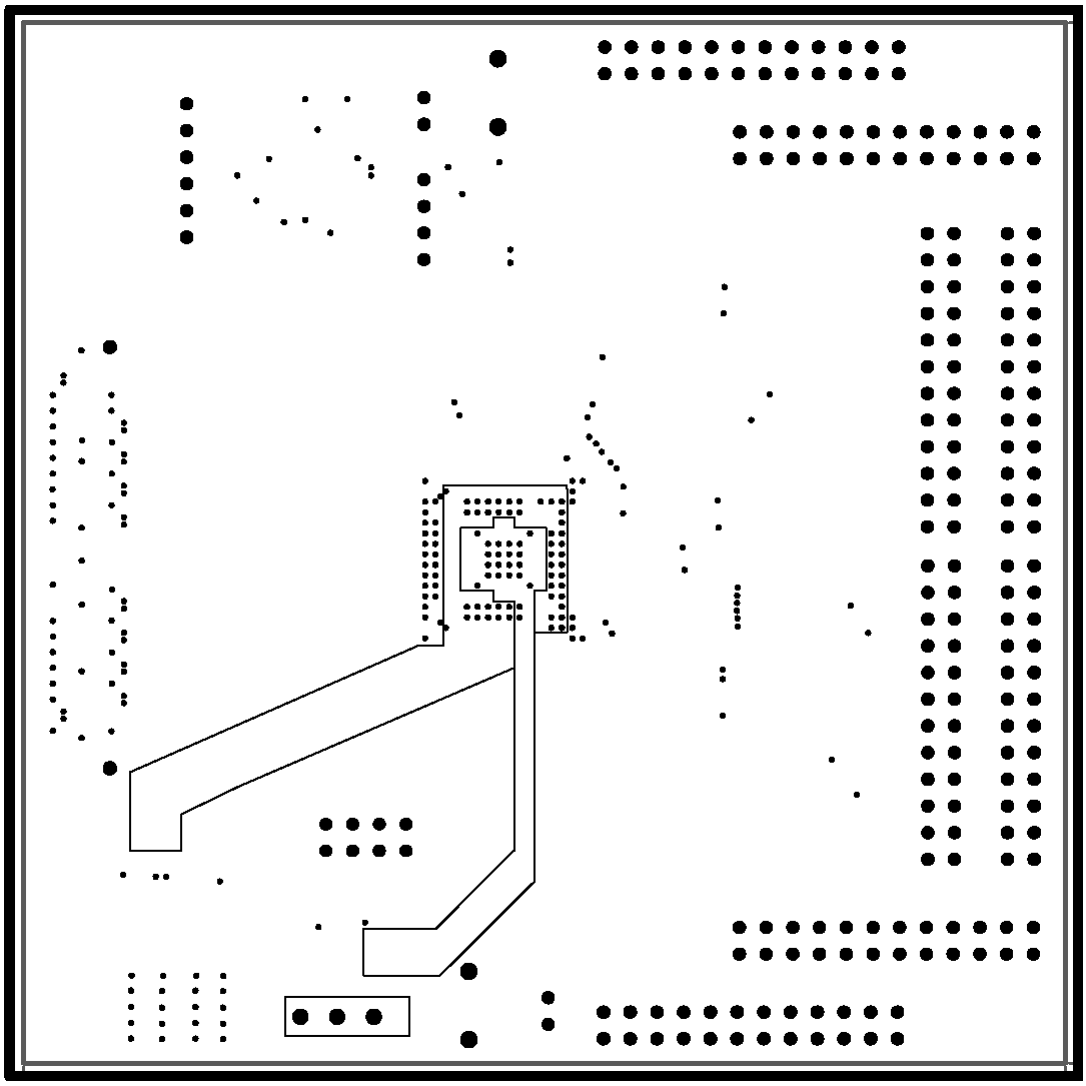


Figure 3−3. ADSDeSer-50EVM—Layer 3 (Mid Signal)

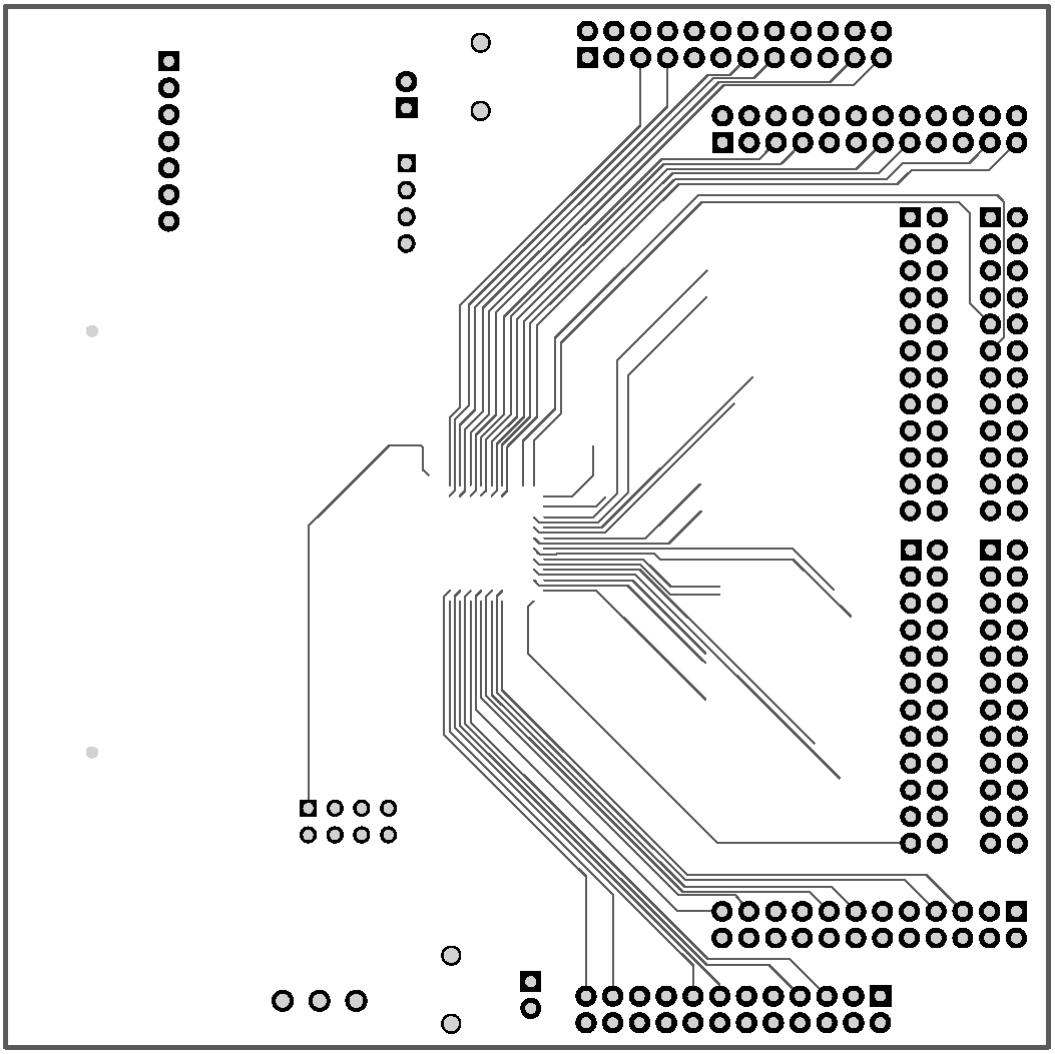


Figure 3−4. ADSDeSer-50EVM—Layer 4 (Ground)

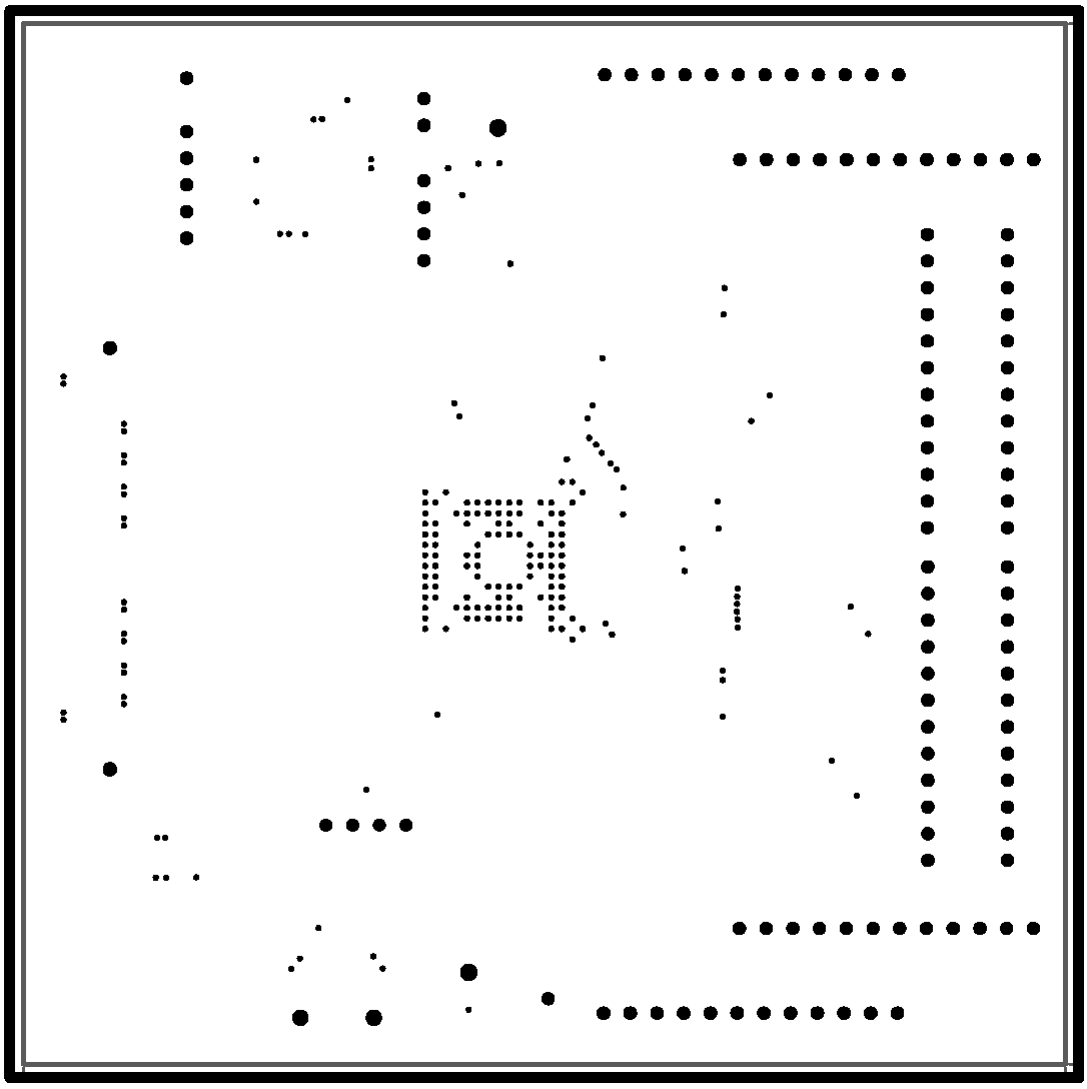
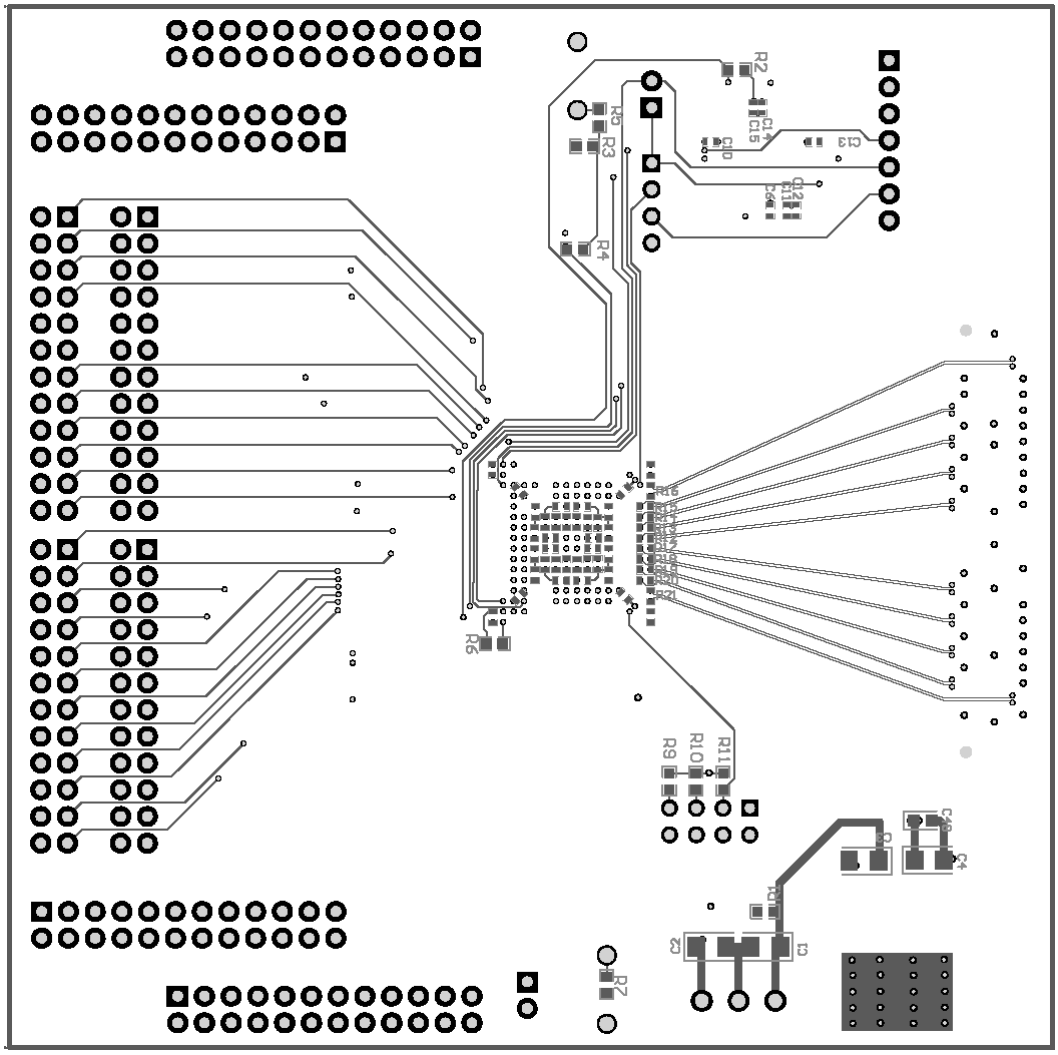
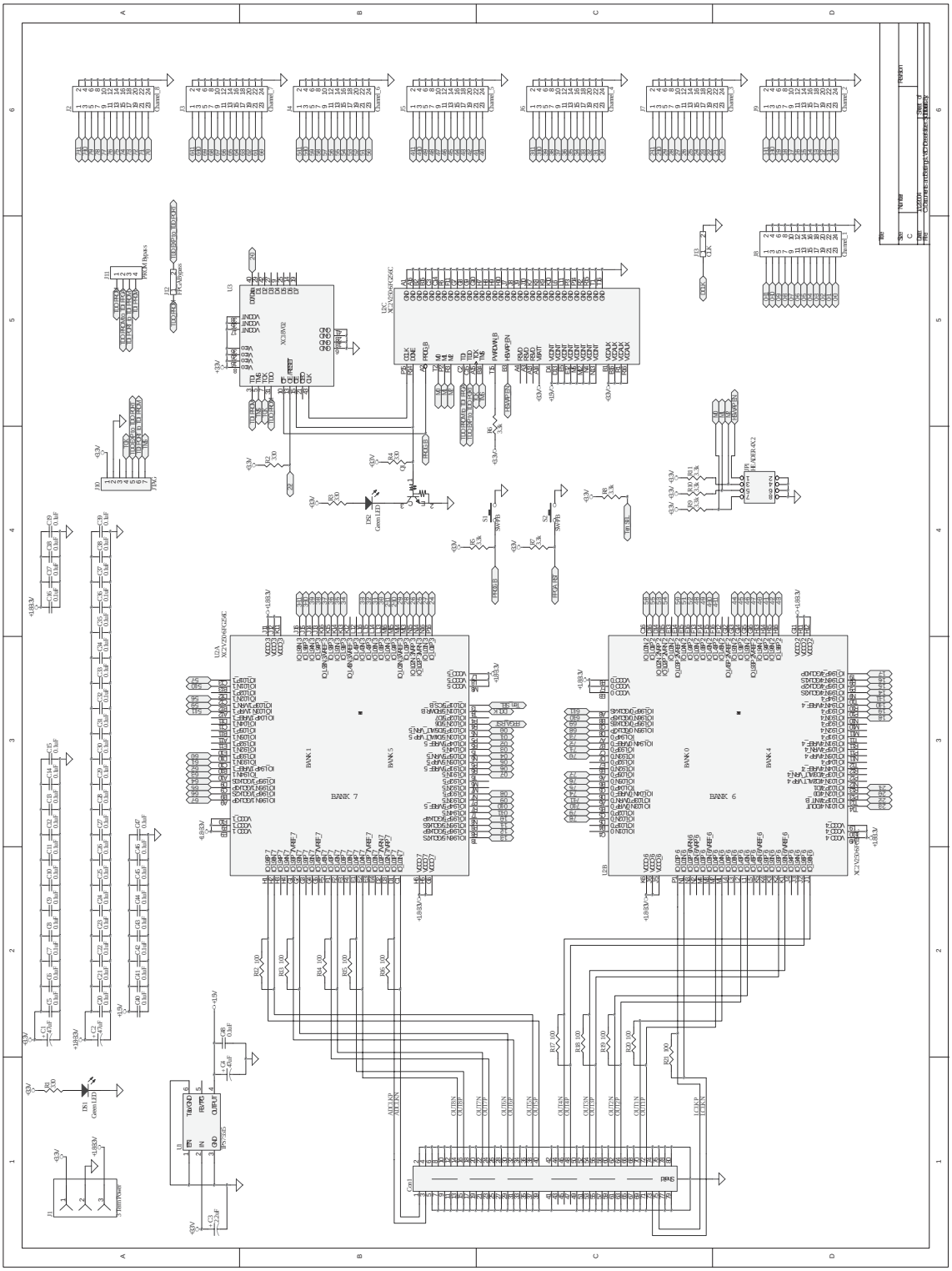


Figure 3−5. ADSDeSer-50EVM—Layer 5 (Bottom)



3.2 Schematic

Figure 3−6. ADSDeSer-50EVM—Schematic



3.3 Bill of Materials

Table 3−1. Bill of Materials

Quantity	Comment	Description	Reference Designator
1		Samtec QSH 040−01−L−D−DP−A	Con1
43	0.1µF	Multilayer Ceramic—0402 size	C5, C6, C7, C8, C9, C10, C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, C32, C33, C34, C35, C36, C37, C38, C39, C40, C41, C42, C43, C44, C45, C46, C47
1	0.1µF	Multilayer Ceramic—0603 size	C48
1	2.2µF	Tantalum Capacitor 1206 size	C3
1	3 Term Power	3 Terminal Screw Connector	J1
8	3.3kΩ	0603 Chip Resistor	R5, R6, R7, R8, R9, R10, R11
10	100Ω	0402 Chip Resistor	R12, R13, R14, R15, R16, R17, R18, R19, R20, R21
3	47µF	AVX TAJA476K004R 3216 size Tantalum Capacitor	C1, C2, C4
3	330Ω	0603 Chip Resistor	R1, R2, R3, R4
1	CLK	0.1” Terminal strip—Square	J13
1	DTC114EET1	On Semiconductor Bias Resistor Transistor NPN	Q1
1	FPGA Bypass	0.1” Terminal strip—Square	J12
2	Green LED	Panasonic 1206 size Green LED Part No.: LNJ311G83RA	DS1, DS2
1	Header 4x2	0.1” Terminal strip—Square	JP1
1	JTAG	0.1” Terminal strip—Square RIGHT ANGLE	J10
1	PROM Bypass	0.1” Terminal strip—Square	J11
2	SW-PB	Push Button Switch Part No.: EVQ−PJB04K	S1, S2
1	TPS75515KTT	TI LDO Regulator	U1
8	Header 12x2	0.1” Terminal strip—Square	J2, J3, J4, J5, J6, J7, J8, J9
1	XC2V250-6FG256C	Xilnix Virtex−II 1.5V FPGA	U2
1	XC18V02VQ44C	Xilinx PROM	U3
5	1-382811-6	AMP 2-position shunt	