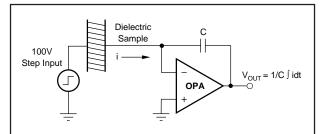
## DIODE-CONNECTED FET PROTECTS OP AMPS

Providing input-overload protection for sensitive measurement circuits proves difficult when you must not degrade the circuits' performance in the process. It's an especially tricky problem when you're measuring a material's dielectric properties. In such an application (see Figure 1), an ultra-low input bias current op amp serves as a current integrator to measure a dielectric's response to a 100V step.



STANDARD DIELECTRIC-EVALUATION SCHEMES can prove disastrous to the op amp they employ. If the dielectric under test shorts, the resulting high voltage at the op amp's input destroys the device unless the device's very-low-bias (low voltage) input stage is somehow protected. The solution is difficult: Whatever you do, it must not degrade the op amp's performance.

FIGURE 1. Dielectric Evaluation Circuit.

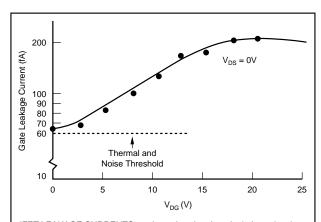
Unfortunately, the op amp is destroyed if the dielectric sample shorts.

For one such measurement setup, low-bias current op amps like the OPA111, OPA121, OPA128, OPA124 or OPA129 can serve because their bias current is in the pA or even fA range and therefore contributes negligible measurement error. What type of protective device doesn't degrade this op amp's parameters? PN-junction devices usually have leakage currents in the nanoamp range even at very-low bias voltages—a degradation of several orders of magnitude. FETs are generally much better in this respect, and Siliconix's 2N4117A JFET proves the best.

Figure 2 shows an experimentally derived curve of leakage current vs voltage for this device. Note that for voltages comparable to those between an op amp's inputs, the 2N4117A's leakage is compatible with the op amp's bias. (The residual 60fA level at 0V arises from thermal effects and measurement-system noise.)

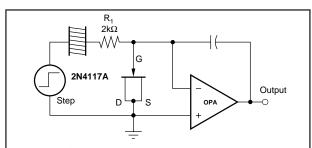
The overload-protected design resulting from these FET measurements is shown in Figure 3. The diode-connected JFET serves as a shunt across the op amp's input—a scheme

that limits the differential input to 0.6V if the dielectric shorts. Resistor  $R_{\rm l}$  limits the maximum short-circuit current to the 50mA level specified in the FET's data sheet.  $R_{\rm l}$ 's effect on measurement accuracy is negligible because the dielectric's impedance is very much greater than the resistor's  $2k\Omega$  value.



JFET LEAKAGE CURRENTS can be so low that they don't degrade a low-input bias op amp's parameters. Measurements show that Siliconix's 2N4117A can serve as a voltage limiter when it's diode-connected. The actual leakage is probably somewhat lower than measured, but thermal effects and noise place a limiting threshold on the measurement.

FIGURE 2. Curve of Leakage Current vs Voltage.



OVERVOLTAGE PROTECTION results when you incorporate a diodeconnected JFET in the measuring circuit. If the dielectric shorts during testing, the FET clamps at 0.6V saving the sensitive op amp from destruction. R,'s resistance—although high enough to protect the FET against overcurrent failure—is still so small relative to the dielectric's impedance that it doesn't impair measurement accuracy.

FIGURE 3. Overvoltage Protection Circuit.

Reprinted from EDN, October 5, 1980; ©1980, Cahners Publishing Company.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

©1994 Burr-Brown Corporation AB-064 Printed in U.S.A. January, 1994

## **IMPORTANT NOTICE**

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Copyright © 2000, Texas Instruments Incorporated