TEXAS INSTRUMENTS

User's Guide
SBVU013–January 2009

TPS71401DRVEVM-426

This user's guide describes the characteristics, operation, and use of the TPS71401DRVEVM-426 evaluation module. This document includes setup instructions, a schematic diagram, thermal guidelines, a bill of materials (BOM), and printed circuit board (PCB) layout drawings.

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1 Overview

This document describes the characteristics, operation, and use of the TPS71401DRVEVM-426 evaluation module (EVM). This EVM demonstrates the capabilities and features of Texas Instruments' TPS71401, a low-dropout (LDO) linear regulator, an 80-mA, low quiescent current linear regulator in a 2-mm x 2-mm SON package. The TPS71401DRVEVM-426 EVM helps designers evaluate the operation and performance of the TPS71401 LDO in a variety of configurations.

1.1 Related Documentation from Texas Instruments

The following related documents are available through the Texas Instruments web site at http://www.ti.com.

Table 1. Related Documentation

Part Number	Literature Number
TPS71401	SBVS116

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS71401EVM.

2.1 Electrostatic Discharge Notice

CAUTION

Many of the components on the TPS71401EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

Failure to observe proper ESD handling procedures may result in damage to EVM components.

2.2 Input/Output Connector Descriptions

2.2.1 J1: VIN

This connector is the positive input supply voltage. The leads to the input supply should be twisted and kept as short as possible to minimize electromagnetic interference (EMI) transmission. Additional bulk capacitance should be added between J1 and J2 if the supply leads are longer than 6 in (15,24 cm). An additional 47uF or greater capacitor improves the transient response of the TPS71401 and helps to reduce ringing on the input when long supply wires are used.

2.2.2 J2: VOUT

This point is the positive connection from the output. Connect this pin to the positive input of the load.

2.2.3 J3: GND

This is the return connection for the input power supply of the regulator.

2.2.4 J4: GND

This point is the return connection for the output.

2.2.5 J5: Output Voltage Selection

This jumper is used to select the output voltage of the TPS71401. The jumper selects different feedback resistors to change the output voltage setting. The output voltage is set by inserting a shorting jumper across two pins of J5. The preprogrammed output voltages are configured as shown in Table 2.

Table 2. Output Voltage Setting

Output Voltage (V)	Jumper Between Pins
5.0	1 and 2
3.3	3 and 4
2.7	5 and 6
2.5	7 and 8

Other output voltages can be configured by changing the feedback resistors on the board. The feedback network is high impedance and sensitive to noise or resistance value changes. The pins of J5 should not be touched while the device is powered on because the impedance of a human is enough to alter the output voltage set point. The output voltage may increase or decrease if J5 is touched, which may damage any load connected to the EVM.

3 Operation

This section discusses the operation of the TPS71401EVM.

3.1 Power On

Connect the positive input power supply to J1. Connect the input power return (ground) to J3. The TPS71401EVM has an absolute maximum input voltage of 11.0 V. The recommended maximum operating voltage is 10 V. The actual highest input voltage may be less than 10 V as a result of thermal conditions. See the Thermal Considerations section of this manual to determine the highest input voltage.

Connect the desired load between J2 (positive lead) and J4 (negative or return lead). Configure jumper J5 for the desired output voltage. The function of J5 is described in the *Setup* section of this manual.

3.2 Fixed Output TPS714xx Device Configuration

The TPS71401 EVM can also be used to evaluate fixed-output voltage versions of the TPS714 LDO. The board layout and device footprints are the same for both the adjustable and the fixed-output voltage versions of the TPS714. To evaluate a fixed-output voltage version, the IC on the board must be changed to the desired fixed output voltage (TPS714xx). Note that R_1 must be removed from the EVM board if a fixed output voltage version is mounted to the EVM board.

4 Thermal Guidelines

This section presents guidelines for the thermal management of the TPS71401DRVEVM-426 PCB.

4.1 Thermal Considerations

Thermal management is a key design component of any power converter application and is especially important when the power dissipation in the LDO is high. To better help users design the TPS71401 family into an application, the following formula should be used to approximate the maximum power dissipation at a particular ambient temperature:

$$T_J = T_A + P_D \times \theta_{JA} \quad (1)$$

Where:

- T_J is the junction temperature
- T_A is the ambient temperature
- P_D is the power dissipation in the IC
- θ_{JA} is the thermal resistance from junction to ambient

All temperatures are in degrees Celsius.

The thermal resistance from junction to ambient for the TPS71401EVM has a typical value of 65°C/W. The recommended maximum operating junction temperature specified in the data sheet for the TPS71401 family is +125°C. With these two pieces of information, the maximum power dissipation can be found by using Equation 1.

Example 1. Maximum Power Dissipation Calculation

What is the maximum input voltage that can be applied to a TPS71401 with the output voltage configured to 3.3 V if the ambient temperature is +85°C and the full 80 mA of load current is required?

Given:

T_J = +125°C, T_A = +85°C, θ_{JA} = 65°C/W

Using Equation 1, we substitute in the given values above and find that the maximum power dissipation for the part is P_D = 0.615 W.

$$+125°C = +85°C + P_D(65°C/W) \quad (2)$$

This result means that the total power dissipation of the TPS71401 must be less than 0.615 W. Now the input voltage can be calculated:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} = (V_{IN} - 3.3\ V) \times 0.08\ A = 0.615\ W \quad (3)$$

Therefore, the maximum input voltage should be 10.98 V or less in order to maintain a safe junction temperature. However, the recommended maximum input voltage is 10.0 V, so the device can be used over the entire recommended input voltage range.

Similar analyses can be performed to determine the maximum ambient temperature allowed and still provide the full output current while maintaining the junction temperature at or below +125°C. The maximum ambient temperature depends on the output voltage. Table 3 lists the maximum ambient temperature allowed for the pre-programmed output voltages.

Table 3. Output Voltage and Maximum Ambient Temperature

Output Voltage (V)	Maximum Ambient Temperature (°C)
5.0	99
3.3	90
2.7	87
2.5	86

5 Board Layout, Schematic, and Parts List

This section provides the TPS71401DRVEVM-426 board layout and illustrations. It also includes the schematic and bill of materials for the EVM.

5.1 PCB Layouts

Figure 1 through Figure 3 show the layout for the TPS71401DRVEVM-426 PCB.

Note: Board layouts are not to scale. These figures are intended to show how the board is laid out; they are not intended to be used for manufacturing TPS71401DRVEVM-426 PCBs.

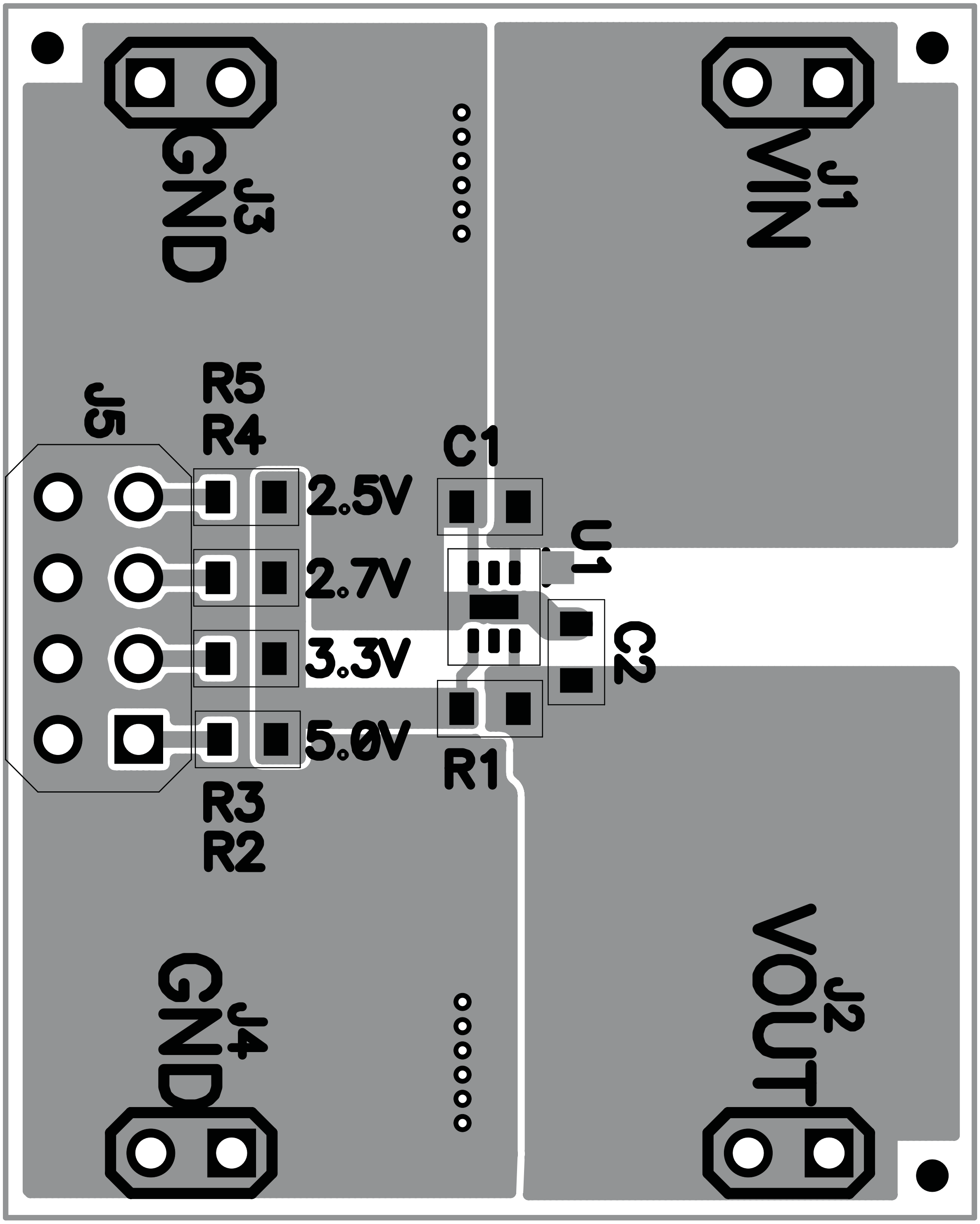

Figure 1. Assembly Layer

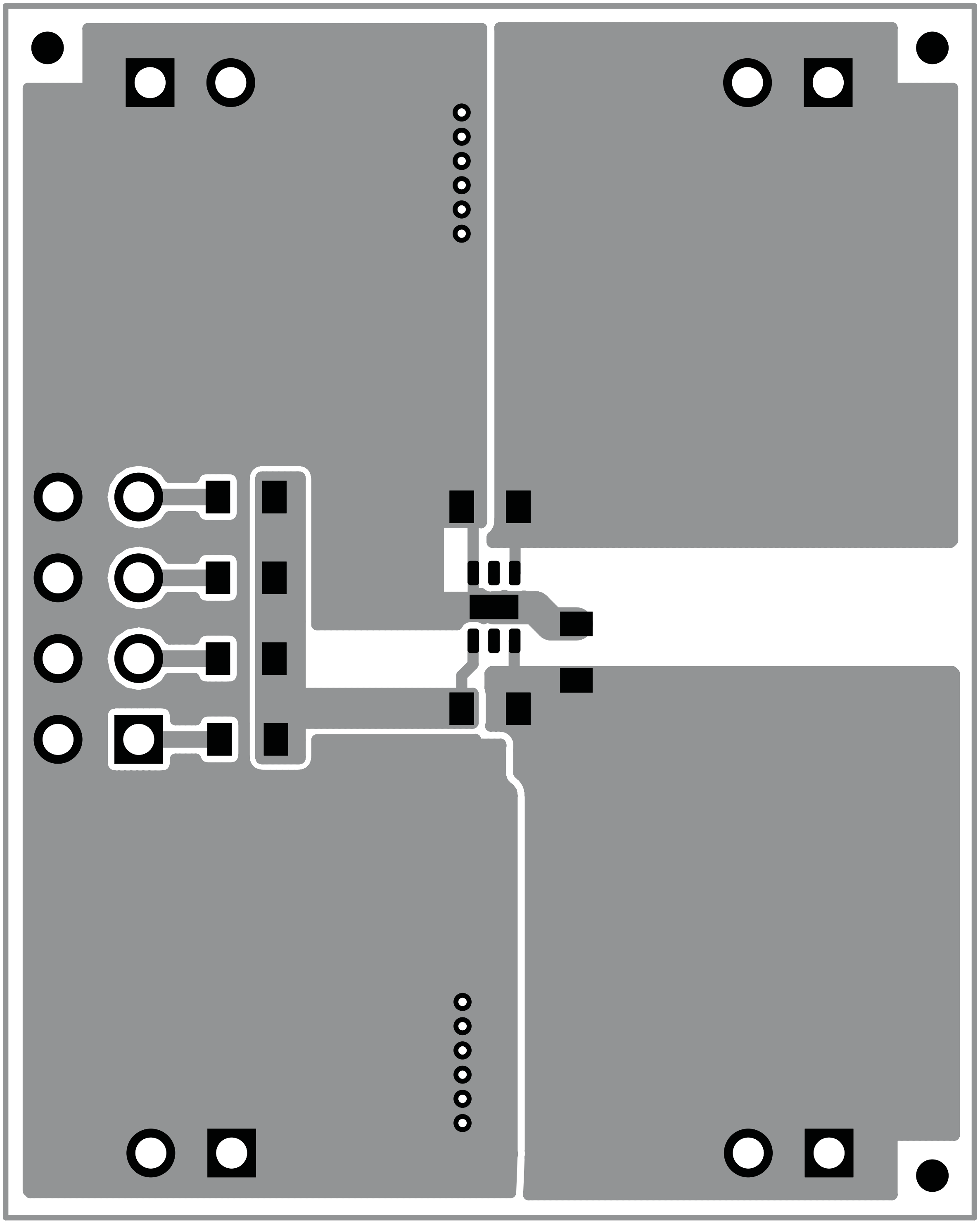

Figure 2. Top Layer Routing

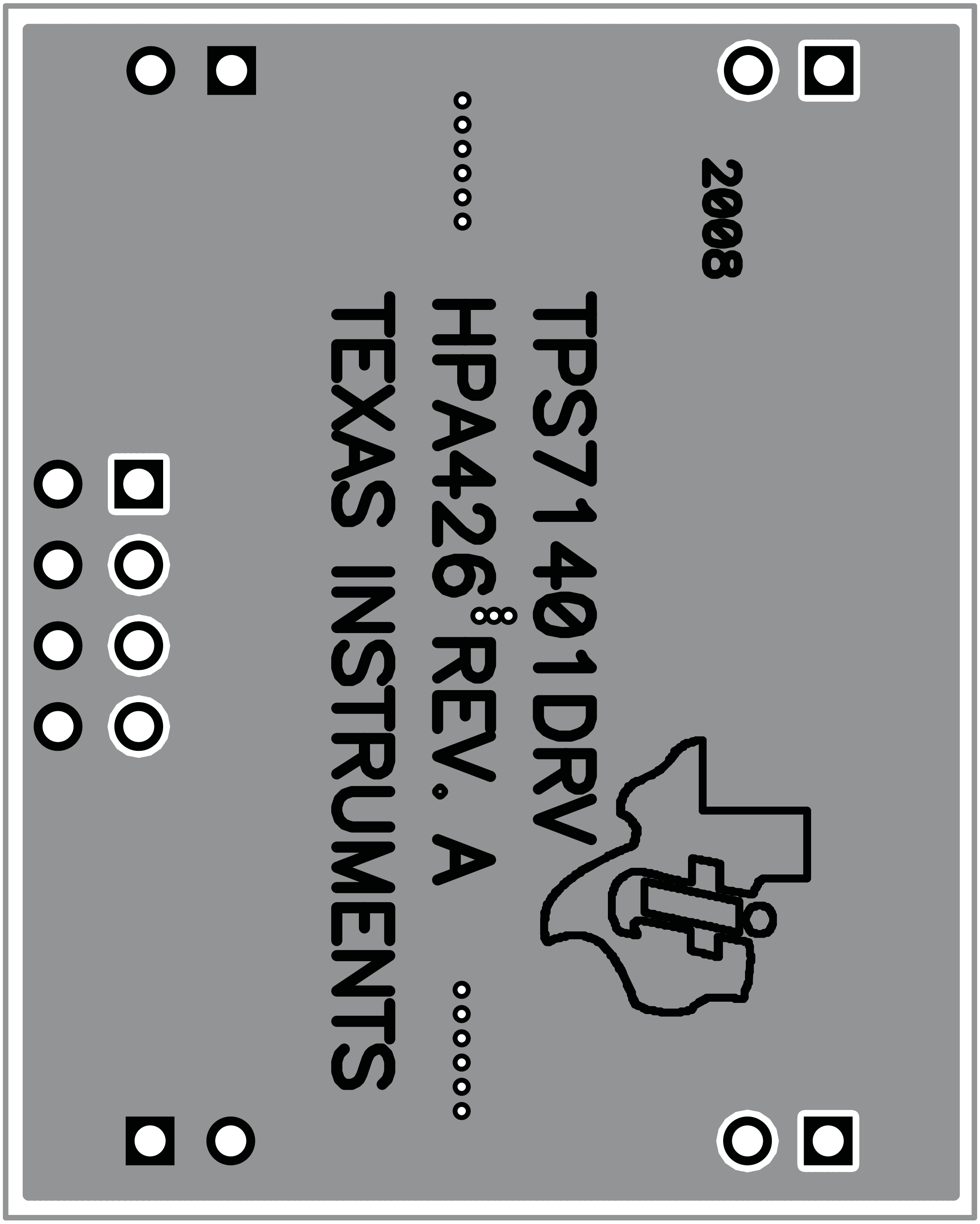

Figure 3. Bottom Layer Assembly

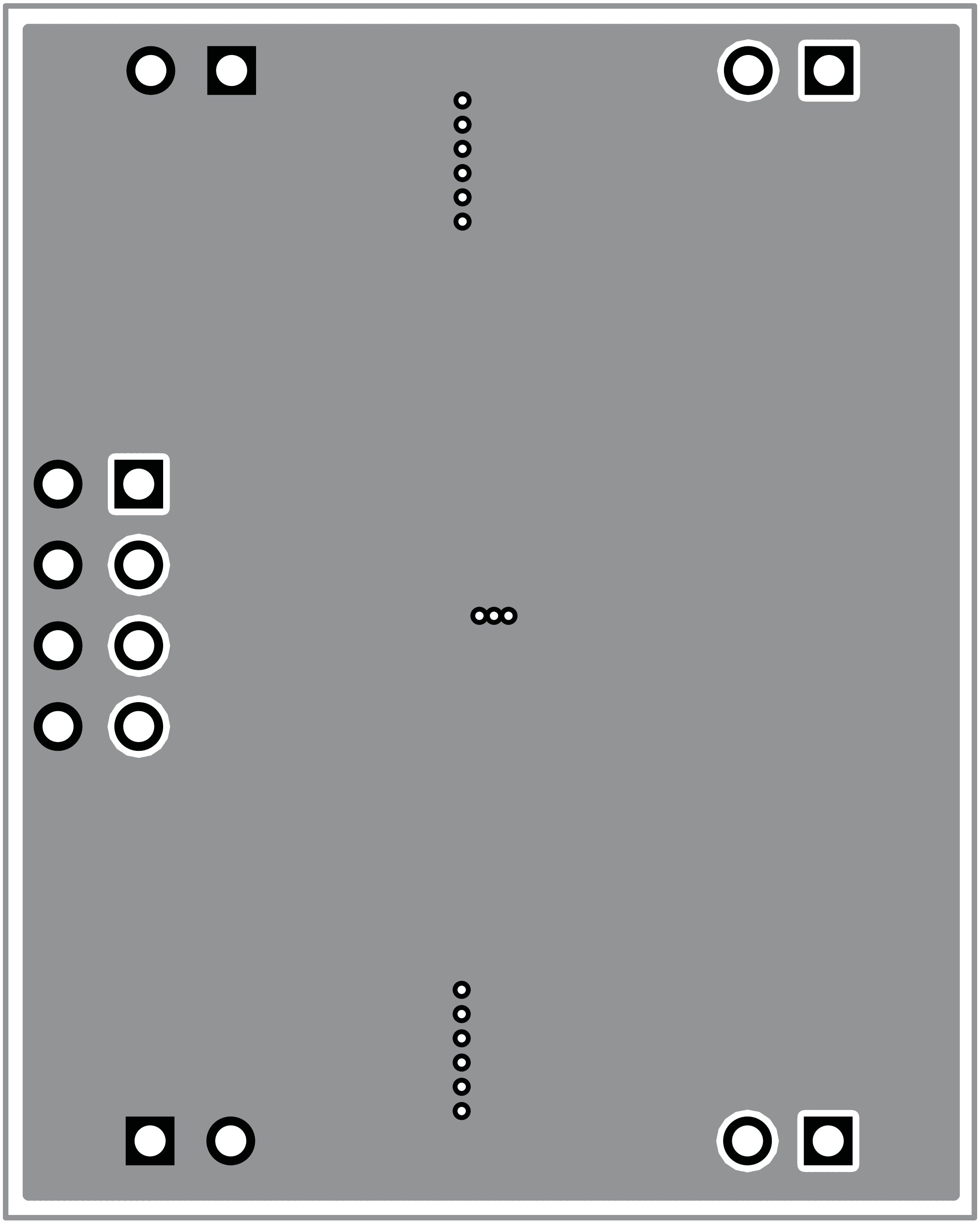

Figure 4. Bottom Layer Routing

5.2 Schematic and BOM

Figure 5 illustrates the TPS71401DRVEVM-426 schematic. Table 4 lists the bill of materials for this EVM.

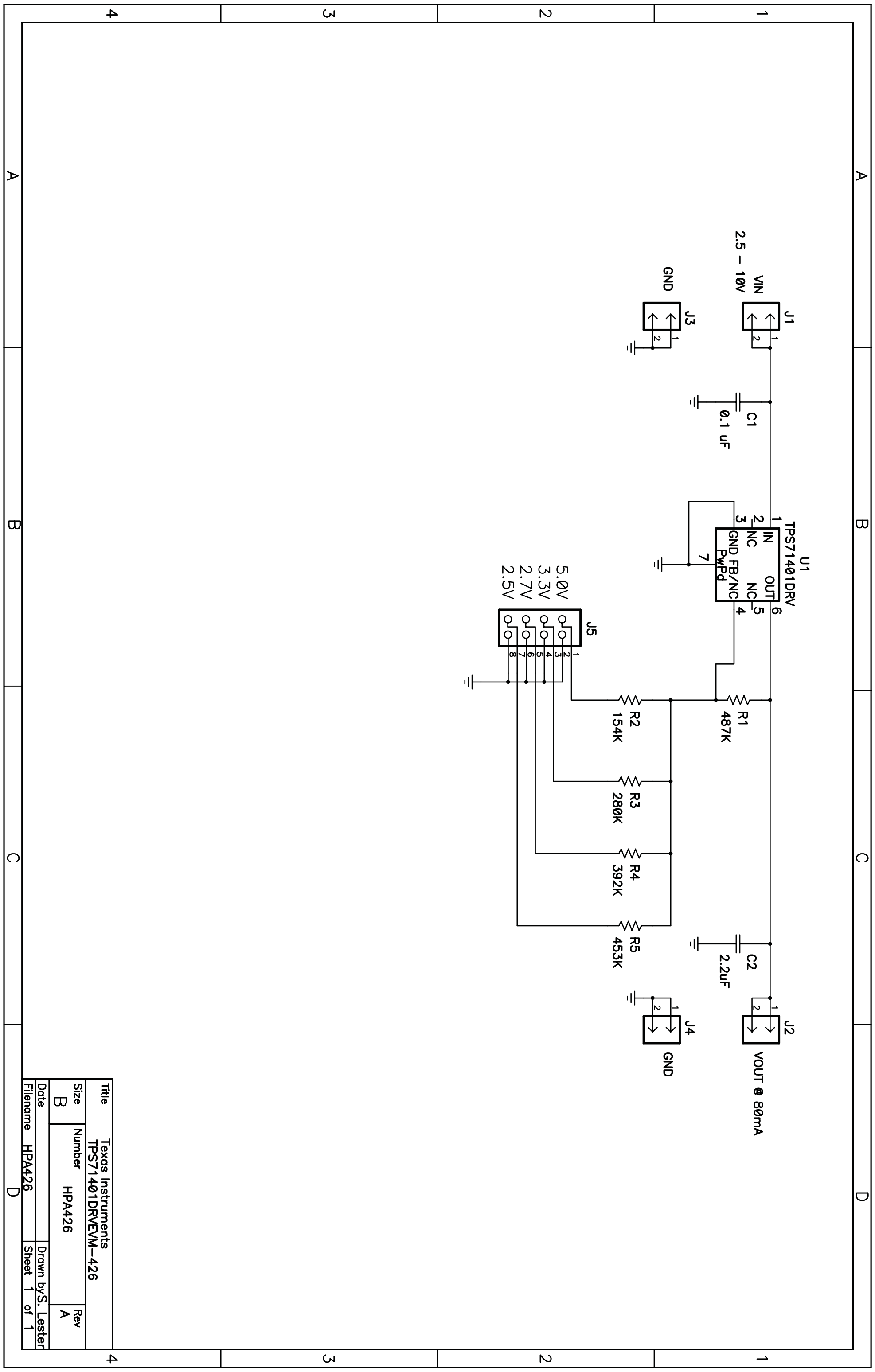

Figure 5. TPS71401DRVEVM-426 Schematic

Table 4. TPS71401DRVEVM-426 Bill of Materials[1][2][3]

Count	RefDes[4]	Value	Description	Size	Part Number	Mfr
1	C1	0.1 µF	Capacitor, Ceramic, 0.1-µF, 16-V, X7R, 10%	603	STD	Any
1	C2	2.2 µF	Capacitor, Ceramic, 2.2-µF, 10-V, X7R, 10%	603	STD	Any
4	J1, J2, J3, J4	PTC36SAAN	Header, Two-pin, 100-mil spacing	0.100 x 2	PTC36SAAN	Sullins
1	J5	PTC36DAAN	Header, Male 2x4-pin, 100-mil spacing	0.20 x 0.40 in	PTC36DAAN	Sullins
1	N/A	N/A	PCB, 1.5 In x 1.2 In x 0.062 In	—	HPA425	Any
1	R1	487 k	Resistor, Chip, 1.00MΩ, 1/16-W, 1%	603	STD	Any
1	R2	154 k	Resistor, Chip, 1/16W, 5%	603	STD	Any
1	R3	280 k	Resistor, Chip, 1/16W, 5%	603	STD	Any
1	R4	392 k	Resistor, Chip, 1/16W, 5%	603	STD	Any
1	R5	453 k	Resistor, Chip, 1/16W, 5%	603	STD	Any
1	U1	TPS71401DRV	IC, 80-mA, 10-V Quiescent Current 3.2-µA LDO Linear Regulator	2mm x 2mm	TPS71401DRV	TI
1	—	—	100-mm Two-Pin Shunt	0.100 x 2	929957-08	3M

(1) These assemblies are ESD sensitive. ESD precautions shall be observed.
(2) These assemblies must be clean and free from flux and all contaminants. Use of no-clean flux is not acceptable.
(3) These assemblies must comply with workmanship standards IPC-A-610 Class 2.
(4) Components can be substituted with equivalent manufacturer components.

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 2.5 V to 10 V and the output voltage range of 1.2 V to 8.8 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than +85°C. The EVM is designed to operate properly with certain components above +85°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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