Contents of MSP430F241x, MSP430F261x Code Examples (slac151.zip) - asm (CCS), .s43 (IAR), and .c (CCS & IAR)

Link to zip file: http://www.ti.com/lit/zip/slac0151

Applicable Devices: MSP430F2416, MSP430F2417, MSP430F2418, MSP430F2419, MSP430F2616, MSP430F2617, MSP430F2618, MSP430F2619

Consult readme.txt included in the zip file for disclaimer and coding style guidelines

Contents:

.asm code examples – CCS	
File name	**Description**
msp430x261x_1.asm	Software Toggle P1.0
msp430x261x_1_vlo.asm	Software Toggle P1.0, MCLK = VLO/8
msp430x261x_adc12_01.asm	ADC12, Sample A0, Set P1.0 if A0 > 0.5*AVcc
msp430x261x_adc12_02.asm	ADC12, Using the Internal Reference
msp430x261x_adc12_03.asm	ADC12, Sample A10 Temp, Set P1.0 if Temp ++ ~2C
msp430x261x_adc12_04.asm	ADC12, Extend Sampling Period with SHT Bits
msp430x261x_adc12_05.asm	ADC12, Using an External Reference
msp430x261x_adc12_06.asm	ADC12, Repeated Sequence of Conversions
msp430x261x_adc12_07.asm	ADC12, Repeated Single Channel Conversions
msp430x261x_adc12_08.asm	ADC12, Using 10 External Channels for Conversion
msp430x261x_adc12_09.asm	ADC12, Sequence of Conversions (non-repeated)
msp430x261x_adc12_10.asm	ADC12, Sample A10 Temp and Convert to oC and oF
msp430x261x_clks.asm	Basic Clock, Output Buffered SMCLK, ACLK, and MCLK
msp430x261x_compA_01.asm	Comparator A, Poll input CA0, result in P1.0
msp430x261x_compA_02.asm	Comparator A, Poll input CA0, CA exchange, result in P1.0
msp430x261x_compA_04.asm	Comparator A, Poll input CA0, result in P1.0
msp430x261x_compA_05.asm	Comparator A, Input to CA0, Interrupt triggered
msp430x261x_dac12_01.asm	DAC12_0, Output 1.0V on DAC0
msp430x261x_dac12_02.asm	DAC12_0, Output 2.0V on DAC1
msp430x261x_dac12_03.asm	DAC12_0, Output Voltage Ramp on DAC0
msp430x261x_dc0_flashcal.asm	DCO Calibration Constants Programmer
msp430x261x_dma_01_IAR.asm	from RAM, Software Trigger
msp430x261x_dma_02_IAR.asm	DMA0, Repeated single transfer to P1OUT, TACCR2 Trigger
msp430x261x_dma_03_IAR.asm	DMA0, Repeated single transferUCA1UART 9600, TACCR2, ACLK
msp430x261x_dma_04_IAR.asm	DMA0, single transfer Mode UART1 9600, ACLK
msp430x261x_dma_05_IAR.asm	DMA0, Repeated single transfer to DAC0, Sine Output, TACCR1, DCO
msp430x261x_dma_06_IAR.asm	DMA2, Rpt'd single transfer to DAC1, 8-Bit Sine, TBCCR2, DCO
msp430x261x_dma_07_IAR.asm	DMA0/1, Rpt'd single transfer to DAC12_0/1, Sin/Cos, TACCR1, XT2
msp430x261x_dma_09_IAR.asm	DMA0, ADC12 A10 single blocktransfer Xfer to RAM, TBCCR1, DCO
msp430x261x_dma_10_IAR.asm	DMA0, ADC12 A10 rpt single transfer Xfer to Flash, TBCCR1, DCO
msp430x261x_dma_11_IAR.asm	DMA0/1, ADC12 A10 rpt single transfer Xfer to MPY/RAM, TBCCR1, DCO

msp430x261x_dma_12_IAR.asm	DMA0/1, Block Mode UART1 9600 Auto RX/TX String, ACLK
msp430x261x_flashwrite_01.asm	Flash In-System Programming, Copy SegC to SegD
msp430x261x_flashwrite_03.asm	Flash In-System Programming w/ EEI, Copy SegC to SegD
msp430x261x_flashwrite_04.asm	Flash In-System Programming w/ EEI, Copy SegD to B&C
msp430x261x_fll_01.asm	Basic Clock, Implement Auto RSEL SW FLL
msp430x261x_fll_02.asm	Basic Clock, Implement Cont. SW FLL with Auto RSEL
msp430x261x_hfxt2.asm	Basic Clock, MCLK Configured to Operate from XT2 HF XTAL
msp430x261x_hfxt2_nmi.asm	Basic Clock, MCLK Sourced from HF XTAL XT2, NMI
msp430x261x_lpm3.asm	Basic Clock, LPM3 Using WDT ISR, 32kHz ACLK
msp430x261x_lpm3_vlo.asm	Basic Clock, LPM3 Using WDT ISR, VLO ACLK
msp430x261x_MPY_01.asm	16x16 Unsigned Multiply
msp430x261x_MPY_02.asm	8x8 Unsigned Multiply
msp430x261x_MPY_03.asm	16x16 Signed Multiply
msp430x261x_MPY_04.asm	8x8 Signed Multiply
msp430x261x_MPY_05.asm	16x16 Unsigned Multiply Accumulate
msp430x261x_MPY_06.asm	8x8 Unsigned Multiply Accumulate
msp430x261x_MPY_07.asm	16x16 Signed Multiply Accumulate
msp430x261x_MPY_08.asm	8x8 Signed Multiply Accumulate
msp430x261x_nmi.asm	Configure RST/NMI as NMI
msp430x261x_OF_XT2.asm	XT2 Oscillator Fault Detection
msp430x261x_P1_01.asm	Software Poll P1.3, Set P1.0 if P1.3 = 1
msp430x261x_P1_02.asm	Software Port Interrupt Service on P1.3 from LPM4
msp430x261x_P1_05.asm	Write a byte to Port 1
msp430x261x_P7_05.asm	Write a byte to Port 7
msp430x261x_P8_08.asm	Write a byte to Port 8
msp430x261x_PA_05.asm	Write a word to Port A
msp430x261x_rosc.asm	DCOCLK Biased with External Resistor Rosc
msp430x261x_svs_01.asm	SVS, POR @ 2.5V Vcc
msp430x261x_ta_01.asm	Timer_A, Toggle P1.0, CCR0 Cont. Mode ISR, DCO SMCLK
msp430x261x_ta_02.asm	Timer_A, Toggle P1.0, CCR0 Up Mode ISR, DCO SMCLK
msp430x261x_ta_03.asm	Timer_A, Toggle P1.0, Overflow ISR, DCO SMCLK
msp430x261x_ta_04.asm	Timer_A, Toggle P1.0, Overflow ISR, 32kHz ACLK
msp430x261x_ta_05.asm	Timer_A, Toggle P1.0, CCR0 Up Mode ISR, 32kHz ACLK
msp430x261x_ta_08.asm	Timer_A, Toggle P1.0,P1.2 & P2.0 Cont. Mode ISR, 32kHz ACLK
msp430x261x_ta_11.asm	Timer_A, Toggle P1.1/TA0, Up Mode, 32kHz ACLK
msp430x261x_ta_13.asm	Timer_A, Toggle P1.1/TA0, Up/Down Mode, DCO SMCLK
msp430x261x_ta_14.asm	Timer_A, Toggle P1.1/TA0, Up/Down Mode, 32kHz ACLK
msp430x261x_ta_16.asm	Timer_A, PWM TA1-2 Up Mode, DCO SMCLK
msp430x261x_ta_17.asm	Timer_A, PWM TA1-2, Up Mode, 32kHz ACLK
msp430x261x_ta_19.asm	Timer_A, PWM TA1-2, Up/Down Mode, DCO SMCLK
msp430x261x_ta_20.asm	Timer_A, PWM TA1-2, Up/Down Mode, DCO SMCLK
msp430x261x_tb_01.asm	Timer_B, Toggle P1.0, CCR0 Cont. Mode ISR, DCO SMCLK
msp430x261x_tb_02.asm	Timer_B, Toggle P1.0, CCR0 Up Mode ISR, DCO SMCLK
msp430x261x_tb_03.asm	Timer_B, Toggle P1.0, Overflow ISR, DCO SMCLK
msp430x261x_tb_04.asm	Timer_B, Toggle P1.0, Overflow ISR, 32kHz ACLK

msp430x261x_tb_05.asm	Timer_B, Toggle P1.0, CCR0 Up Mode ISR, 32kHz ACLK
msp430x261x_tb_07.asm	Timer_B, PWM TB1-6, Up Mode, 32kHz ACLK
msp430x261x_uscia0_irda_01.asm	USCI_A0 IrDA External Loopback Test, 8MHz SMCLK
msp430x261x_uscia0_spi_09.asm	USCI_A0, SPI 3-Wire Master Incremented Data
msp430x261x_uscia0_spi_10.asm	USCI_A0, SPI 3-Wire Slave Data Echo
msp430x261x_uscia0_uart_01.asm	USCI_A0, 115200 UART Echo ISR, DCO SMCLK
msp430x261x_uscia0_uart_03.asm	USCI_A0, UltraLow Pwr UART 9600 Echo ISR, 32kHz ACLK
msp430x261x_uscia0_uart_04.asm	USCI_A0, 9600 UART, SMCLK, LPM0, Echo with over-sampling
msp430x261x_uscia1_uart_02.asm	USCI_A1, Ultra-Low Pwr UART 2400 Echo ISR, 32kHz ACLK
msp430x261x_uscib0_i2c_04.asm	USCI_B0 I2C Master RX single bytes from MSP430 Slave
msp430x261x_uscib0_i2c_05.asm	USCI_B0 I2C Slave TX single bytes to MSP430 Master
msp430x261x_uscib0_i2c_06.asm	USCI_B0 I2C Master TX single bytes to MSP430 Slave
msp430x261x_uscib0_i2c_07.asm	USCI_B0 I2C Slave RX single bytes from MSP430 Master
msp430x261x_uscib0_i2c_08.asm	USCI_B0 I2C Master TX multiple bytes to MSP430 Slave
msp430x261x_uscib0_i2c_09.asm	USCI_B0 I2C Slave RX multiple bytes from MSP430 Master
msp430x261x_uscib0_i2c_10.asm	USCI_B0 I2C Master RX multiple bytes from MSP430 Slave
msp430x261x_uscib0_i2c_11.asm	USCI_B0 I2C Slave TX multiple bytes to MSP430 Master
msp430x261x_uscib0_spi_09.asm	USCI_B0, SPI 3-Wire Master Incremented Data
msp430x261x_uscib0_spi_10.asm	USCI_B0, SPI 3-Wire Slave Data Echo
msp430x261x_vlo_capture.asm	Basic Clock, VLO-Driven Timer with VLO Compensation
msp430x261x_wdt_01.asm	WDT, Toggle P1.0, Interval Overflow ISR, DCO SMCLK
msp430x261x_wdt_02.asm	WDT, Toggle P1.0, Interval Overflow ISR, 32kHz ACLK
msp430x261x_wdt_04.asm	WDT+ Failsafe Clock, WDT mode, DCO SMCLK
msp430x261x_wdt_05.asm	Reset on Invalid Address fetch, Toggle P1.0
msp430x261x_wdt_06.asm	WDT+ Failsafe Clock, 32kHz ACLK

.s43 code examples – IAR	
File name	**Description**
msp430x261x_1.s43	Software Toggle P1.0
msp430x261x_1_vlo.s43	Software Toggle P1.0, MCLK = VLO/8
msp430x261x_adc12_01.s43	ADC12, Sample A0, Set P1.0 if A0 > 0.5*AVcc
msp430x261x_adc12_02.s43	ADC12, Using the Internal Reference
msp430x261x_adc12_03.s43	ADC12, Sample A10 Temp, Set P1.0 if Temp ++ ~2C
msp430x261x_adc12_04.s43	ADC12, Extend Sampling Period with SHT Bits
msp430x261x_adc12_05.s43	ADC12, Using an External Reference
msp430x261x_adc12_06.s43	ADC12, Repeated Sequence of Conversions
msp430x261x_adc12_07.s43	ADC12, Repeated Single Channel Conversions
msp430x261x_adc12_08.s43	ADC12, Using 10 External Channels for Conversion
msp430x261x_adc12_09.s43	ADC12, Sequence of Conversions (non-repeated)
msp430x261x_adc12_10.s43	ADC12, Sample A10 Temp and Convert to oC and oF
msp430x261x_clks.s43	Basic Clock, Output Buffered SMCLK, ACLK, and MCLK
msp430x261x_compA_01.s43	Comparator A, Poll input CA0, result in P1.0
msp430x261x_compA_02.s43	Comparator A, Poll input CA0, CA exchange, result in P1.0
msp430x261x_compA_04.s43	Comparator A, Poll input CA0, result in P1.0

msp430x261x_compA_05.s43	Comparator A, Input to CA0, Interrupt triggered
msp430x261x_dac12_01.s43	DAC12_0, Output 1.0V on DAC0
msp430x261x_dac12_02.s43	DAC12_0, Output 2.0V on DAC1
msp430x261x_dac12_03.s43	DAC12_0, Output Voltage Ramp on DAC0
msp430x261x_dc0_flashcal.s43	DCO Calibration Constants Programmer
msp430x261x_dma_01_IAR.s43	DMA0, Repeated Burst to-from RAM, Software Trigger
msp430x261x_dma_02_IAR.s43	DMA0, Repeated single transfer to P1OUT, TACCR2 Trigger
msp430x261x_dma_03_IAR.s43	DMA0, Repeated single transferUCA1UART 9600, TACCR2, ACLK
msp430x261x_dma_04_IAR.s43	DMA0, single transfer Mode UART1 9600, ACLK
msp430x261x_dma_05_IAR.s43	DMA0, Repeated single transfer to DAC0, Sine Output, TACCR1, DCO
msp430x261x_dma_06_IAR.s43	DMA2, Rpt'd single transfer to DAC1, 8-Bit Sine, TBCCR2, DCO
msp430x261x_dma_07_IAR.s43	DMA0/1, Rpt'd single transfer to DAC12_0/1, Sin/Cos, TACCR1, XT2
msp430x261x_dma_09_IAR.s43	DMA0, ADC12 A10 single blocktransfer Xfer to RAM, TBCCR1, DCO
msp430x261x_dma_10_IAR.s43	DMA0, ADC12 A10 rpt single transfer Xfer to Flash, TBCCR1, DCO
msp430x261x_dma_11_IAR.s43	DMA0/1, ADC12 A10 rpt single transfer Xfer to MPY/RAM, TBCCR1, DCO
msp430x261x_dma_12_IAR.s43	DMA0/1, Block Mode UART1 9600 Auto RX/TX String, ACLK
msp430x261x_flashwrite_01.s43	Flash In-System Programming, Copy SegC to SegD
msp430x261x_flashwrite_03.s43	Flash In-System Programming w/ EEI, Copy SegC to SegD
msp430x261x_flashwrite_04.s43	Flash In-System Programming w/ EEI, Copy SegD to B&C
msp430x261x_fll_01.s43	Basic Clock, Implement Auto RSEL SW FLL
msp430x261x_fll_02.s43	Basic Clock, Implement Cont. SW FLL with Auto RSEL
msp430x261x_hfxt2.s43	Basic Clock, MCLK Configured to Operate from XT2 HF XTAL
msp430x261x_hfxt2_nmi.s43	Basic Clock, MCLK Sourced from HF XTAL XT2, NMI
msp430x261x_lpm3.s43	Basic Clock, LPM3 Using WDT ISR, 32kHz ACLK
msp430x261x_lpm3_vlo.s43	Basic Clock, LPM3 Using WDT ISR, VLO ACLK
msp430x261x_MPY_01.s43	16x16 Unsigned Multiply
msp430x261x_MPY_02.s43	8x8 Unsigned Multiply
msp430x261x_MPY_03.s43	16x16 Signed Multiply
msp430x261x_MPY_04.s43	8x8 Signed Multiply
msp430x261x_MPY_05.s43	16x16 Unsigned Multiply Accumulate
msp430x261x_MPY_06.s43	8x8 Unsigned Multiply Accumulate
msp430x261x_MPY_07.s43	16x16 Signed Multiply Accumulate
msp430x261x_MPY_08.s43	8x8 Signed Multiply Accumulate
msp430x261x_nmi.s43	Configure RST/NMI as NMI
msp430x261x_OF_XT2.s43	XT2 Oscillator Fault Detection
msp430x261x_P1_01.s43	Software Poll P1.3, Set P1.0 if P1.3 = 1
msp430x261x_P1_02.s43	Software Port Interrupt Service on P1.3 from LPM4
msp430x261x_P1_05.s43	Write a byte to Port 1
msp430x261x_P7_05.s43	Write a byte to Port 7
msp430x261x_P8_08.s43	Write a byte to Port 8
msp430x261x_PA_05.s43	Write a word to Port A
msp430x261x_rosc.s43	DCOCLK Biased with External Resistor Rosc
msp430x261x_svs_01.s43	SVS, POR @ 2.5V Vcc
msp430x261x_ta_01.s43	Timer_A, Toggle P1.0, CCR0 Cont. Mode ISR, DCO SMCLK
msp430x261x_ta_02.s43	Timer_A, Toggle P1.0, CCR0 Up Mode ISR, DCO SMCLK

msp430x261x_ta_03.s43	Timer_A, Toggle P1.0, Overflow ISR, DCO SMCLK
msp430x261x_ta_04.s43	Timer_A, Toggle P1.0, Overflow ISR, 32kHz ACLK
msp430x261x_ta_05.s43	Timer_A, Toggle P1.0, CCR0 Up Mode ISR, 32kHz ACLK
msp430x261x_ta_08.s43	Timer_A, Toggle P1.0,P1.2 & P2.0 Cont. Mode ISR, 32kHz ACLK
msp430x261x_ta_11.s43	Timer_A, Toggle P1.1/TA0, Up Mode, 32kHz ACLK
msp430x261x_ta_13.s43	Timer_A, Toggle P1.1/TA0, Up/Down Mode, DCO SMCLK
msp430x261x_ta_14.s43	Timer_A, Toggle P1.1/TA0, Up/Down Mode, 32kHz ACLK
msp430x261x_ta_16.s43	Timer_A, PWM TA1-2 Up Mode, DCO SMCLK
msp430x261x_ta_17.s43	Timer_A, PWM TA1-2, Up Mode, 32kHz ACLK
msp430x261x_ta_19.s43	Timer_A, PWM TA1-2, Up/Down Mode, DCO SMCLK
msp430x261x_ta_20.s43	Timer_A, PWM TA1-2, Up/Down Mode, DCO SMCLK
msp430x261x_tb_01.s43	Timer_B, Toggle P1.0, CCR0 Cont. Mode ISR, DCO SMCLK
msp430x261x_tb_02.s43	Timer_B, Toggle P1.0, CCR0 Up Mode ISR, DCO SMCLK
msp430x261x_tb_03.s43	Timer_B, Toggle P1.0, Overflow ISR, DCO SMCLK
msp430x261x_tb_04.s43	Timer_B, Toggle P1.0, Overflow ISR, 32kHz ACLK
msp430x261x_tb_05.s43	Timer_B, Toggle P1.0, CCR0 Up Mode ISR, 32kHz ACLK
msp430x261x_tb_07.s43	Timer_B, PWM TB1-6, Up Mode, 32kHz ACLK
msp430x261x_uscia0_irda_01.s43	USCI_A0 IrDA External Loopback Test, 8MHz SMCLK
msp430x261x_uscia0_spi_09.s43	USCI_A0, SPI 3-Wire Master Incremented Data
msp430x261x_uscia0_spi_10.s43	USCI_A0, SPI 3-Wire Slave Data Echo
msp430x261x_uscia0_uart_01.s43	USCI_A0, 115200 UART Echo ISR, DCO SMCLK
msp430x261x_uscia0_uart_03.s43	USCI_A0, Ultra-Low Pwr UART 9600 Echo ISR, 32kHz ACLK
msp430x261x_uscia0_uart_04.s43	USCI_A0, 9600 UART, SMCLK, LPM0, Echo with over-sampling
msp430x261x_uscia1_uart_02.s43	USCI_A1, Ultra-Low Pwr UART 2400 Echo ISR, 32kHz ACLK
msp430x261x_uscib0_i2c_04.s43	USCI_B0 I2C Master RX single bytes from MSP430 Slave
msp430x261x_uscib0_i2c_05.s43	USCI_B0 I2C Slave TX single bytes to MSP430 Master
msp430x261x_uscib0_i2c_06.s43	USCI_B0 I2C Master TX single bytes to MSP430 Slave
msp430x261x_uscib0_i2c_07.s43	USCI_B0 I2C Slave RX single bytes from MSP430 Master
msp430x261x_uscib0_i2c_08.s43	USCI_B0 I2C Master TX multiple bytes to MSP430 Slave
msp430x261x_uscib0_i2c_09.s43	USCI_B0 I2C Slave RX multiple bytes from MSP430 Master
msp430x261x_uscib0_i2c_10.s43	USCI_B0 I2C Master RX multiple bytes from MSP430 Slave
msp430x261x_uscib0_i2c_11.s43	USCI_B0 I2C Slave TX multiple bytes to MSP430 Master
msp430x261x_uscib0_spi_09.s43	USCI_B0, SPI 3-Wire Master Incremented Data
msp430x261x_uscib0_spi_10.s43	USCI_B0, SPI 3-Wire Slave Data Echo
msp430x261x_vlo_capture.s43	Basic Clock, VLO-Driven Timer with VLO Compensation
msp430x261x_wdt_01.s43	WDT, Toggle P1.0, Interval Overflow ISR, DCO SMCLK
msp430x261x_wdt_02.s43	WDT, Toggle P1.0, Interval Overflow ISR, 32kHz ACLK
msp430x261x_wdt_04.s43	WDT+ Failsafe Clock, WDT mode, DCO SMCLK
msp430x261x_wdt_05.s43	Reset on Invalid Address fetch, Toggle P1.0
msp430x261x_wdt_06.s43	WDT+ Failsafe Clock, 32kHz ACLK

C code examples – IAR & CCS	
File name	**Description**
msp430x261x_1.c	Software Toggle P1.0
msp430x261x_1_vlo.c	Software Toggle P1.0, MCLK = VLO/8
msp430x261x_adc12_01.c	ADC12, Sample A0, Set P1.0 if A0 > 0.5*AVcc
msp430x261x_adc12_02.c	ADC12, Using the Internal Reference
msp430x261x_adc12_03.c	ADC12, Sample A10 Temp, Set P1.0 if Temp ++ ~2C
msp430x261x_adc12_04.c	ADC12, Extend Sampling Period with SHT Bits
msp430x261x_adc12_05.c	ADC12, Using an External Reference
msp430x261x_adc12_06.c	ADC12, Repeated Sequence of Conversions
msp430x261x_adc12_07.c	ADC12, Repeated Single Channel Conversions
msp430x261x_adc12_08.c	ADC12, Using 10 External Channels for Conversion
msp430x261x_adc12_09.c	ADC12, Sequence of Conversions (non-repeated)
msp430x261x_adc12_10.c	ADC12, Sample A10 Temp and Convert to oC and oF
msp430x261x_clks.c	Basic Clock, Output Buffered SMCLK, ACLK, and MCLK
msp430x261x_compA_01.c	Comparator A, Poll input CA0, result in P1.0
msp430x261x_compA_02.c	Comparator A, Poll input CA0, CA exchange, result in P1.0
msp430x261x_compA_04.c	Comparator A, Poll input CA0, result in P1.0
msp430x261x_compA_05.c	Comparator A, Input to CA0, interrupt triggered
msp430x261x_dac12_01.c	DAC12_0, Output 1.0V on DAC0
msp430x261x_dac12_02.c	DAC12_0, Output 2.0V on DAC1
msp430x261x_dac12_03.c	DAC12_0, Output Voltage Ramp on DAC0
msp430x261x_dc0_flashcal.c	DCO Calibration Constants Programmer
msp430x261x_dma_01_CCE.c	(Built with CCE) DMA0, Repeated Burst to-from RAM, Software Trigger
msp430x261x_dma_02_CCE.c	(Built with CCE) DMA0, Repeated single transfer to P1OUT, TACCR2 Trigger
msp430x261x_dma_03_CCE.c	(Built with CCE) DMA0, Repeated single transfer UCA1UART 9600, TACCR2, ACLK
msp430x261x_dma_04_CCE.c	(Built with CCE) DMA0, single transfer Mode UART1 9600, ACLK
msp430x261x_dma_05_CCE.c	(Built with CCE) DMA0, Repeated single transfer to DAC0, Sine Output, TACCR1, DCO
msp430x261x_dma_06_CCE.c	(Built with CCE) DMA2, Rpt'd single transfer to DAC1, 8-Bit Sine, TBCCR2, DCO
msp430x261x_dma_07_CCE.c	(Built with CCE) DMA0/1, Rpt'd single transfer to DAC12_0/1, Sin/Cos, TACCR1, XT2
msp430x261x_dma_09_CCE.c	(Built with CCE) DMA0, ADC12 A10 single Block Xfer to RAM, TBCCR1, DCO
msp430x261x_dma_10_CCE.c	(Built with CCE) DMA0, ADC12 A10 Block Xfer to Flash, TBCCR1, DCO
msp430x261x_dma_11_CCE.c	(Built with CCE) DMA0/1, ADC12 A10 rpt single transfer Xfer to MPY/RAM, TBCCR1, DCO
msp430x261x_dma_12_CCE.c	(Built with CCE) DMA0/1, rpt single transfer Mode UART1 9600 Auto RX/TX String, ACLK
msp430x261x_dma_01_IAR.c	(Built with IAR) DMA0, Repeated Burst to-from RAM, Software Trigger
msp430x261x_dma_02_IAR.c	(Built with IAR) DMA0, Repeated single transfer to P1OUT, TACCR2 Trigger
msp430x261x_dma_03_IAR.c	(Built with IAR) DMA0, Repeated single transferUCA1UART 9600, TACCR2, ACLK
msp430x261x_dma_04_IAR.c	(Built with IAR) DMA0, single transfer Mode UART1 9600, ACLK
msp430x261x_dma_05_IAR.c	(Built with IAR) DMA0, Repeated single transfer to DAC0, Sine Output, TACCR1, DCO
msp430x261x_dma_06_IAR.c	(Built with IAR) DMA2, Rpt'd single transfer to DAC1, 8-Bit Sine, TBCCR2, DCO

msp430x261x_dma_07_IAR.c	(Built with IAR) DMA0/1, Rpt'd single transfer to DAC12_0/1, Sin/Cos, TACCR1, XT2
msp430x261x_dma_09_IAR.c	(Built with IAR) DMA0, ADC12 A10 single blocktransfer Xfer to RAM, TBCCR1, DCO
msp430x261x_dma_10_IAR.c	(Built with IAR) DMA0, ADC12 A10 rpt single transfer Xfer to Flash, TBCCR1, DCO
msp430x261x_dma_11_IAR.c	(Built with IAR) DMA0/1, ADC12 A10 rpt single transfer Xfer to MPY/RAM, TBCCR1, DCO
msp430x261x_dma_12_IAR.c	(Built with IAR) DMA0/1, Block Mode UART1 9600 Auto RX/TX String, ACLK
msp430x261x_flashwrite_01.c	Flash In-System Programming, Copy SegC to SegD
msp430x261x_flashwrite_03.c	Flash In-System Programming w/ EEI, Copy SegC to SegD
msp430x261x_flashwrite_04.c	Flash In-System Programming w/ EEI, Copy SegD to B&C
msp430x261x_fll_01.c	Basic Clock, Implement Auto RSEL SW FLL
msp430x261x_fll_02.c	Basic Clock, Implement Cont. SW FLL with Auto RSEL
msp430x261x_hfxt2.c	Basic Clock, MCLK Configured to Operate from XT2 HF XTAL
msp430x261x_hfxt2_nmi.c	Basic Clock, MCLK Sourced from HF XTAL XT2, NMI
msp430x261x_lpm3.c	Basic Clock, LPM3 Using WDT ISR, 32kHz ACLK
msp430x261x_lpm3_vlo.c	Basic Clock, LPM3 Using WDT ISR, VLO ACLK
msp430x261x_MPY_01.c	16x16 Unsigned Multiply
msp430x261x_MPY_02.c	8x8 Unsigned Multiply
msp430x261x_MPY_03.c	16x16 Signed Multiply
msp430x261x_MPY_04.c	8x8 Signed Multiply
msp430x261x_MPY_05.c	16x16 Unsigned Multiply Accumulate
msp430x261x_MPY_06.c	8x8 Unsigned Multiply Accumulate
msp430x261x_MPY_07.c	16x16 Signed Multiply Accumulate
msp430x261x_MPY_08.c	8x8 Signed Multiply Accumulate
msp430x261x_nmi.c	Configure RST/NMI as NMI
msp430x261x_OF_XT2.c	XT2 Oscillator Fault Detection
msp430x261x_P1_01.c	Software Poll P1.3, Set P1.0 if P1.3 = 1
msp430x261x_P1_02.c	Software Port Interrupt Service on P1.3 from LPM4
msp430x261x_P1_05.c	Write a byte to Port 1
msp430x261x_P7_05.c	Write a byte to Port 7
msp430x261x_P8_08.c	Write a byte to Port 8
msp430x261x_PA_05.c	Write a word to Port A
msp430x261x_rosc.c	DCOCLK Biased with External Resistor Rosc
msp430x261x_svs_01.c	SVS, POR @ 2.5V Vcc
msp430x261x_ta_01.c	Timer_A, Toggle P1.0, CCR0 Cont. Mode ISR, DCO SMCLK
msp430x261x_ta_02.c	Timer_A, Toggle P1.0, CCR0 Up Mode ISR, DCO SMCLK
msp430x261x_ta_03.c	Timer_A, Toggle P1.0, Overflow ISR, DCO SMCLK
msp430x261x_ta_04.c	Timer_A, Toggle P1.0, Overflow ISR, 32kHz ACLK
msp430x261x_ta_05.c	Timer_A, Toggle P1.0, CCR0 Up Mode ISR, 32kHz ACLK
msp430x261x_ta_08.c	Timer_A, Toggle P1.0,P1.2 & P2.0 Cont. Mode ISR, 32kHz ACLK
msp430x261x_ta_11.c	Timer_A, Toggle P1.1/TA0, Up Mode, 32kHz ACLK
msp430x261x_ta_13.c	Timer_A, Toggle P1.1/TA0, Up/Down Mode, DCO SMCLK
msp430x261x_ta_14.c	Timer_A, Toggle P1.1/TA0, Up/Down Mode, 32kHz ACLK
msp430x261x_ta_16.c	Timer_A, PWM TA1-2 Up Mode, DCO SMCLK
msp430x261x_ta_17.c	Timer_A, PWM TA1-2, Up Mode, 32kHz ACLK

msp430x261x_ta_19.c	Timer_A, PWM TA1-2, Up/Down Mode, DCO SMCLK
msp430x261x_ta_20.c	Timer_A, PWM TA1-2, Up/Down Mode, 32kHz ACLK
msp430x261x_tb_01.c	Timer_B, Toggle P1.0, CCR0 Cont. Mode ISR, DCO SMCLK
msp430x261x_tb_02.c	Timer_B, Toggle P1.0, CCR0 Up Mode ISR, DCO SMCLK
msp430x261x_tb_03.c	Timer_B, Toggle P1.0, Overflow ISR, DCO SMCLK
msp430x261x_tb_04.c	Timer_B, Toggle P1.0, Overflow ISR, 32kHz ACLK
msp430x261x_tb_05.c	Timer_B, Toggle P1.0, CCR0 Up Mode ISR, 32kHz ACLK
msp430x261x_tb_07.c	Timer_B, PWM TB1-6, Up Mode, 32kHz ACLK
msp430x261x_uscia0_irda_01.c	USCI_A0 IrDA External Loopback Test, 8MHz SMCLK
msp430x261x_uscia0_spi_09.c	USCI_A0, SPI 3-Wire Master Incremented Data
msp430x261x_uscia0_spi_10.c	USCI_A0, SPI 3-Wire Slave Data Echo
msp430x261x_uscia0_uart_01.c	UUSCI_A0, 115200 UART Echo ISR, DCO SMCLK
msp430x261x_uscia0_uart_03.c	USCI_A0, Ultra-Low Pwr UART 9600 Echo ISR, 32kHz ACLK
msp430x261x_uscia0_uart_04.c	UUSCI_A0, 9600 UART, SMCLK, LPM0, Echo with over-sampling
msp430x261x_uscia1_uart_02.c	USCI_A1, Ultra-Low Pwr UART 2400 Echo ISR, 32kHz ACLK
msp430x261x_uscib0_i2c_04.c	USCI_B0 I2C Master RX single bytes from MSP430 Slave
msp430x261x_uscib0_i2c_05.c	USCI_B0 I2C Slave TX single bytes to MSP430 Master
msp430x261x_uscib0_i2c_06.c	USCI_B0 I2C Master TX single bytes to MSP430 Slave
msp430x261x_uscib0_i2c_07.c	USCI_B0 I2C Slave RX single bytes from MSP430 Master
msp430x261x_uscib0_i2c_08.c	USCI_B0 I2C Master TX multiple bytes to MSP430 Slave
msp430x261x_uscib0_i2c_09.c	USCI_B0 I2C Slave RX multiple bytes from MSP430 Master
msp430x261x_uscib0_i2c_10.c	USCI_B0 I2C Master RX multiple bytes from MSP430 Slave
msp430x261x_uscib0_i2c_11.c	USCI_B0 I2C Slave TX multiple bytes to MSP430 Master
msp430x261x_uscib0_spi_09.c	USCI_B0, SPI 3-Wire Master Incremented Data
msp430x261x_uscib0_spi_10.c	USCI_B0, SPI 3-Wire Slave Data Echo
msp430x261x_vlo_capture.c	Basic Clock, VLO-Driven Timer with VLO Compensation
msp430x261x_wdt_01.c	WDT, Toggle P1.0, Interval Overflow ISR, DCO SMCLK
msp430x261x_wdt_02.c	WDT, Toggle P1.0, Interval Overflow ISR, 32kHz ACLK
msp430x261x_wdt_04.c	WDT+ Failsafe Clock, WDT mode, DCO SMCLK
msp430x261x_wdt_05.c	Reset on Invalid Address fetch, Toggle P1.0
msp430x261x_wdt_06.c	WDT+ Failsafe Clock, 32kHz ACLK
msp430x261x_adc12_11.c	ADC12, Single Channel Extended Sample, TA1 Trigger
msp430x261x_uscib0_i2c_16.c	USCI_B0 to USCI_B1 I2C RX and TX single bytes

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