Texas Instruments

ADS528x EVM User's Guide

User's Guide

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Contents

List of Figures

List of Tables

1 Overview

This preliminary user's guide gives a general overview of the ADS5281/82/87 (ADS528X) QFN evaluation module (EVM) and provides a general description of the features and functions to be considered while using this module. The EVM is pictured in Figure 1.

1.1 Purpose

The EVM provides a platform for evaluating the eight-channel ADS528X analog-to-digital converter (ADC) under various signal, reference, and supply conditions. This document should be used in combination with the EVM schematic diagram supplied. The ADS5281 and ADS5282 are 12-bit ADCs, whereas the ADS5287 is a 10-bit ADC.

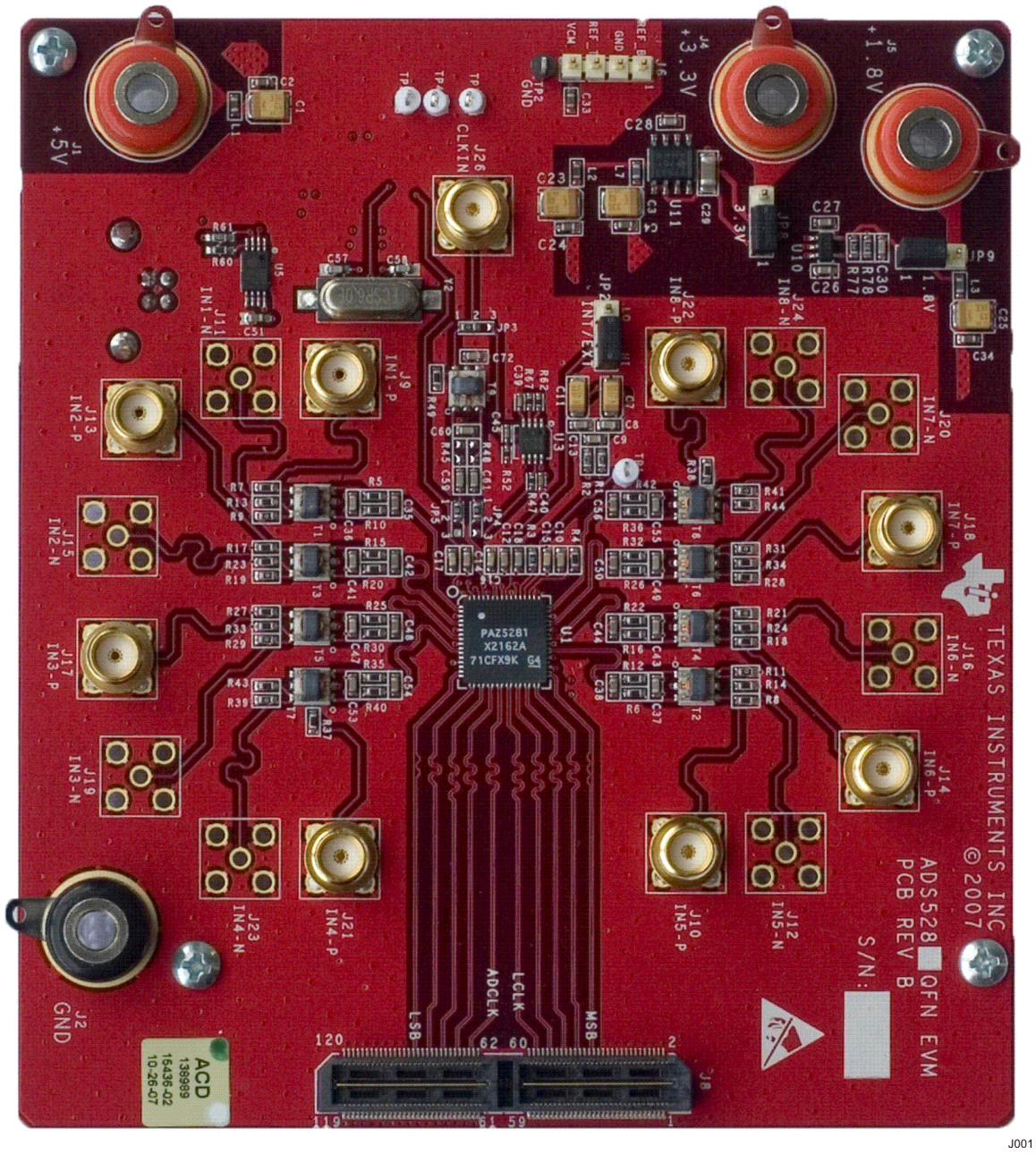

Figure 1. ADS5281 EVM

1.2 EVM Basic Functions

Eight analog inputs to the ADC are provided via external SMA connectors.

The EVM provides an external SMA connector for input of the ADC clock. The ADC can be clocked using either a single-ended or differential clock. Provisions are made on the EVM to allow users to evaluate the ADC using a single-ended PECL clock and a differential transformer-coupled clock.

Digital output from the EVM is via a high-speed, high-density Samtec output header. The digital output connector mates directly to the TSW1200 Rev B or through an adapter to the TI ADSDeSer-50EVM, both of which deserialize the serial data stream into parallel CMOS data.

Power connections to the EVM are via banana jack sockets. Separate sockets are provided for the ADC analog and ADC digital supplies and for the auxiliary circuits.

1.3 ADS528x EVM Quick Start Procedure

The ADS528x EVM provides a flexible means of evaluating the ADS528x in a number of modes of operation. A basic setup procedure that can be used as a board confidence check is as follows:

1. Verify all jumper settings against the schematic jumper list in Table 1.

Table 1. Three-Pin Jumper List

JUMPER	FUNCTION	LOCATION: PINS 1–2	LOCATION: PINS 2–3	DEFAULT
JP2	ADC internal or external reference selection	ADC internal reference	ADC external reference	1–2
JP3 (SMT)	EVM clock input selection	Transformer coupled	Single-ended PECL	1–2
JP4 (SMT)	ADC CLKP	Transformer	Single-ended PECL	1–2
JP5 (SMT)	ADC CLKM	Transformer	GND	1–2
JP8	Selects power management configuration	ADC powered by LDO (3.3 V)	ADC powered by J4 (3.3 V)	1–2
JP9	Selects power management configuration	ADC powered by LDO (1.8 V)	ADC powered by J5 (1.8 V)	1–2

2. Connect a 5-V supply to J1 and its return to J2.
3. Switch power supplies on.
4. Using a function generator with 50-Ω output, generate a 0-V offset, 1.5-Vpp sine-wave clock into J26. The frequency of the clock must be within the specification for the device speed grade.
5. Use a frequency generator with a 50-Ω output to provide a 5-MHz, 0-V offset, –1-dBFS-amplitude sine-wave signal into J9. This provides a transformer-coupled differential input signal to the ADC.
6. Connect the USB cable, open the PC software and provide a reset command. **For first-time use, see Section 3.1** for installation instructions.
7. Connect J8 to the ADS5281DeSerAdapter+ADSDeser-50EVM or TSW1200 deserializer card to evaluate the ADC digital data using a logic analyzer.

Note: **Software Operation**: Users must use the accompanying software to issue a reset command before taking measurements. In addition to providing the ADS528X with the initialization register writes detailed in the data sheet, the accompanying software also sets the state of ADC pins ADCRESET and PD. Failure to do so can cause improper operation.

2 Circuit Description

2.1 Schematic Diagram

The schematic diagram for the EVM is in Section 6.3.

2.2 Circuit Function

The following sections describe the function of individual circuits. Refer to the relevant data sheet for device operating characteristics.

2.2.1 Power

Power is supplied to the EVM via banana jack sockets. By default, the EVM is configured to use a power management solution to supply the ADC and analog and digital power supplies, allowing users to power the board with a single 5-V power supply. The ADC power management solution is based on TI's TPS77533 and TPS73218, which supply 3.3 V and 1.8 V, respectively. In addition, the EVM offers the capability to supply to the ADC independent 3.3-V analog and 1.8-V digital supplies. The circuit board uses only one ground plane, and the heat slug is tied to ground with multiple vias to provide for thermal dissipation. Table 2 offers a snapshot of the power-supply options.

Table 2. EVM Power-Supply Options

EVM Banana Jack	DESCRIPTION
J1	Auxiliary circuit 5-V digital supply: PECL driver and USB circuitry
J2	Single ground plane
J4	ADS528x 3.3-V analog supply (only active when JP8 = 2–3)
J5	ADS528x 1.8-V digital supply (only active when JP9 = 2–3)

2.2.2 Clock Input

A single-ended square or sinusoidal clock input should be applied to J26. The clock frequency should not exceed the maximum speed rating found in the data sheet. Several different clocking options exist to allow flexible evaluation of the ADC.

In the default case, a single-ended clock is converted to a differential clock using a Mini-Circuits TC1-1T transformer. When using this option, the ADC should be configured in differential clock mode by writing 0x8001 to ADC register address 0x42. By default, after a software reset this option is asserted to coincide with the EVM default.

A second EVM option allows the ADC to be configured in single-ended mode. This is provided to the ADC using an On Semiconductor™ MC100EPT21 amplifier, which provides for sine-wave to square-wave conversion. This configuration can be used for both ADS528X and ADS527X devices. To use this mode, use the surface-mount jumpers JP3, JP4, and JP5, and configure each one of them to have positions 2–3 shorted.

2.2.3 External References

The EVM offers the ability to force external references to the ADC. By default, the ADC is configured to use the references generated internal to the ADC. To force the ADC to use external references, users must short JP2 pads 2–3, which in turn grounds the INT/EXT pin of the ADC. Users can then use J6 pin 1 to force a REFB and pin 3 to force a REFT voltage. GND should be connected to J6 pin 2.

2.2.4 Analog Inputs

The EVM provides eight analog inputs, using an SMA connector for each of the eight channels of the ADC. SMA channel inputs are J9, J10, J13, J14, J17, J18, J21, and J22. By default, the ADC accepts a single-ended input and translates it to a differential signal using a Mini Circuits TC1-1T transformer. The ADC inputs are dc-biased by feeding the ADC VCM voltage to the transformer center tap on the secondary windings. Provisions have also been made on the EVM to allow for differential inputs using two SMAs per input channel.

2.2.5 Digital Outputs

The serial LVDS digital outputs can be accessed through the J8 output connector. The EVM is designed to be interfaced to the TI TSW1200 Rev B deserializer card, which plugs into J8. In addition, the EVM can be interfaced to the ADSDeSer-50EVM using a translation card, the ADS5281DeSerAdapter. Both the TSW1200 Rev B and the ADSDeSer-50EVM contain the required parallel 100-Ω termination resistor that must be placed at the receiver to terminate each LVDS data pair properly.

Note: **TSW1200 Rev B:** Users wishing to use the TSW1200 for deserialization should note that the minimium ADC sampling frequency this can be operated at is 32 MHz. The TSW1200 uses a digital clock manager (DCM) with a minimium operational frequency of 32 MHz.

Full documentation on the TI ADSDeSer-50EVM deserializer is found in the *ADSDeSer-50EVM Evaluation Module User's Guide* (SBAU091) and *Connecting Xilinx FPGAs to Texas Instruments ADS527x Series ADCs*, Xilinx™ application report XAPP774. The VHDL deserializer source code can be found on the Xilinx Web site.

3 TI ADC SPI Control Interface

This section describes the software designed to communicate with the ADC three-wire SPI interface. The information is to be used in conjunction with the device data sheet, which explains the valid registers of the device.

3.1 Installing the ADC SPI Control Software

The ADC SPI control software can be installed on a personal computer by running the setup.exe file located on the CD. This file installs the graphical user interface (GUI) along with the USB drivers needed to communicate to the USB port that resides on the EVM. After the software is installed and the USB cable has been plugged in for the first time, the user is prompted to complete the installation of the USB drivers. When prompted, users should allow the Windows™ operating system to search for device drivers, and it should automatically find the TI ADC SPI interface drivers. See Figure 2.

Note: **First-time operation**: For proper installation of the necessary USB drivers, users should install the accompanying software before connecting the USB cable to the EVM for the first time. Not doing so could cause problems in communicating to the EVM.

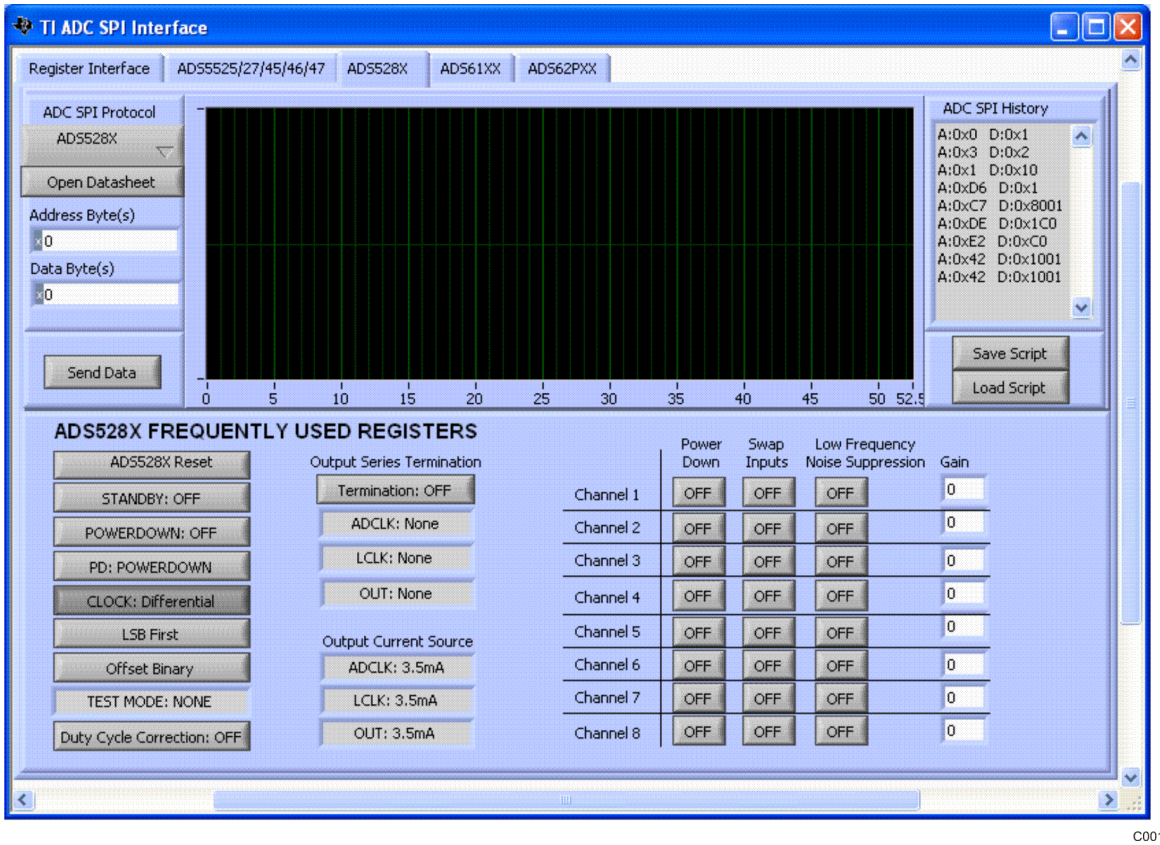

Figure 2. TI ADC SPC Interface Screen

3.2 Using the TI ADC SPI Interface Software

Once the software is installed and the USB cable is connected, three primary modes of operating the software are available: SPI register write, SPI register write using a script file, and ADS528X frequently used registers.

3.2.1 SPI Register Write

The most basic mode of operation allows full control of writing to individual register addresses. In the top left corner of the interface screen (Figure 2), select the ADS528X ADC from the ADC SPI Protocol drop-down list. Next, type the hexadecimal (hex) Address Bytes(s) in and Data Byte(s), which can be found in the device data sheet. When you are ready to send this command to the ADC, press *Enter* on your keyboard or click the *Send Data* button. The graph indicator is updated with the patterns sent to the ADC. The default inputs to both the Address Byte(s) and Data Byte(s) fields are hex inputs as designated by the small *x* in the control. Users can change the default input style by clicking on the *x* to binary, decimal, octal, or hex. Multiple register writes can be written simply by changing the contents of the Address Byte(s) and Data Byte(s) fields and pressing "Enter" or "Send Data" again.

3.2.2 SPI Register Write Using a Script File

For situations where the same multiple registers must be written on a frequent basis, users can easily save a script file representing all of the register writes they have performed after a Reset has been issued by simply clicking on the *Save Script* button. This can easily be loaded at a later time by using the *Load Script* button. When ready to write the contents of the script file to the ADC, users can press the *Load Script* button and be prompted for the file location of their script file. The commands are sent to the ADC when the user acknowledges the selection of the file. Please note that the graph indicator and the frequently used register buttons are not updated when a script file is used.

Conversely, users can by using a text editor easily create a script file containing all ADC register writes. An example script file is located in the \\Install Directory\ADC SPI Control\Script Files\ADS5281_Init.reg_ADS528X. Users who wish to take advantage of writing their own script files should start by using the ADS5281_Init.reg_ADS528X as a template file. When editing script files manually, make sure there is no carriage return following the last register write.

3.2.2.1 ADS528X Frequently Used Registers

For ease of use, several buttons have been added that allow one-click register writes of commonly used features found in Table 3. These buttons represent a subset of the available features found on the ADS528X. The buttons are found in the ADS528X tab, as these commands are specific to the ADS528X ADC only. The software writes to the ADC both the contents of the associated address and data when the button is clicked. When the ADS528X Reset button is pressed, it issues a software reset to the ADC, and it resets the button values to match the contents inside of the ADC. The graph indicator plots the SPI commands written to the ADC when a button has been pressed.

Table 3. ADS528X Frequently Used Registers

Default Value	Alternate Value	Description
ADS528X Reset		Issues a software reset and also sends the initialization routine outlined in the data sheet. Furthermore, the clock is set to differential, which matches the default EVM configuration. A Reset should take place before any evaluation is done.
Standby: Off	Standby: On	Toggles the ADC standby.
Powerdown: Off	Powerdown: On	Toggles the ADC power down.
PD: Powerdown	PD: Standby	Assigns the ADS528X PD pin either a power-down or standby function.
Clock: Standby	Clock: Differential	Sets the ADC to accept either a single-ended or a differential clock. By defualt the ADS528X EVM is configured for a differential clock.
LSB first	MSB first	Toggles the ADC output format.
Testmode: None	Output = Ramp, Output = Deskew, Output = Synch	Sets the ADC to ignore the analog input and to apply a test pattern on the digital output.
Duty Cycle Correction: Off	Duty Cycle Correction: On	Toggles the duty-cycle correction feature.
Termination: Off	Termination: On	Enables the ability to provide a series source termination on the output signals.
ADCLK: None	ADCLK: 260, 150, 94, 125, 80, 66, 55 Ω	Changes the value of the source termination on ADCLK. Note that Termination must be On for values to take effect.
LCLK: None	LCLK: 260, 150, 94, 125, 80, 66, 55 Ω	Changes the value of the source termination on LCLK. Note that Termination must be On for values to take effect.
OUT: None	OUT: 260, 150, 94, 125, 80, 66, 55 Ω	Changes the value of the source termination on the outputs Note that Termination must be On for values to take effect.
ADCLK: 3.5 mA	ADCLK: 0.5–7.5 mA	Changes the output source current on ADCLK.
LCLK: 3.5 mA	LCLK: 0.5–7.5 mA	Changes the output source current on LCLK.
OUT: 3.5 mA	OUT: 0.5–7.5 mA	Changes the output source current on OUT.
Power Down: Off (per channel control)	Power Down: On (per channel control)	On an individual-channel basis, allows the user to toggle power down.
Swap Inputs: Off (per channel control)	Swap Inputs: On (per channel control)	On an individual-channel basis, allows the user to toggle power down.
Low-Frequency Noise Suppression: Off (per channel control)	Low-Frequency Noise Suppression: On (per channel control)	On an individual-channel basis, allows the user to toggle the low-frequency noise-suppression mode.
Gain = 0 db–12 dB (per channel control)	Gain = 0 db–12 dB (per channel control)	On an individual-channel basis, allows the user to apply gain.

4 ADC Evaluation

This section describes how to set up a typical ADC evaluation system that is similar to what TI uses to perform testing for data-sheet generation. Consequently, the information in this section is generic in nature and is applicable to all high-speed, high-resolution ADC evaluations. This section covers signal tone analysis, which yields ADC data-sheet figures of merit such as signal-to-noise ratio (SNR) and spurious free dynamic range (SFDR).

4.1 Hardware Selection

To reveal the true performance of the ADC under evaluation, great care should be taken in selecting both the ADC signal source and ADC clocking source.

4.1.1 Analog Input Signal Generator

When choosing the quality of the ADC analog input source, consider both harmonic distortion performance of the signal generator and the noise performance of the source.

In many cases, the harmonic distortion performance of the signal generator is inferior to that of the ADC, and additional filtering is needed if users expect to reproduce the ADC SFDR numbers found in the data sheet. Users can easily evaluate the harmonic distortion of their signal generator by hooking it directly to a spectrum analyzer and measuring the power of the output signal and comparing that to the power of the integer multiples of the output-signal frequency. If the harmonic distortion is worse than the ADC under evaluation, the ADC digitizes the performance of the signal generator and the true ADC SFDR is masked. To alleviate this, it is recommended that users provide additional LC filtering after the signal generator output.

Another important metric when deciding on a signal generator is its noise performance. As with the distortion performance, if the noise performance is worse than that of the ADC under evaluation, the ADC digitizes the performance of the source. Noise can be broken into two components, broadband noise and close-in phase noise. Broadband noise can be improved by the LC filter added to improve distortion performance; however, the close-in phase noise typically cannot be improved by additional filtering. Therefore, when selecting an analog signal source, it is important to review the manufacturer's phase-noise plots and take care to choose a signal generator with the best phase-noise performance.

4.1.2 Clock Signal Generator

Equally important in the high-performance ADC evaluation setup is the selection of the clocking source. Most modern ADCs, the ADS61xx included, accept either a sinusoidal or a square-wave clock input. The key metric in selecting a clocking source is selecting a source with the lowest jitter. This becomes increasingly important as the ADC input frequency (f_{in}) increases, because the ADC SNR evaluation setups can become jitter-limited (t_j) as shown by the following equation.

$$\text{SNR (dBc)} = 20 \log (2\pi \times f_{in} \times t_j(\text{rms}))$$

In theory, a square-wave source with femtosecond jitter would be ideal for an ADC evaluation setup. However, in practical terms, most commercially available square-wave generators offer jitter measured in picoseconds, which is too great for high-resolution ADC evaluation setups. Therefore, most evaluation setups rely on the ADC internal clock buffer to convert a sinusoidal input signal into an ultralow-jitter square wave. When selecting a sinusoidal clocking source, it has been shown that phase noise has a direct impact on jitter performance. Consequently, great scrutiny should be applied to the phase-noise performance of the clocking signal generator. TI has found that high-Q monolithic crystal filters can improve the phase noise of the signal generator, and these filters become essential elements of the evaluation setup when high ADC input frequencies are being evaluated.

4.2 Coherent Input Frequency Selection

Typical ADC analysis requires users to collect the resulting time-domain data and perform a Fourier transform to analyze the data in the frequency domain. A stipulation of the Fourier transform is that the signal must be continuous-time; however, this is impractical when looking at a finite set of ADC samples, usually collected from a logic analyzer. Consequently, users typically apply a window function to minimize the time-domain discontinuities that arise when analyzing a finite set of samples. For ADC analysis, window functions have their own frequency signatures or lobes that distort both SNR and SFDR measurements of the ADC.

TI uses the concept of coherent sampling to work around the use of a window function. The central premise of coherent sampling entails that the input signal into the ADC is carefully chosen such that when a continuous-time signal is reconstructed from a finite sample set, no time-domain discontinuities exist. To achieve this, the input frequency must be an integer multiple of the ratio of the ADC sample rate (f_s) and the number of samples collected from the logic analyzer (N_s). The ratio of f_s to N_s is typically referred to as the fundamental frequency (f_f). Determining the ADC input frequency is a two-step process. First, the users select the frequency of interest for evaluating the ADC; then, they divide this by the fundamental frequency. This typically yields a non-integer value, which should be rounded to the nearest odd, preferably prime, integer. Once that integer, or frequency bin (f_{bin}), has been determined, users multiply this with the fundamental frequency to obtain a coherent frequency to program into their ADC input signal generator. The procedure is summarized as follows.

$f_f = f_s/N_s$

$f_{bin} = \text{Odd\_round}(f_{desired}/f_f)$

Coherent frequency = $f_f \times f_{bin}$

5 Errata

This section describes the known issues with Rev B of the EVM.

5.1 Silkscreen Errata

The JP2 silkscreen incorrectly identifies the internal (INT) and external (EXT) reference selection. The ADC internal reference is selected by shorting pins 1–2 on JP2, which corresponds to the silkscreen designators of *HI* or *EXT*. This will be amended in Rev. C of the EVM.

6 Physical Description

This section describes the physical characteristics and PCB layout of the EVM.

6.1 PCB Layout

The EVM is constructed on a 4-layer, 0.062-inch (1.58-mm) thick PCB using FR-4 material. The individual layers are shown in Figure 3 through Figure 6. The layout features a common ground plane; however, similar performance can be had with careful layout using a split ground plane.

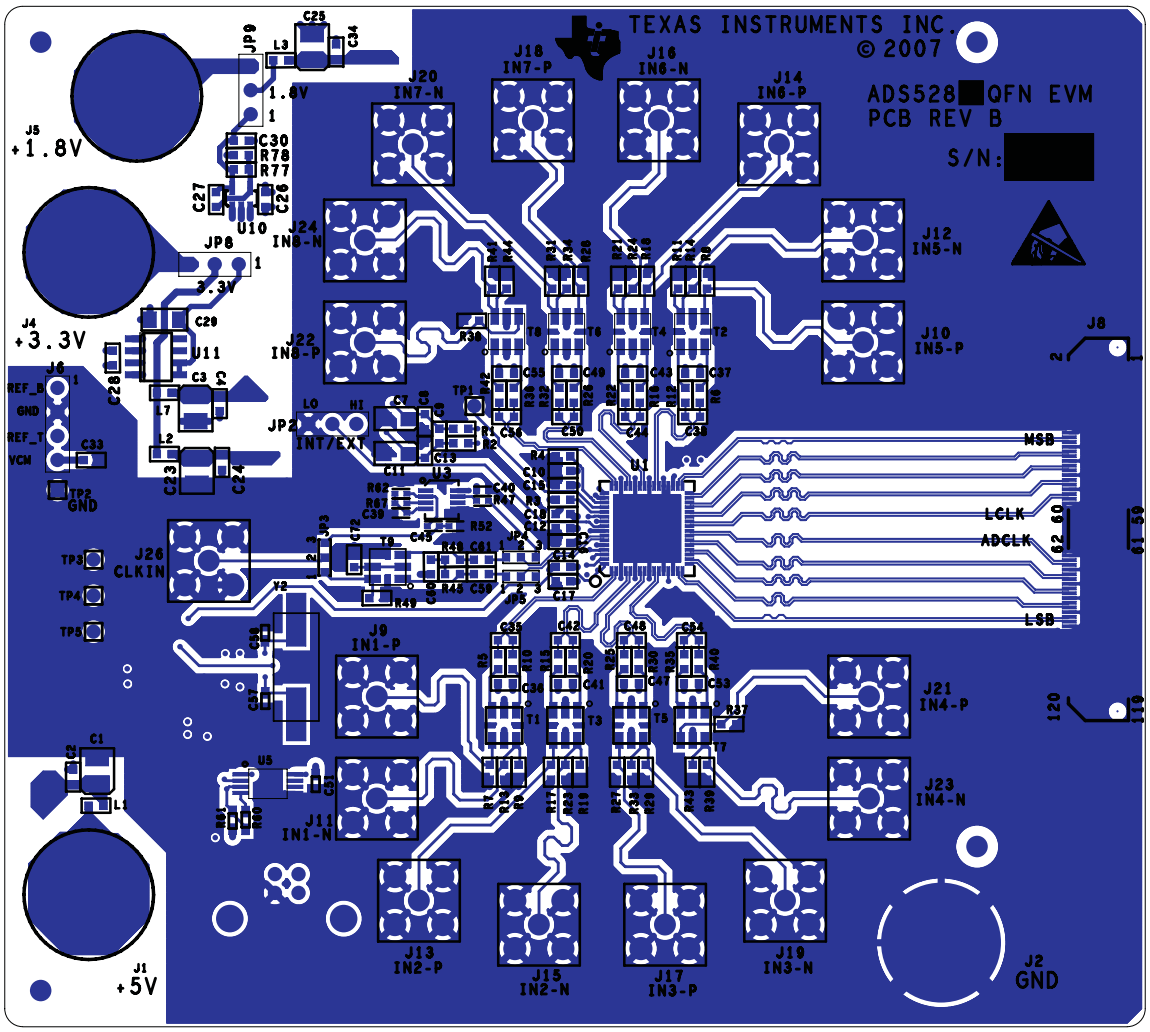

Figure 3. Top Silkscreen

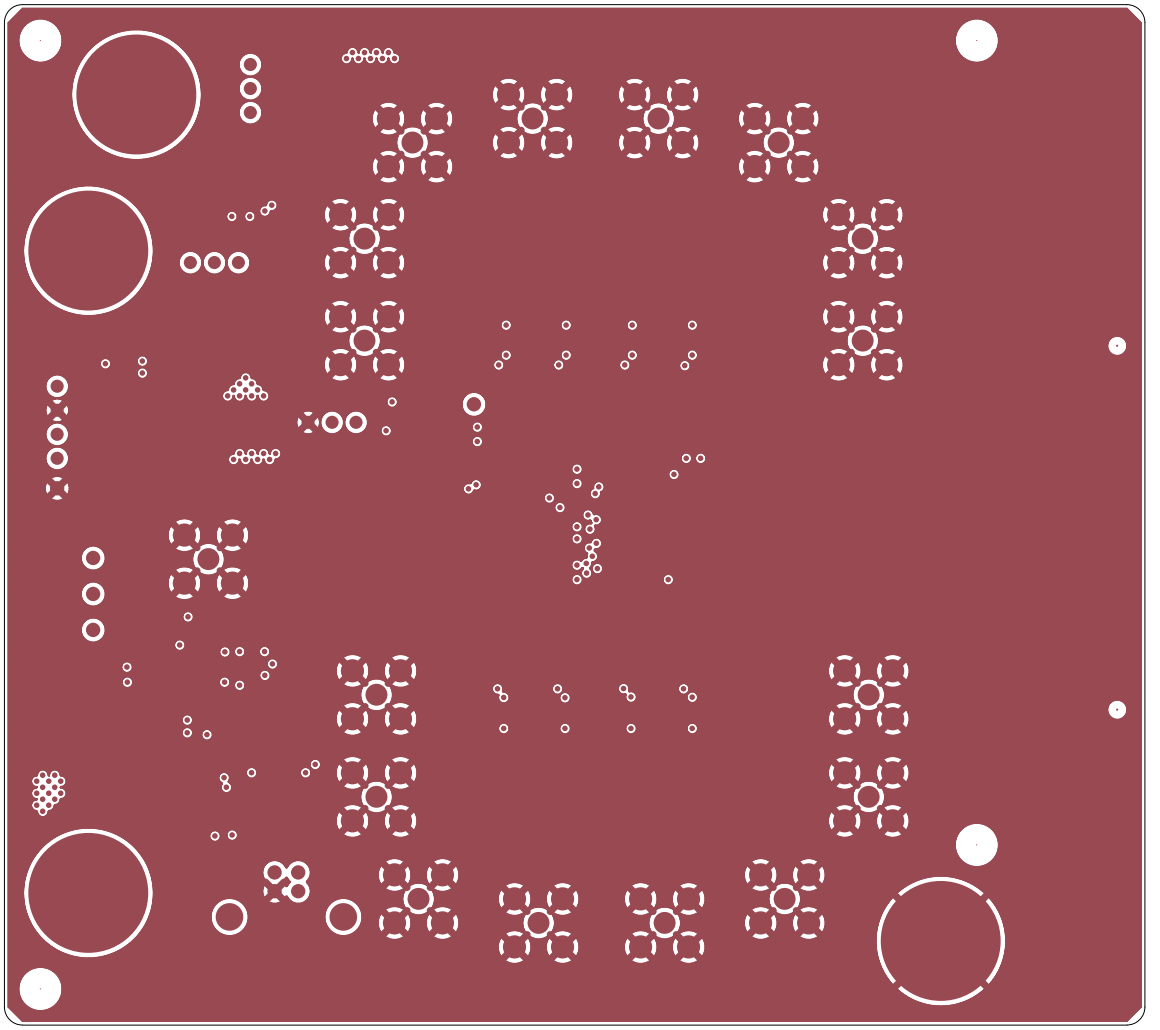

Figure 4. Ground Plane

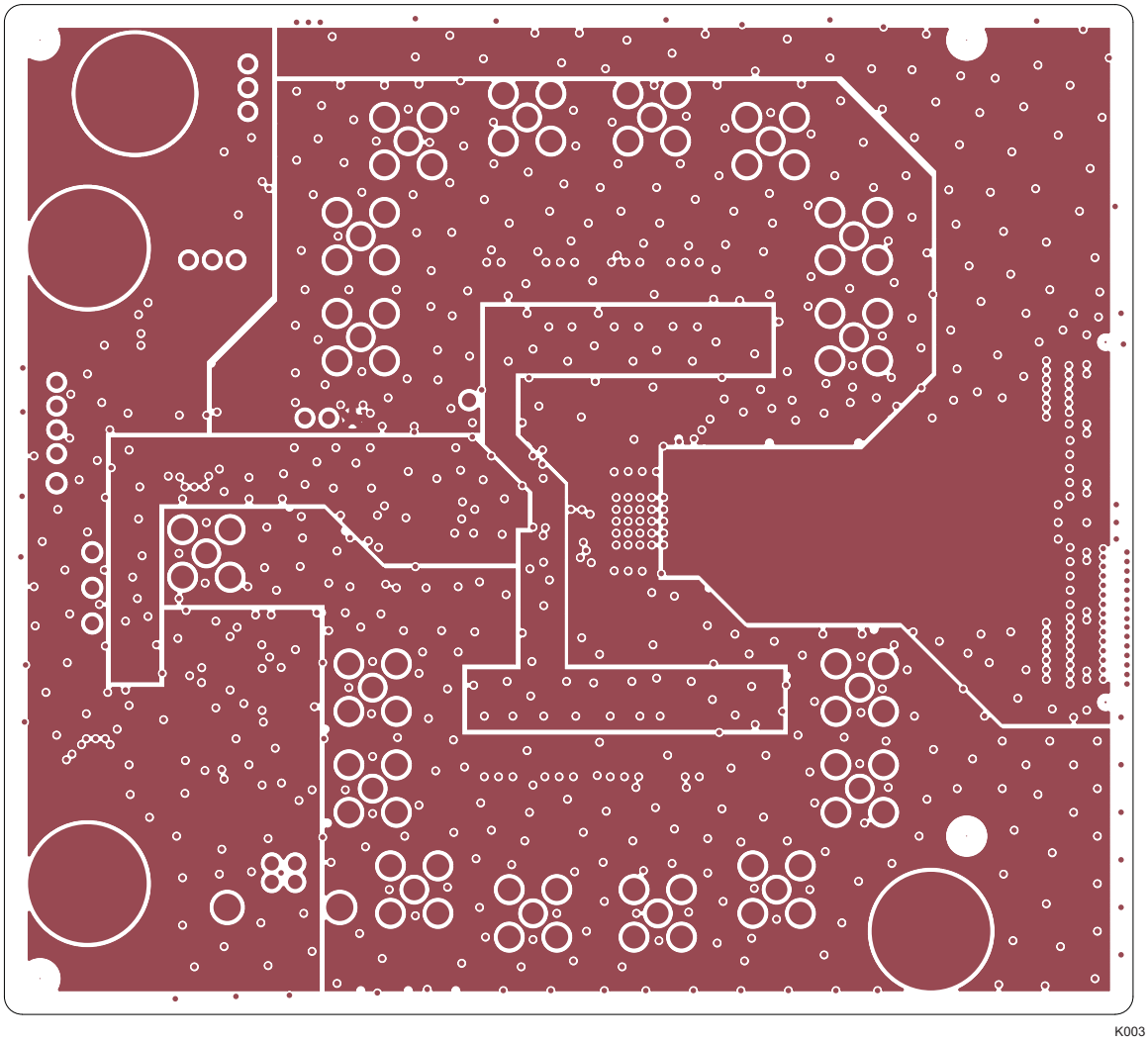

Figure 5. Power Plane

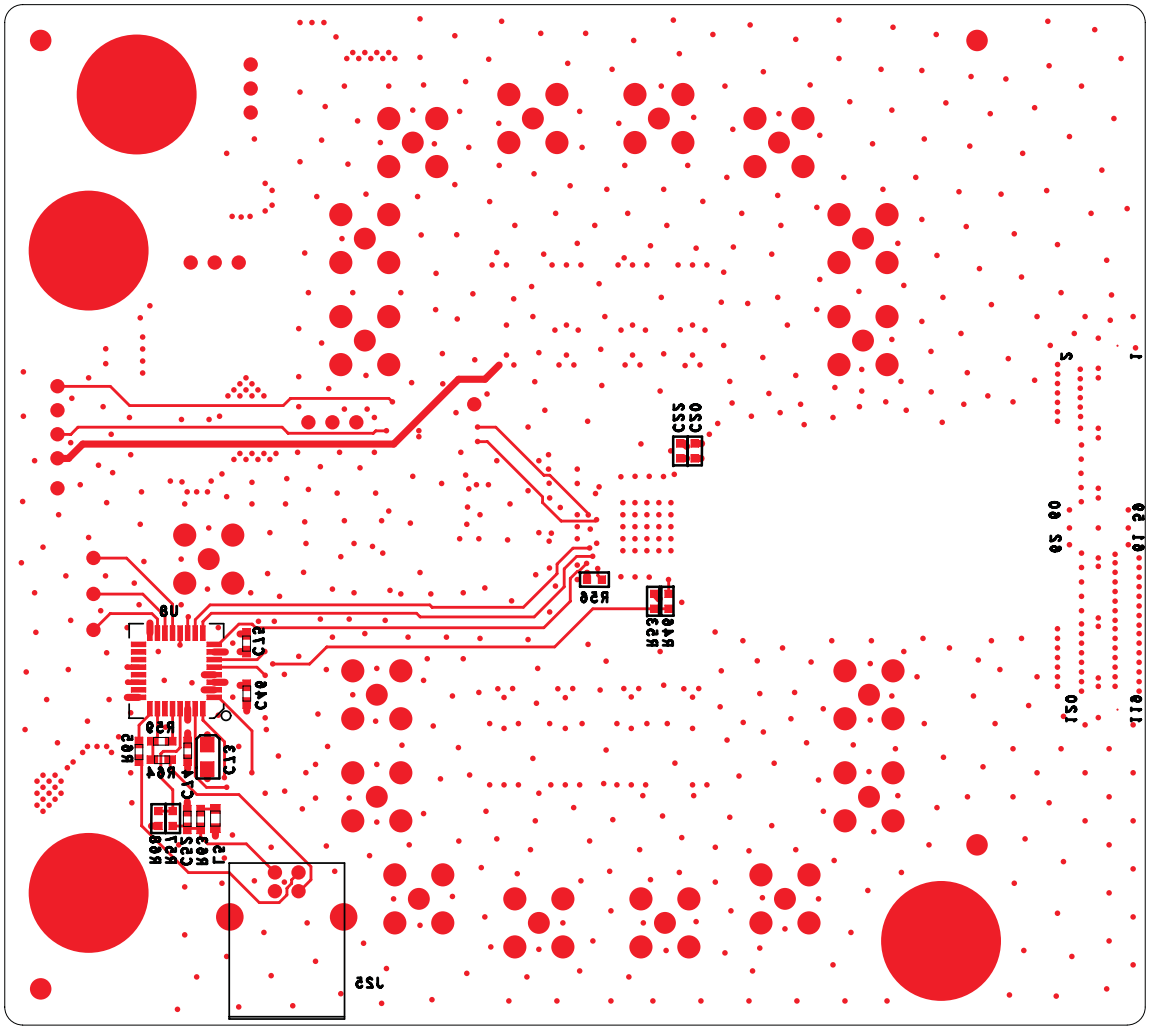

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Figure 6. Bottom Silkscreen

6.2 Bill of Materials

Table 4. Bill of Materials

Reference	Not Installed	Part	Footprint	Part Number	Manufacturer	Tolerance
C1, C3, C23, C25		33 µF	TANT_B	B45196H1336K209	Kemet	10%
C2, C4, C24, C34		1 µF	603	ECJ-1VB0J105K	Panasonic	10%
C7, C11		22 µF	TANT_A	B45196H1226K109	Kemet	10%
C8, C9, C10, C12, C13, C14, C18, C20, C26, C27, C28, C30, C36, C37, C41, C43, C47, C49, C53, C55, C59, C60, C61, C72		0.1 µF	603	ECJ-1VB1C104K	Panasonic	10%
C15, C16, C17, C22		0.01 µF	603	06035C103KAT2A	AVX	10%
C29		10 µF	1206	ECJ-3YB1C106K	Panasonic	10%
C33		2.2 µF	603	ECJ-1VB0J225K	Panasonic	10%
C35, C38, C42, C44, C48, C50, C54, C56		10 pF	603	ECJ-1VC1H100D	Panasonic	0.5 pF
C40, C39, C45		0.1 µF	402	ECJ-0EB1A104K	Panasonic	10%
C46, C51, C74, C75		0.1 µF	SMD_0603	GRM188R71H104KA93D	Murata	10%
C52		0.01 µF	SMD_0603	C0603C103K1RACTU	Kemet	10%
C57, C58		27 pF	SMD_0603	GRM1885C2A270JA01D	Murata	5%
C73		10 µF	TANT_A	TAJA106K016R	AVX	10%
JP2, JP8, JP9		HEADER 3POS .1 CTR				Short pins 1–2 with shunt connectors DigiKey # S9000-ND
		CONN JUMPER SHORTING		S9000-ND	DigiKey	
JP3, JP4, JP5		NO PART	SMD_BRIDGE_0603			Short pins 1–2 using 0-Ω resistors
J1, J4, J5		RED		ST-351A	ALLIED ELECTRONICS	
J2		BLK		ST-351B	ALLIED ELECTRONICS	
J6		HEADER 4	JUMPER4			
J8		QTH-060-02-F-D-A		QTH-040-01-F-D-DP-A	Samtec	
J9, J10, J13, J14, J17, J18, J21, J22, J26		SMA		142-0701-201	Johmson Components	
J11, J12, J15, J16, J19, J20, J23, J24	NOT INSTALLED	SMA		142-0701-201	Johmson Components	
J25		CONN USB TYP B FEM		897-43-004-90-000000	Milmax	

Table 4. Bill of Materials (continued)

Reference	Not Installed	Part	Footprint	Part Number	Manufacturer	Tolerance
L1, L2, L3, L7		68 Ω at 100 MHz	603	MI0603J680R-10	Steward	
L5		1 kΩ at 100 MHZ	SMD_0805	BLM21AG102SN1D	Murata	
R1, R2		2 Ω	603	ERJ-3GEYJ2R0V	Panasonic	5%
R3		0 Ω	603	ERJ-3GEY0R00V	Panasonic	5%
R4		56.2 kΩ	603	ERJ-3EKF5622V	Panasonic	1%
R5, R6, R7, R8, R10, R12, R13, R14, R15, R16, R17, R18, R20, R22, R23, R24, R25, R26, R27, R28, R30, R32, R33, R34, R35, R36, R37, R38, R40, R42, R43, R44, R49		49.9 Ω	603	ERJ-3EKF49R9V	Panasonic	1%
R9, R11, R19, R21, R29, R31, R39, R41		0 Ω	603	ERJ-3GEY0R00V	Panasonic	1%
R45, R48	NOT INSTALLED	121 Ω	603	ERJ-3EKF1210V	Panasonic	1%
R46		10 Ω	603	ERJ-3EKF10R0V	Panasonic	1%
R47, R52		49.9 Ω	402	ERJ-2RKF49R9X	Panasonic	1%
R53, R56		10 kΩ	603	ERJ-3EKF1002V	Panasonic	1%
R57		4.7 kΩ	603	ERJ-3GEYJ472V	Panasonic	5%
R59		1.5 kΩ	SMD_0603	ERJ-3EKF1501V	Panasonic	5%
R60		2.21 kΩ	SMD_0603	ERJ-3EKF2211V	Panasonic	1%
R61		10 kΩ	SMD_0603	ERJ-3GEYJ103V	Panasonic	5%
R62, R67		499 Ω	402	ERJ-2RKF4990X	Panasonic	1%
R63	NOT INSTALLED	0 Ω	SMD_0603	ERJ-3GEY0R00V	Panasonic	5%
R64, R65		26.7 Ω	SMD_0603	ERJ-3EKF26R7V	Panasonic	1%
R68	NOT INSTALLED	10 kΩ	603	ERJ-3EKF1002V	Panasonic	1%
R77		28 kΩ	603	RC0603FR-0728KL	Yageo	1%
R78		56.2 kΩ	603	RC0603FR-0756K2L	Yageo	1%
TP1, TP3, TP4, TP5		T POINT R	TESTPOINT	5002	Keystone	
TP2		T POINT R	TESTPOINT	5001	Keystone	
T1, T2, T3, T4, T5, T6, T7, T8, T9		TC1-1T	XFMR_TC4-1W	TC1-1T	Mini Circuits	
U1		ADS528X_QFN64	QFN64	ADS528X	TI	
U3		MC100EPT21		MC100EPT21DTG	On Semiconductor	

Table 4. Bill of Materials (continued)

Reference	Not Installed	Part	Footprint	Part Number	Manufacturer	Tolerance
U5		93C66B	TSSOP8	93C66B-I/ST	Microchip	
U8		FT245BM	PQFN32	FT245BM	Future Technology Devices	
U10		TPS73201-SOT23	DBV5	TPS73218DBVT	TI	
U11		TPS77533D	SOIC8	TPS77533D	TI	
Y2		6.0000 MHz		ECS-60-32-5PDN-TR	ECS	
MP2		Screw, machine, ph 4-40 × 3/8		PMS 440 0038 PH	Building Fasteners	PCB legs
MP3		Stand-off, hex, .5/4-40THR		1902C	Keystone Electronic	

6.3 PCB Schematics

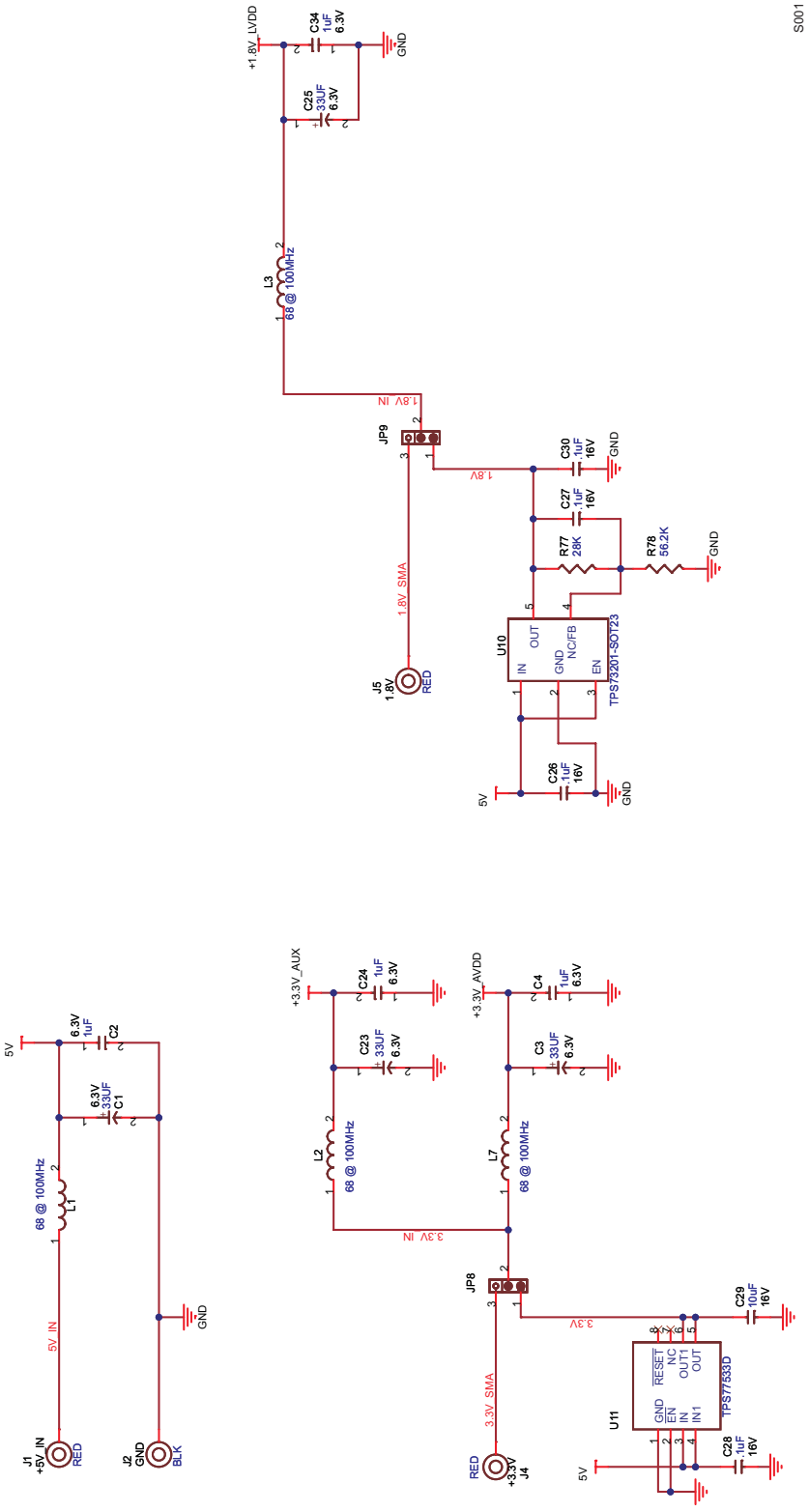

Figure 7. EVM Schematics (Sheet 1 of 5)

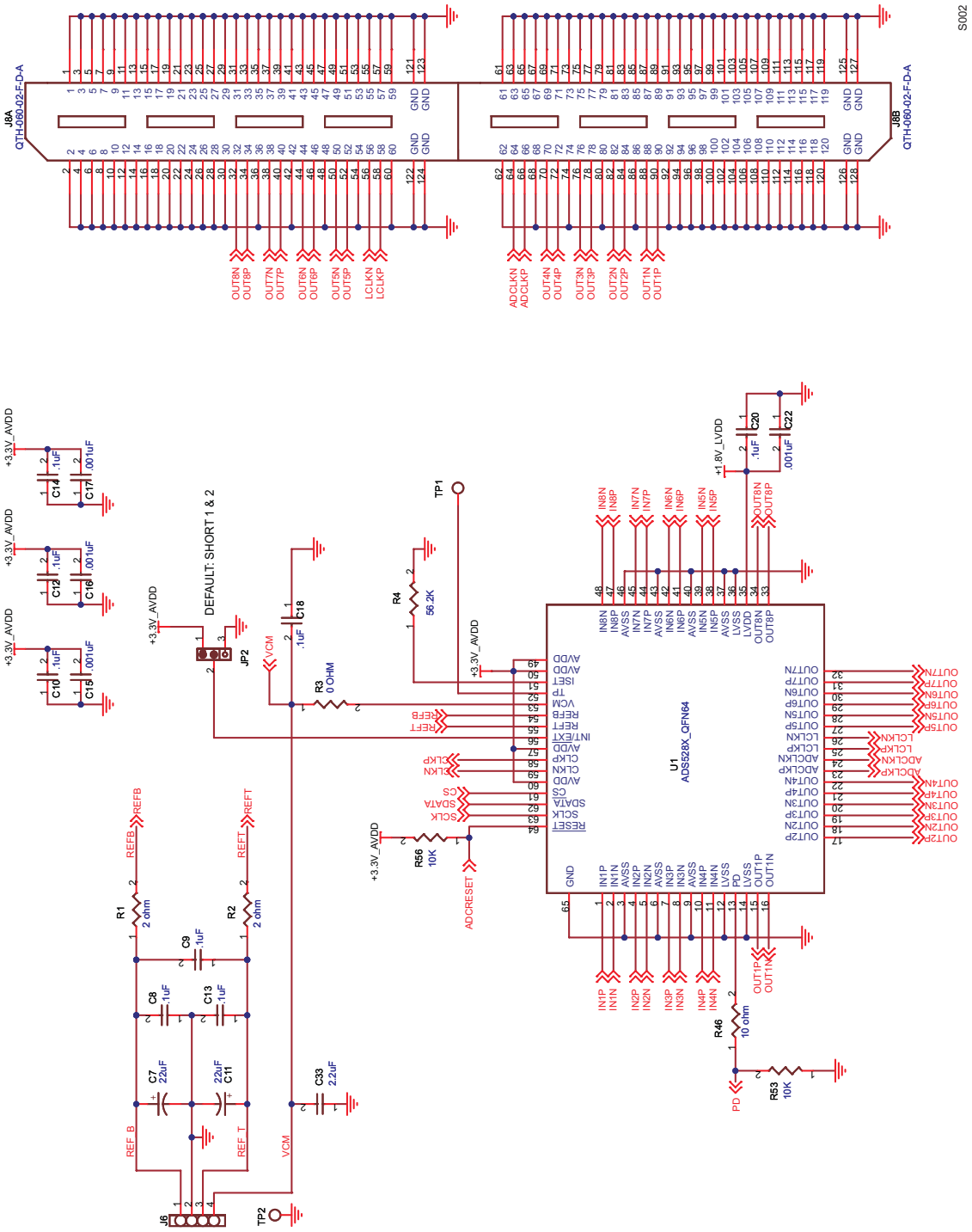

Figure 8. EVM Schematics (Sheet 2 of 5)

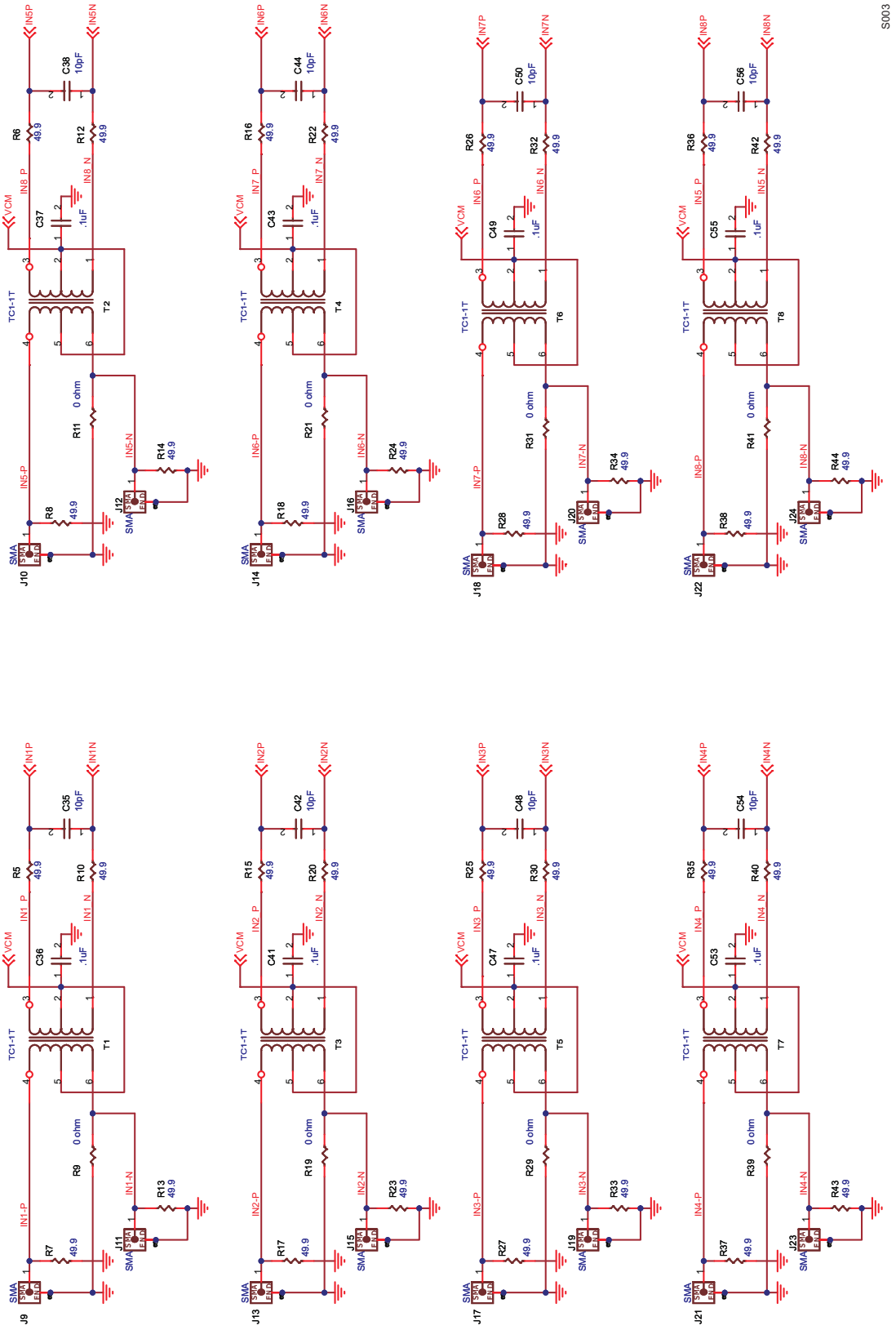

Figure 9. EVM Schematics (Sheet 3 of 5)

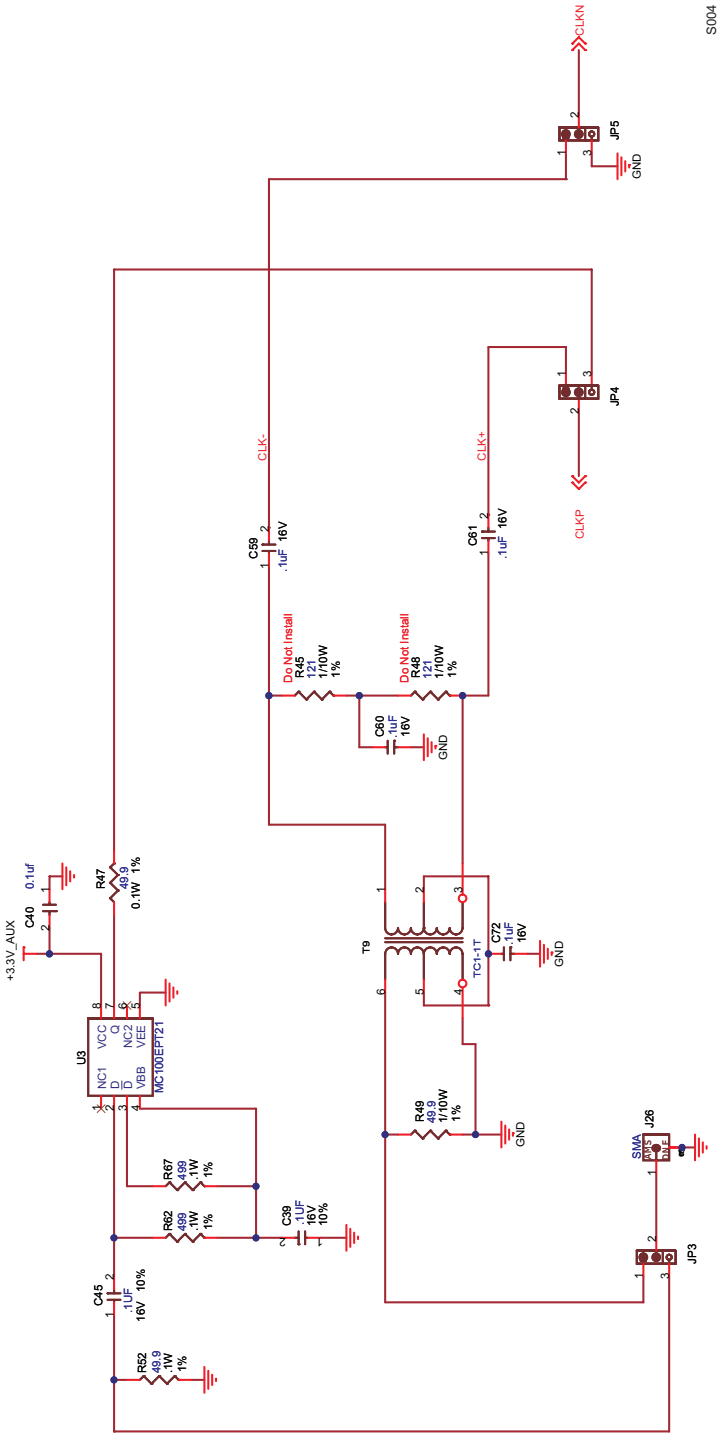

Figure 10. EVM Schematics (Sheet 4 of 5)

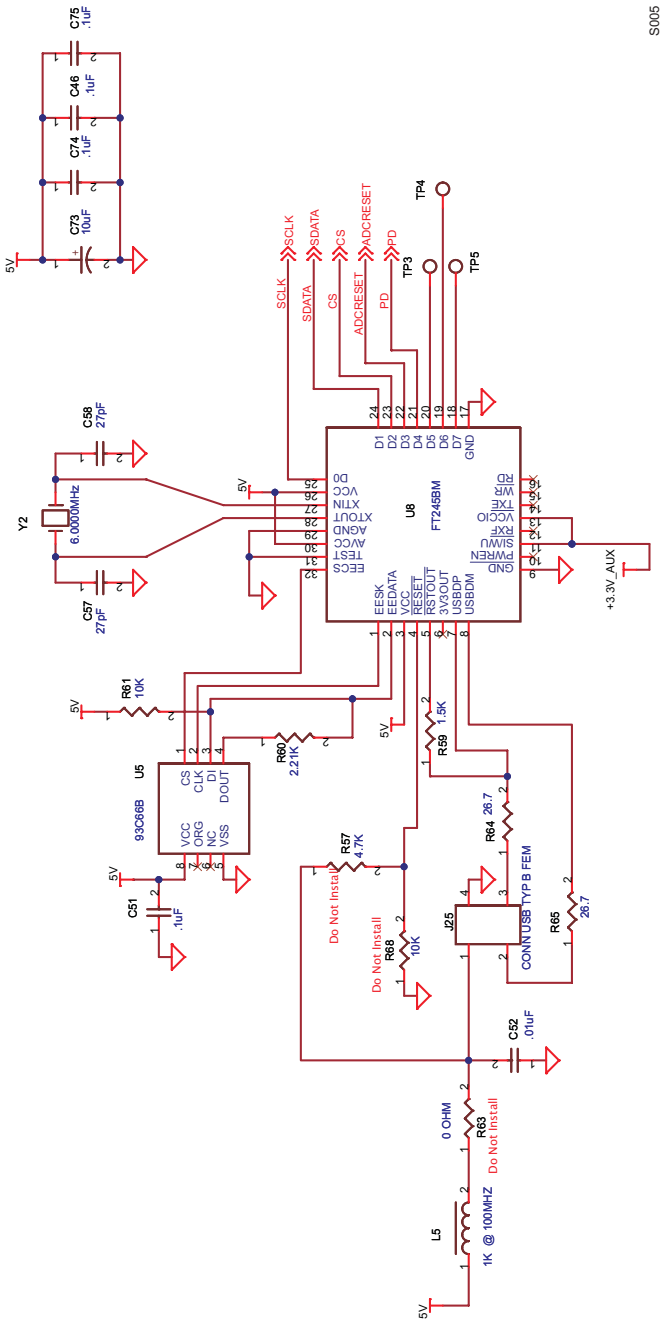

Figure 11. EVM Schematics (Sheet 5 of 5)

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of –3 V to 3.8 V and the output voltage range of –3 V to 3.8 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

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During normal operation, some circuit components may have case temperatures greater than 50°C. The EVM is designed to operate properly with certain components above 25°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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