Errata to TFP410 Datasheet

This document describes errata to the TFP410 and its datasheet (literature number SLDS145).

Revision History

VERSION	DATE	DESCRIPTION
1.0	Initial	DE generator
1.1	1/22/2003	Items 2-4
1.2	5/20/2003	V_{IH}, V_{IL} clarification, CTL3 encoding, pad size update, revision history
A	4/17/2009	Removed pad size information

DE Generator

The DE generator function has a limitation which limits its use in high pixel count formats. The DE_DLY and DE_CNT values are limited by DE_DLY + DE_CNT < 2047.

For resolutions where the timing allows, it may be possible to work around this limitation by using the inactive edge of HSYNC as the starting point for DE_DLY. Appropriate timing allowances may be needed for the vertical count starting location.

Changes in the Document Text

In the “register descriptions” section, under the pictorial for DE_DLY (Page 20), add after the existing sentence: The value must be less than or equal to (2047 - DE_CNT).

In the “register descriptions” section, under the pictorial for DE_CNT (Page 21), add after the existing sentence: The value must be less than or equal to (2047 - DE_DLY)

MSEN Output

The MSEN output description is incorrect in the “Terminal Functions” table. MSEN behavior of the 410 with manual configuration is to output the receiver connected status as a high, receiver not connected as a low.

Changes in the Document Text

From: When I^2C is disabled (ISEL = low), a low level indicates a powered on receiver is detected at the differential outputs. A high level indicates a powered on receiver is not detected. This function is only valid in dc-coupled systems.

To: When I^2C is disabled (ISEL = low), a high level indicates a powered on receiver is detected at the differential outputs. A low level indicates a powered on receiver is not detected. This function is only valid in dc-coupled systems.

Error in Register Capability

Changes in the Document Text

Sheet 17, in the register map for sub-address 0B, change the RW column value

From: RW **To:** R

Error in Default Value

Changes in the Document Text

Sheet 18, Reg sub-address 08 change register default

From: FE **To:** BE

CTL3 Not Encoded in Output

The CTL3 input from the device pin or register value is not encoded into the DVI stream. The current TFP410 is aware of HDCP and encodes the CTL3 signal as 0 in the output. When the device is configured for manual input with pins 6-8 selected as CTL[3:1], pin 6 is not encoded. When the device is configured for I2C operation, bit 3 of the CTL_# MODE register at Sub-Address 0A can be written and read, but the bit is not encoded.

Changes in the Document Text

Sheet 2, change pin 6 label

From: CTL3/A3/DK3 **To:** A3/DK3

Sheet 4, in the Terminal Functions table, change the name of pin 6

From: CTL3/A3/DK3 **To:** A3/DK3

Sheet 4, in the Terminal Functions table, change pin 6 Description

From: When the I^2C bus is disabled (ISEL = low) and the de-skew mode is disabled (DKEN = low), these three inputs become the control inputs, CTL[3:1], which can be used to send additional information across the DVI link during the blanking interval (DE = low). The CTL3 input is reserved for HDCP compliant DVI TXs (TFP510) and the CTL[2:1] inputs are reserved for future use.

To: When the I^2C bus is disabled (ISEL = low) and the de-skew mode is disabled (DKEN = low), pins 7 and 8 become the control inputs, CTL[2:1], which can be used to send additional information across the DVI link during the blanking interval (DE = low). Pin 6 is not used.

Sheet 10, in the first paragraph of the T.M.D.S. pixel data and control signal encoding section, change the sentence

From: These same three channels are also used to transmit HSYNC, VSYNC, and three user definable control signals, CTL[3:1], during the inactive display or blanking interval (DE = Low).

To: These same three channels are also used to transmit HSYNC, VSYNC, and the control signals, CTL[3:1], during the inactive display or blanking interval (DE = Low).

Sheet 10, in note 8, change the second sentence

From: The CTL3 input is reserved for HDCP compliant DVI TXs and the CTL[2:1] inputs are reserved for future use.

To: CTL3 is reserved for HDCP and is always encoded as 0. The CTL[2:1] inputs are reserved for future use.

Sheet 19, register CTL_3_MODE, change definition of bits 3:1 in the diagram

From:

3	2	1
CTL[3:1]		

To:

3	2	1
RSVD	CTL[2:1]	

In the text below the diagram, change the CTL bit definition name

From: CTL[3:1]:This read/write register contains the values of the three CTL[3:1] bits that are output on the DVI port during the blanking interval.

To: CTL[2:1]:This read/write register contains the values of the three CTL[2:1] bits that are output on the DVI port during the blanking interval.

Input Voltage Clarifications

In the DC specification table, V_{IH} and V_{IL} are not clear for signals that are not part of the video input bus.

Changes in the Document Text

Sheet 7, in the dc specifications table, change the V_{IH} and V_{IL} specifications to contain the following information:

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	Data, DE, VSYNC, HSYNC and IDCK+/–	$V_{REF} = DV_{DD}$	$0.7 \times V_{DD}$			V
			$0.5\ V \le V_{REF} \le 0.95\ V$	$V_{REF} + 0.2$			
		Other inputs		$0.7 \times V_{DD}$			
V_{IL}	Low-level input voltage	Data, DE, VSYNC, HSYNC and IDCK+/–	$V_{REF} = DV_{DD}$			$0.3 \times V_{DD}$	V
			$0.5\ V \le V_{REF} \le 0.95\ V$			$V_{REF} – 0.2$	
		Other inputs				$0.3 \times V_{DD}$	

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