Power Supply Design Seminar

GaN-Optimized Transition-Mode Power Factor Correction

TEXAS INSTRUMENTS

Reproduced from
2024 Texas Instruments Power Supply Design Seminar
SEM2600
Topic 1
Brent McDonald
Literature Number: SLUP418

This topic introduces a gallium nitride (GaN)-optimized power factor correction (PFC) topology and control methodology for high-performance, high-density and cost-effective PFC. Employing a new zero voltage detection (ZVD) circuit and algorithm enhances zero voltage switching (ZVS) and total harmonic distortion (THD) over the entire line cycle and load range. A 5-kW prototype with a power density of 120 W/in^3 and a THD <6% serves as a proof of concept for demonstrating optimal control methods for startup, transient response and AC dropout.

Introduction

A PFC circuit intentionally shapes the input current to be in phase with the instantaneous line voltage and minimizes the total apparent power consumed. Using data centers as an example (see **Figure 1**), you can see why a small, reliable and efficient power supply is so important. The typical data center server rack example shown in **Figure 1** has seven power-supply units (PSUs), which each have their own PFC.

Each PFC must supply several kilowatts of power to meet the functional demands of the individual servers. At a data center level, a typical installation needs support for about 50 MW. The data center industry estimates that there about 8,000 data centers worldwide. With numbers like that, it is really easy to see why a small, reliable and efficient power supply is so important.

In this paper, I'll discuss some exciting new PFC technologies that are very relevant to these kinds of systems.

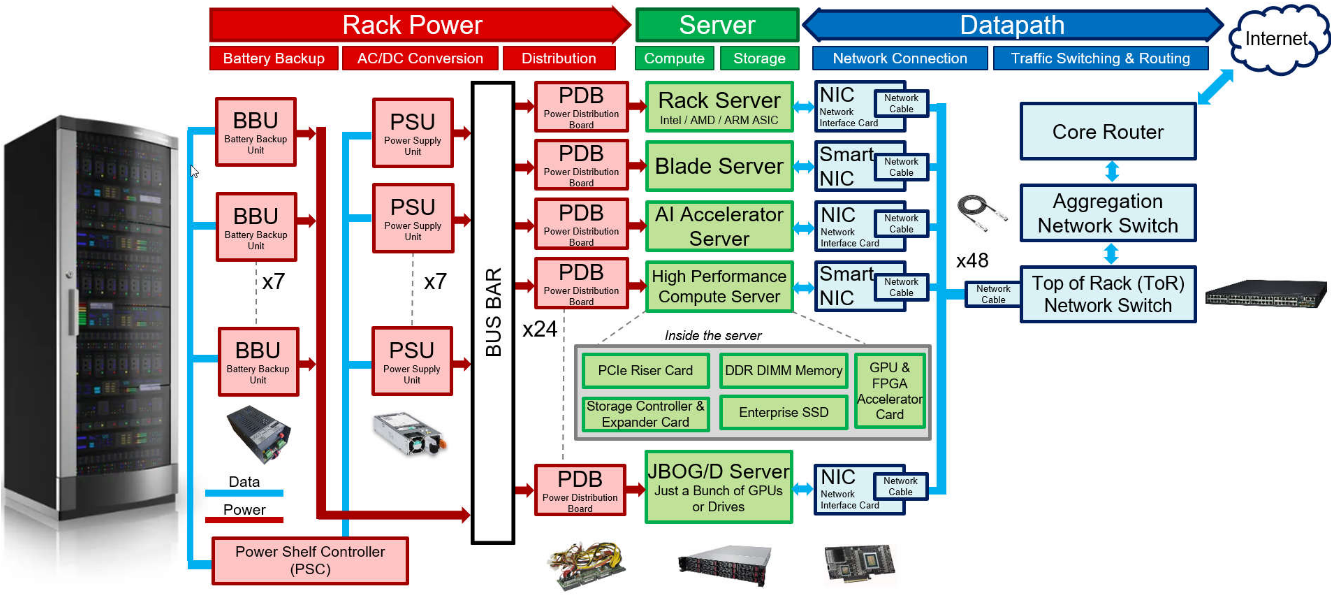


Figure 1. Typical enterprise data center system.

Boost Converter Topology Review

Let's begin with a brief review of some of the core technology inside a typical PFC.

The boost converter is the workhorse of the PFC. **Figure 2** through **Figure 5** are schematics of a boost converter during each of the four operational modes that occur during an AC line cycle. **Figure 2** and **Figure 4** show how the converter works during the positive half cycle. **Figure 2** and **Figure 3** show the operation of the control field-effect transistor (FET). This FET is in charge of what is classically known as the "D" conduction time. **Figure 4** and **Figure 5** show operation during the rectification period – in this case using a diode, but you could also use a synchronous rectifier (SR). The colored lines show the current flow paths during each conduction period. For example, during the positive half-cycle control-FET interval, current flows through the input inductor, FET and AC source. From **Figure 2**, you can see that current flow during the positive half cycle tends to always be out of the positive terminal of the input source. During the negative half cycle, current flow tends to always be out of the negative terminal of the input source.

Figure 6 through **Figure 9** show the same information as **Figure 2** through **Figure 5**, except this time I've replaced the topology with a totem-pole PFC boost converter. At its heart it is still a boost converter; however, some additional switches facilitate automatic switching between the various operating modes.

One FET leg is designated the high-frequency leg, consisting of switches S_1 and S_2. For this leg, switching losses, conduction losses and reverse recovery are extremely important device characteristics. The other leg consists of switches S_3 and S_4. This is the so-called low-frequency leg, which in some cases can even be replaced with diodes. The function of the low-frequency leg is simply to switch at the AC line frequency to complete the conduction path for the boost converter.

Totem-pole PFC is the workhorse of any application requiring the highest efficiency and the smallest form factor. In recent years, the proliferation of wide band-gap devices such as GaN and silicon carbide (SiC) have made this topology more and more relevant. The control complexity required to raise the efficiency while keeping the size small is really the driving force behind this paper.

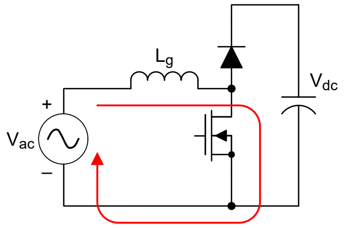
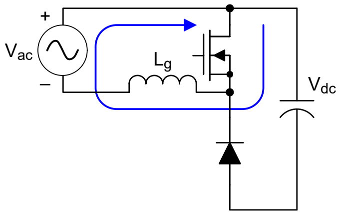
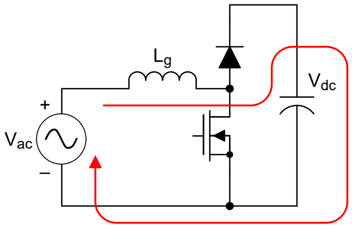
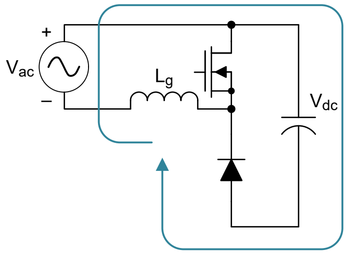
	Positive Half Cycle	Negative Half Cycle
Control FET	 ***Figure 2.*** *Control FET conduction, positive ½.*	 ***Figure 3.*** *Control FET conduction, negative ½.*
Rectifier	 ***Figure 4.*** *Rectifier conduction, positive ½.*	 ***Figure 5.*** *Rectifier conduction, negative ½.*

Table 1. *PFC boost converter topologies.*

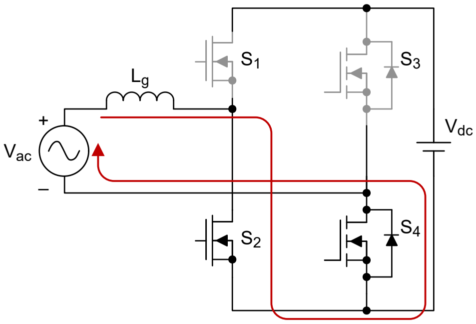
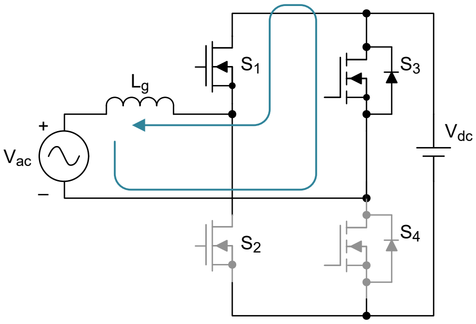
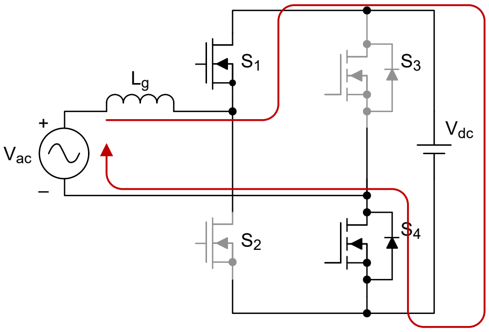
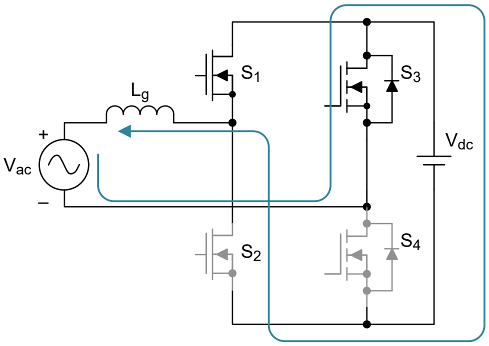
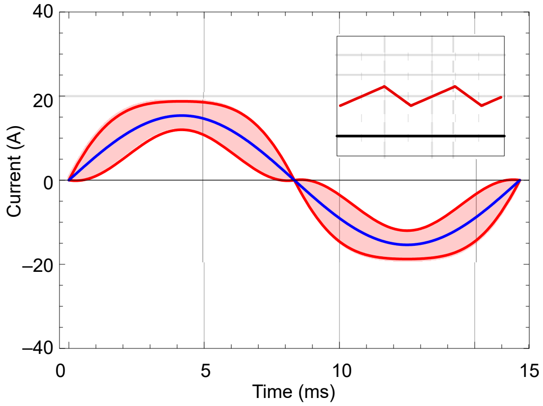
	Positive Half Cycle	Negative Half Cycle
Control FET	 ***Figure 6.*** *Control FET conduction, positive ½.*	 ***Figure 7.*** *Control FET conduction, negative ½.*
Rectifier	 ***Figure 8.*** *Rectifier conduction, positive ½.*	 ***Figure 9.*** *Rectifier conduction, negative.*

Table 2. *Totem-pole PFC boost converter topologies*

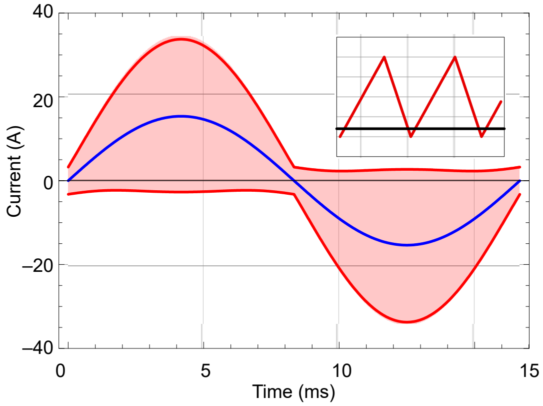
Conduction Modes

As already mentioned, the totem-pole PFC converter is essentially a boost converter. As such, you can manage the inductor current through design and control to achieve different ripple current behaviors. **Figure 10** through **Figure 12** show the ripple current envelope of the inductor current in red, along with the cycle average inductor current in blue.



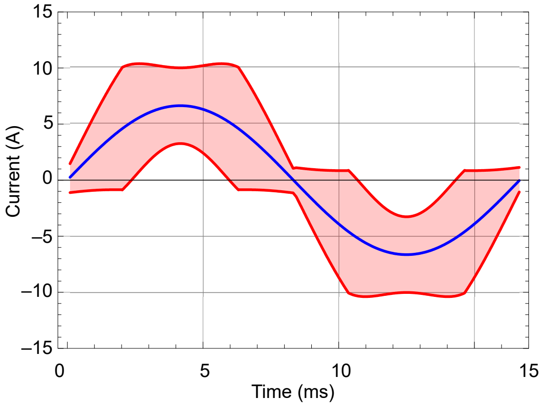
- Hard switching and reverse recovery.
- Lower conductive losses.
- Small ripple current.
- Simple control.

Figure 10. *Continuous conduction mode (CCM).*



- ZVS.
- Higher conduction losses.
- Large ripple.
- Complex control.

Figure 11. *Transition conductive mode (TCM).*



- Combination of CCM and TCM.
- Attempts to get the benefit of each.
- Complex control.

Figure 12. *Multimode.*

The first and most common mode is CCM, in which the inductor is always positive for the positive half cycle and negative for the negative half cycle. CCM's biggest disadvantages come from hard switching. Plus, with the need to reverse-recover the body diode of the FET, it's not really possible to use silicon metal-oxide semiconductor FETs for this mode. Instead, you'd have to use a wide band-gap device such as SiC or GaN, given their low to zero reverse recovery.

Aside from that, CCM has several advantages, including small ripple; lower root-mean-square (RMS) currents resulting in reduced conduction losses; and a well-known, relatively straightforward way to control it.

The second mode is TCM, in which the inductor current ripple is sized such that the current goes to zero every switching cycle (in reality, it pokes below zero a little bit). Because the control always has to wait for the current to hit zero before initiating the next switching cycle, TCM operates with variable frequency. One of the biggest draws to using TCM is the fact that it can achieve ZVS across all input and load conditions. The higher ripple current also results in larger RMS currents, and therefore more conduction losses. In order to get a high power factor and ZVS over all operating conditions, the required control can become quite complex.

Multimode PFC attempts to take the benefits from both CCM and TCM and capture them in a single converter. It uses a smaller inductor, but not so small that the ripple is as high as in full TCM. As a result, the RMS currents are lower; therefore the conduction losses are lower as well. Multimode can capture ZVS under certain line and load conditions, but not everywhere. The net result is that you end up with conduction loss levels in between the CCM and TCM cases.

One downside of multimode is that the control becomes very complex. Essentially, you have to manage the control for ZVS and the power factor and make sure that the mode transition from CCM to TCM is sufficiently smooth so as not to cause large distortion in the power factor.

Returning to the data center rack server application, the biggest goal is to maximize efficiency in a small space. The best topology is one that can switch fast enough to benefit from the size reduction that comes from raising the switching frequency. This makes the TCM and multimode options the ones to look at more closely.

Figure 13 through **Figure 16** compare the FET losses in a GaN switch for a multimode design and a TCM design. The design is running with 230 V_{AC}, 60-Hz input and a 400-V output. **Figure 13** and **Figure 15** show the multimode design performance. **Figure 13** shows how the frequency will change on a cycle-by-cycle basis over one-half a line cycle. The different colored lines show the different load conditions. For multimode, the frequency is clamped on the low end to 60 kHz. Whenever the converter is running with a 60-kHz frequency, it is in CCM. Any frequency above 60 kHz is TCM. The frequency variation is between about 60 kHz and 250 kHz. **Figure 15** shows the turnon losses, turnoff losses and conduction losses. The multimode case has significant turnon and conduction losses.

Figure 14 and **Figure 16** show similar data for the TCM design. In this case, the frequency variation is between 75 kHz and 750 kHz. That's substantially wider than the multimode case. If you look at the losses, you can see that the $R_{DS(on)}$-related losses in **Figure 16** are higher for the TCM case, but the turnon loss is much lower. The net result is that the TCM case has significantly lower FET-related losses.

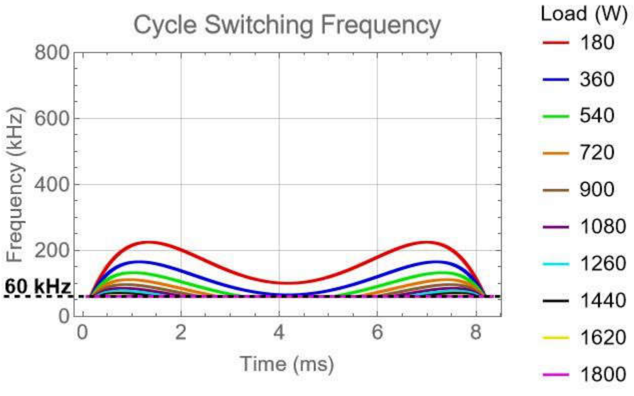


Figure 13. CCM/TCM multimode frequency range.

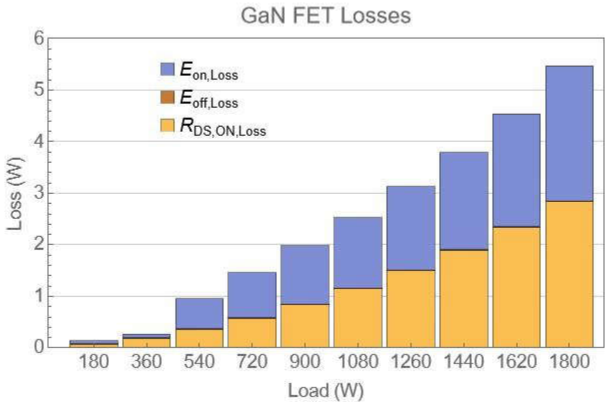


Figure 14. CCM/TCM ultimode FET loss.

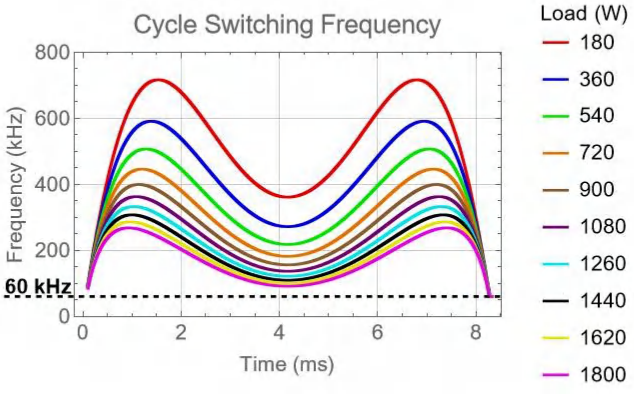


Figure 15. TCM frequency range.

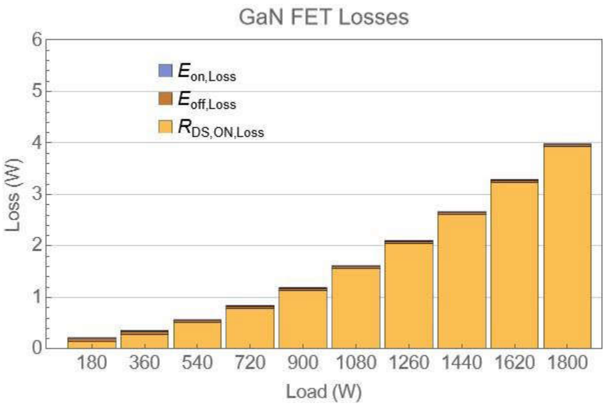


Figure 16. *TCM FET loss.*

Table 3 summarizes how several of the primary system concerns stack up. The TCM design is going to have a physically smaller inductor given the lower inductance requirement. The larger ripple current in the TCM will require a larger electromagnetic interference (EMI) filter. The lower FET loss in the TCM topology makes for a great fit in a data center power-conversion system requiring high density and high efficiency.

Topology	Multimode CCM and TCM	TCM
Inductor	150 µH	25 µH
f_S range	60 kHz-250 kHz	75 kHz-750 kHz
FET loss	High	**Low**
Inductor volume	Big	**Small**
EMI filter size	**Small**	Big

Table 3. *Conduction-mode impact on FET losses.*

Control Methods and Constraints

Capturing the potential efficiency benefits of TCM operation requires a suitable control methodology; unfortunately, this has historically been difficult to achieve. To better understand the issue, take a closer look at what the control actually needs to do. **Figure 17** is a simplified schematic of the TCM converter. I've added in the GaN FET C_{oss}, since you must account for these parasitic components in order to get ZVS.

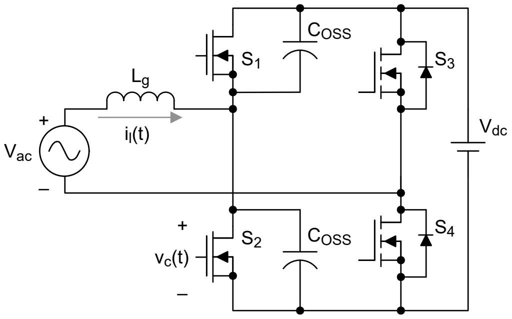


Figure 17. *Simplified totem-pole PFC with relevant parasitics.*

Figure 18 shows a ZVS-equivalent circuit that includes the circuit elements relevant during the dead times.

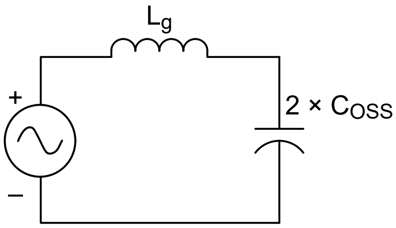


Figure 18. *ZVS equivalent circuit.*

Equation 1 through **Equation 3** are the applicable differential equations:

$$i_l(t) = 2 \times C_{oss} \times \frac{dv_c(t)}{dt} \tag{1}$$

$$v_{ac}(t) - v_c(t) = L_g \frac{di_l(t)}{dt} \tag{2}$$

$$Z_0 = \sqrt{\frac{L_g}{2 \times C_{oss}}} \tag{3}$$

It is possible to simplify the control for this converter down to two fundamental requirements:

- It must achieve ZVS at all operating points.
- It must target a THD of 0.

These requirements mean that S_1 achieves ZVS if $V_C(t) = V_{OUT}$ before turnon and S_2 achieves ZVS if $V_C(t) = 0$ before turnon.

You can achieve the second objective if you average the current in the inductor over one switching cycle and force that average to be equal to a current value that looks like the AC input voltage is supplying power to a resistor. The power consumed by this equivalent resistor is the same as the power consumed by the output. Table 4 defines this concept mathematically.

AC line voltage	$v_{ac}(t) = \sqrt{2} \times v_{ac,rms} \times \sin(\omega \times t + \varphi)$
Cycle average inductor current	$\left\langle I_{L_g}(t) \right\rangle_{T_S} = \frac{v_{ac}(t)}{R_e}$
PFC-equivalent resistance	$R_e = \frac{v_{ac,rms}^2}{P_{out}}$
$\left\langle I_{L_g}(t) \right\rangle_{T_S}$ – denotes the current in L_g averaged over each switching cycle	

Table 4. Mathematical THD description.

All that remains is for the microcontroller to solve for the timing parameters such that these two objectives are true for all input and output conditions. As you will see in the subsequent sections, this is not a trivial task.

Timing Definitions

Let's talk briefly about what timing parameters the microcontroller needs to manage. I've replicated the system schematic and added some key waveforms in Figure 19 and Figure 20.

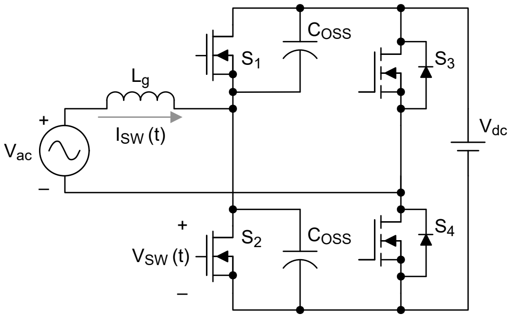


Figure 19. Simplified TCM converter.

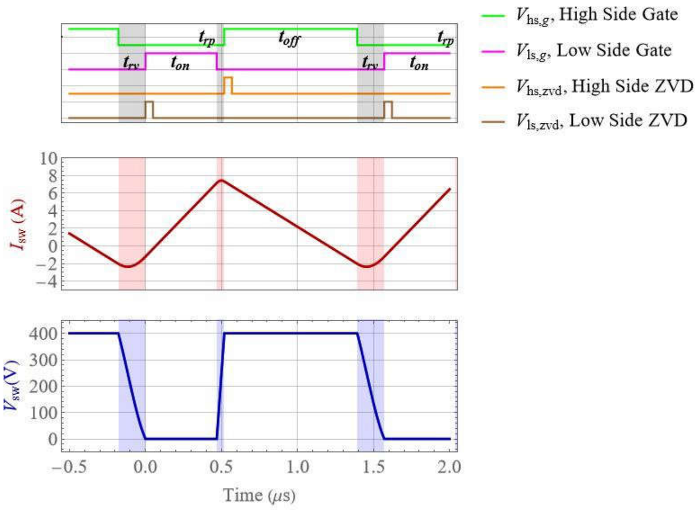


Figure 20. TCM converter key waveforms and timing.

On the top of Figure 20 are the gate-drive signals for S_1 and S_2. Right below is the current in L_g in red and the voltage at the drain source connection of S_1/S_2 in blue. There are four timing parameters that are important; these timing parameters are defined relative to the roles that the FETs play in the circuit. During the positive one-half cycle, S_2 is the control FET and S_1 is the synchronous rectifier. During the negative one-half cycle, the roles of each FET are swapped.

With these definitions, t_{ON} becomes the on-time of the control FET, with t_{OFF} the on-time of the synchronous rectifier. t_{RP} is the dead time between the control FET turnoff and the synchronous rectifier turnon. The "p" in t_{RP} denotes the fact that this dead time occurs at the peak of the inductor current. t_{RV} is the dead time between the synchronous rectifier turnoff and the control FET turnon. The "v" in t_{RV} denotes the fact that this dead time occurs at the valley of the inductor current.

In the most general sense, the microcontroller needs to calculate these four timing parameters every switching cycle such that it is possible to achieve the dual objectives of ZVS for both FETs and unity power factor.

Constant On-Time

Let's start out with the simplest control method out there for transition-mode control. **Equation 4** shows the current in L_g averaged over each switching cycle. Notice that if t_{ON} is a constant, the cycle average input current $\langle I_{L_g}(t)\rangle_{T_s}$ is always proportional to $V_{ac}(t)$.

$$\langle I_{L_g}(t)\rangle_{T_s} = \frac{V_{ac}(t)}{2\ L_g} t_{ON} \tag{4}$$

This is constant on-time control. This control works by simply using a constant on-time for the control FET for a given power level. The on-time is held constant over the entire input voltage range. Some kind of zero current sensor is used to signal the converter to turn on when the inductor current has reached 0 A.

Figure 21 through **Figure 26** show the operating waveforms during constant on-time operation. **Figure 21** through **Figure 25** show the AC line voltage and horizontal markers for V_{out} and one-half V_{out}. **Figure 22** through **Figure 26** are zoomed in to show the switching cycle activity of the inductor current and switch-node voltage. It also shows the AC input, V_{OUT} and one-half V_{OUT}. Three different points in the line cycle are illustrated. The first shows how constant on-time performs when the input voltage is very low. The second shows operation slightly below one-half V_{OUT} and the third shows operation above one-half V_{out}.

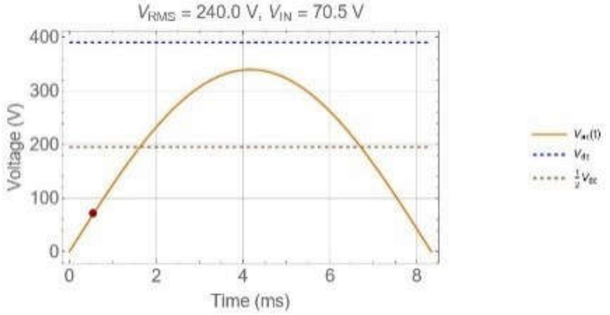


Figure 21. *COT, $V_{IN} << 1/2\ V_{OUT}$, AC line timing.*

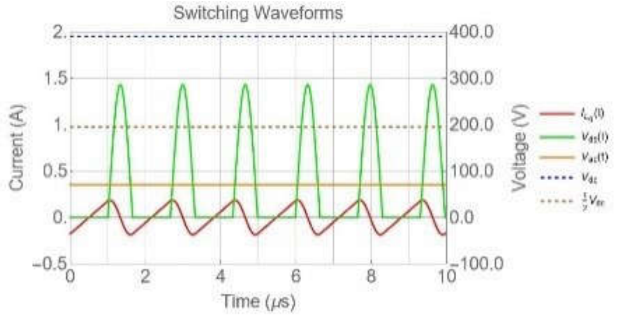


Figure 22. *COT, $V_{IN} << 1/2\ V_{OUT}$, waveforms.*

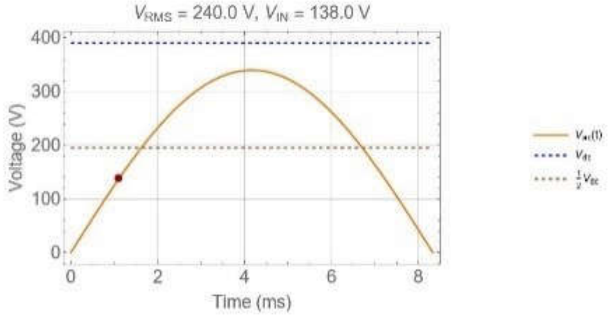


Figure 23. *COT, $V_{IN} < 1/2\ V_{OUT}$, AC line timing.*

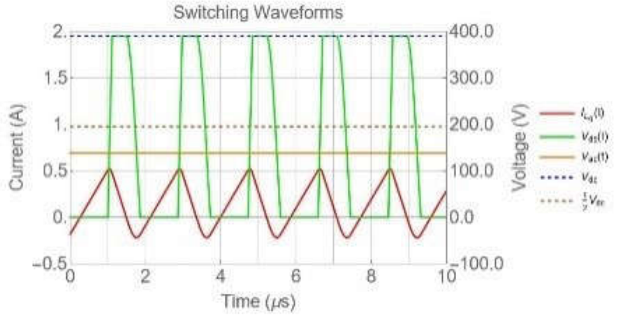


Figure 24. *COT, $V_{IN} < 1/2\ V_{OUT}$, waveforms.*

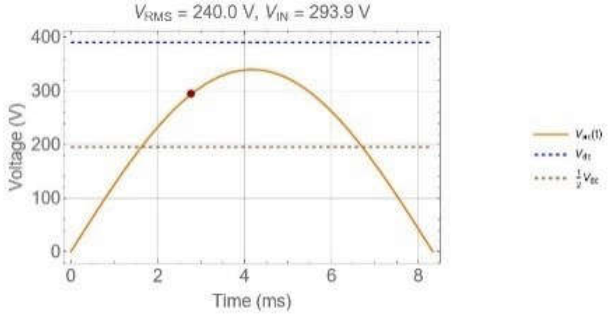


Figure 25. *COT, $V_{IN} > 1/2\ V_{OUT}$, AC line timing.*

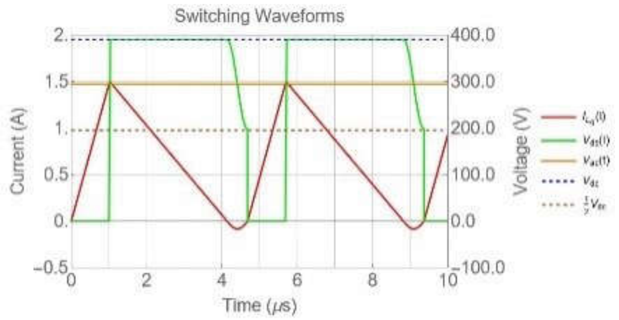


Figure 26. *COT, V_{IN} > 1/2 V_{OUT}, waveforms.*

A few observations about **Figure 21** through **Figure 26**:

- It is very clear that the system is running with constant on-time and consistently operating on the discontinuous conduction mode (DCM) and CCM boundary.
- There is a large variation in switching frequency.
- You lose ZVS when $V_{IN} > ½ V_{OUT}$.
- The inductor current goes negative every switching cycle.
- There is no power delivery near the zero crossings.

The problems described by the third, fourth and fifth bullet points are a result of constant on-time being too crude of an approximation, since it does not account for the negative current generated every switching cycle.

In following sections, you'll see how it is possible to resolve these issues.

ZCD

There is a method that, at least in theory, will solve both the loss of ZVS and the harmonic distortion at zero crossings. It requires a precise zero current detection (ZCD) algorithm and a reliable algorithm that can determine the correct timing. **Figure 27** illustrates this converter.

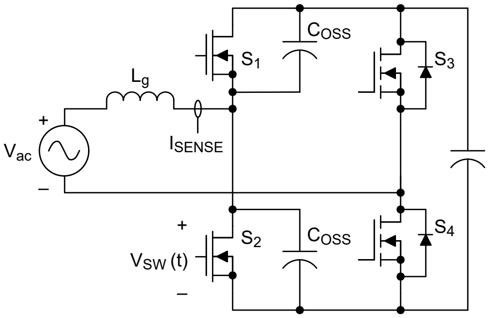


Figure 27. *ZCD schematic.*

Figure 28 through **Figure 36** show the converter waveforms at three different operating points. **Figure 28**, **Figure 31** and **Figure 34** show the AC input voltage, V_{out} and one-half V_{out}. **Figure 29**, **Figure 30**, **Figure 32**, **Figure 33**, **Figure 35** and **Figure 36** show the switch-node voltage $V_C(t)$ and the inductor current $I_L(t)$. I've shaded each of the timing intervals.

Figure 28 through **Figure 30** show the operation when V_{in} is less than one-half V_{out}. You can see in this region that the synchronous rectifier always turns off when the inductor current is exactly equal to zero. This is similar to the constant on-time case. However, when the input goes above one-half V_{out}, the synchronous rectifier must stay on longer. The longer synchronous rectifier time builds up some negative current to ensure that there is enough energy to transition the switch node without hard switching, as shown in **Figure 31** through **Figure 33**.

Another observation is the constant delivery of energy to the load, as shown in **Figure 34** through **Figure 36**. You can see that there is never a time where there isn't enough inductor current to both resonant-transition the switch node all the way to V_{out} and send some current to the output. The converter is no longer operating with constant on-time. In fact, in this control method, all four timing parameters are variable.

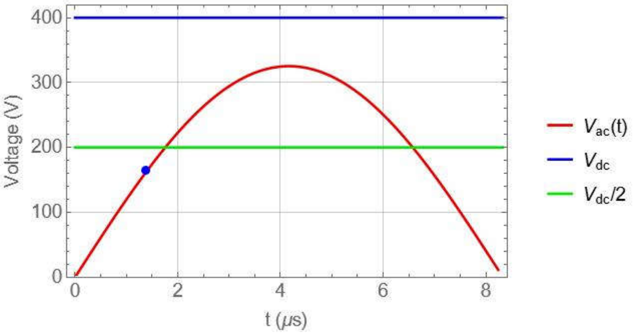


Figure 28. *V_{IN}<1/2 V_{OUT}, ZCD AC line cycle location.*

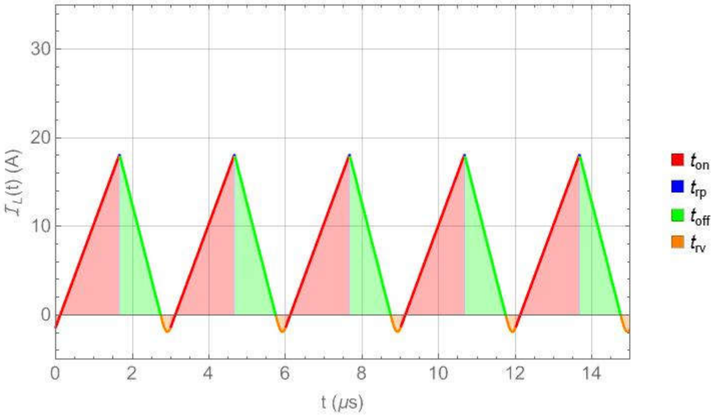


Figure 29. *V_{IN}<1/2 V_{OUT}, ZCD inductor current.*

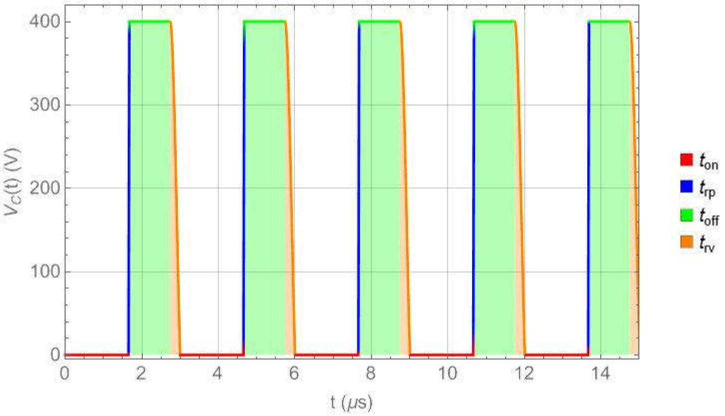


Figure 30. *V_{IN}<1/2 V_{OUT}, ZCD FET V_{DS}.*

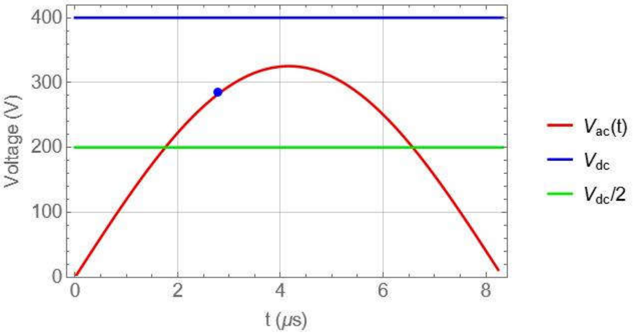


Figure 31. *V_{IN}>1/2 V_{OUT}, ZCD AC line cycle location.*

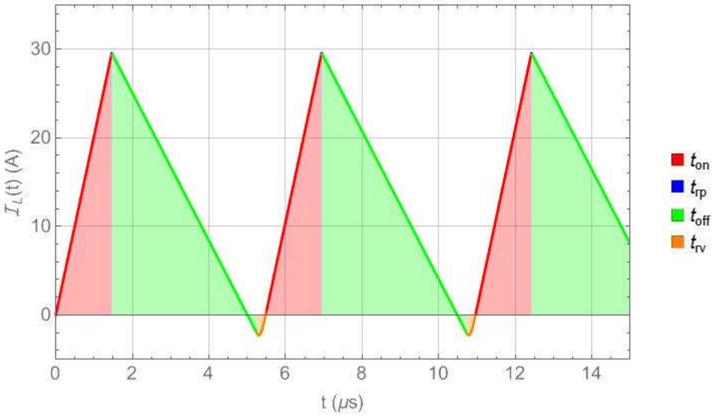


Figure 32. *V_{IN}>1/2 V_{OUT}, ZCD inductor current.*

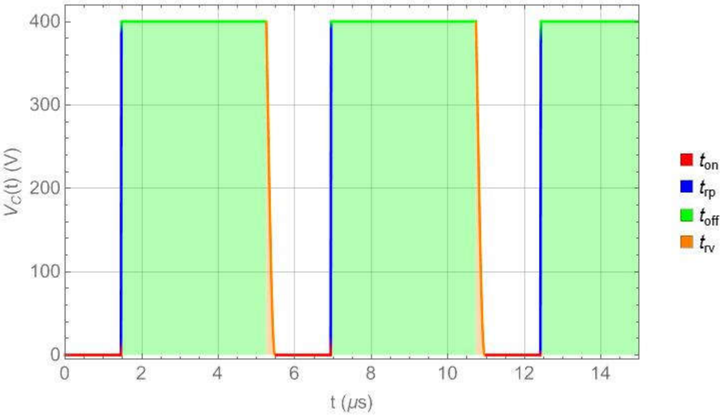


Figure 33. *V_{IN}>1/2 V_{OUT}, ZCD FET V_{DS}.*

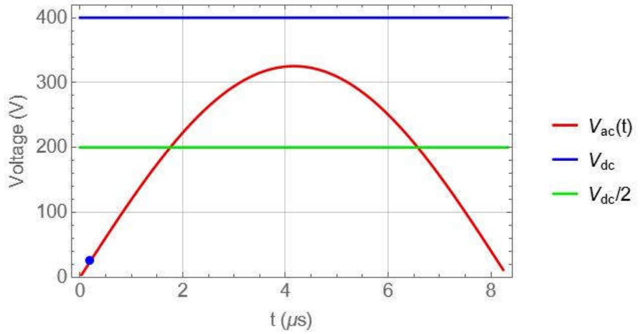


Figure 34. *$V_{IN}<<1/2\ V_{OUT}$, ZCD AC line cycle location.*

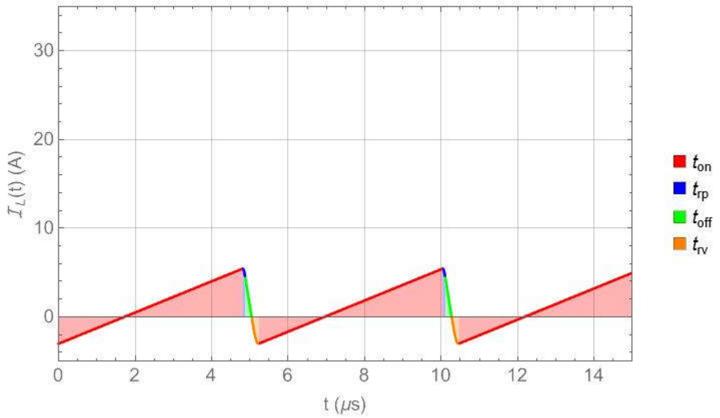


Figure 35. *$V_{IN}<<1/2\ V_{OUT}$, ZCD inductor current.*

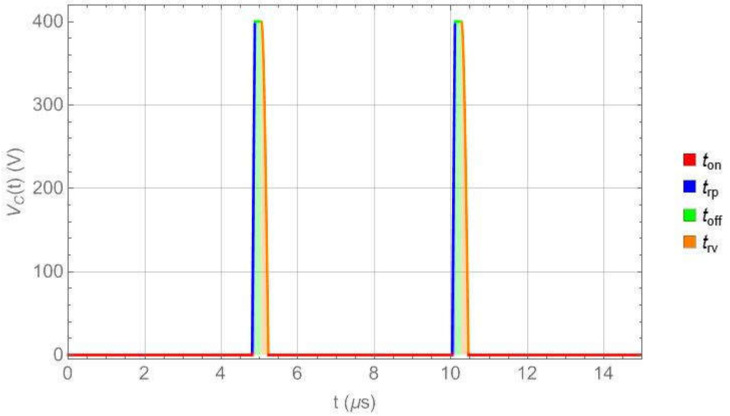


Figure 36. *$V_{IN}<<1/2\ V_{OUT}$, ZCD FET V_{DS}.*

Figure 37 through **Figure 41** show how each of the four timing parameters (t_{ON}, t_{OFF}, t_{RP}, t_{RV}) from **Figure 19** and **Figure 20** vary across a line cycle. In addition to these timing parameters, I've also included a plot of the AC input voltage, cycle-by-cycle switching frequency, average inductor current and ripple current envelope.

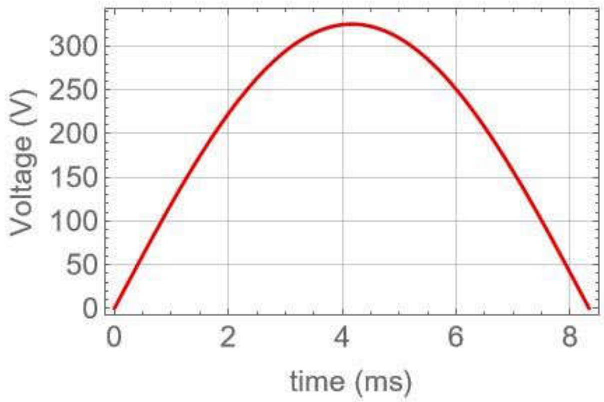


Figure 37. *ZCD control parameters: V_{IN}.*

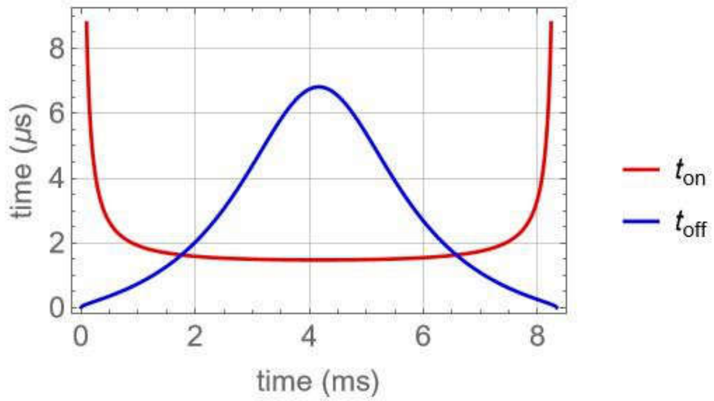


Figure 38. *ZCD control parameters: f_S.*

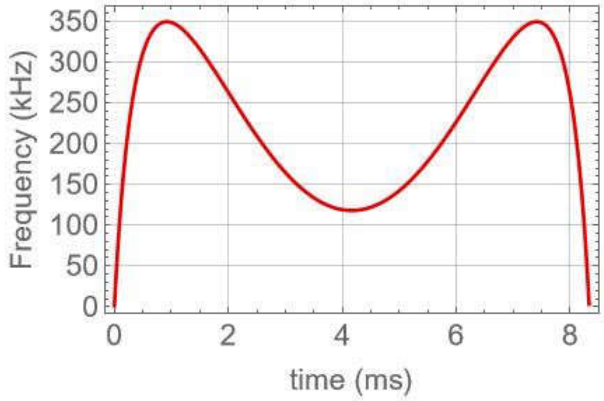


Figure 39. *ZCD control parameters: t_{ON}, t_{OFF}.*

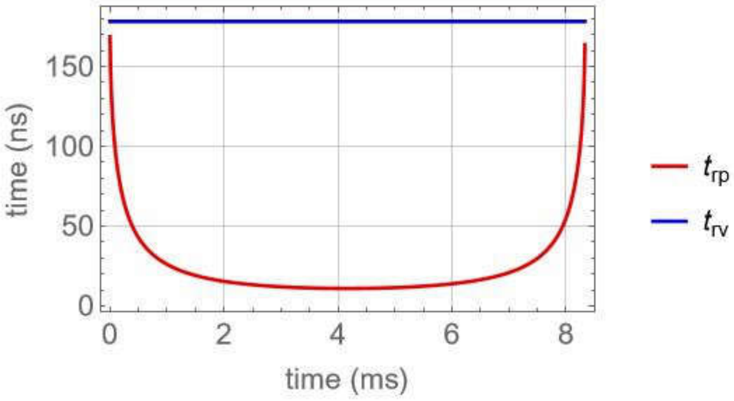


Figure 40. ZCD control parameters: dead times.

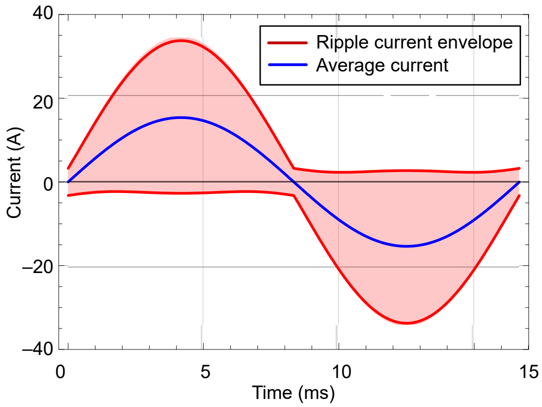


Figure 41. ZCD control current envelope.

From the simulation results in **Figure 28** through **Figure 36**, it is obvious that ZVS is everywhere. The average current in **Figure 41** clearly shows a good power factor. Based on the earlier discussion of constant on-time control, I think the on-time behavior makes some sense. It is approximately constant for a pretty wide input voltage range, but it becomes longer at the zero crossings in order to solve that zero-crossing distortion issue.

There are some problems, however. First and foremost, it is not possible to solve this system explicitly for the four timing variables (t_{ON}, t_{OFF}, t_{RP}, t_{RV}). The control equations are just too complicated to solve in real time. Therefore, you must resort to some approximation that will inevitably compromise ZVS, THD, or both.

There is one more problem with this approach: How do you design and implement an effective zero current detector?

Figure 42 through **Figure 45** illustrate the timing issue. Figure 39 is a schematic of the system. **Figure 43** shows the ideal timings for ZVS and ideal power factor on the left. ZCD-based control requires a precise measurement of when the current in the synchronous rectifier hits zero. The problem is that there are delays in the measurement, detection and pulse generation that will essentially result in the synchronous rectifier being held on longer than it should. This isn't a problem for ZVS, but it is a problem for the power factor and will result in additional losses from higher RMS currents. Adding a high-bandwidth, low-latency sensor and additional computations in the microcontroller will compensate for the errors introduced in the current wave shape. The plots in **Figure 44** and **Figure 45** illustrate this error.

The bottom line is that the current-sensing issue takes already complex control and makes it more complex.

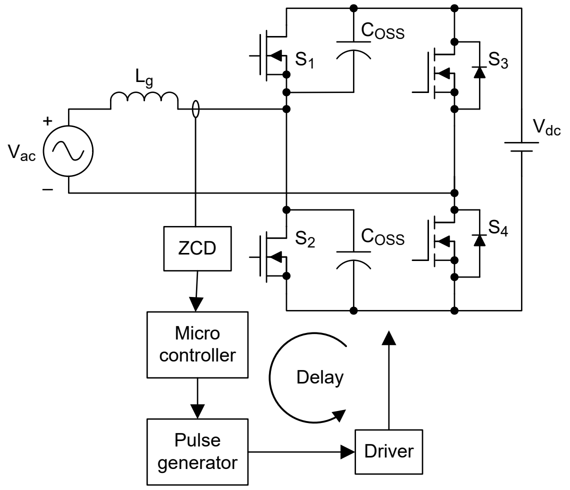


Figure 42. ZCD timing challenge.

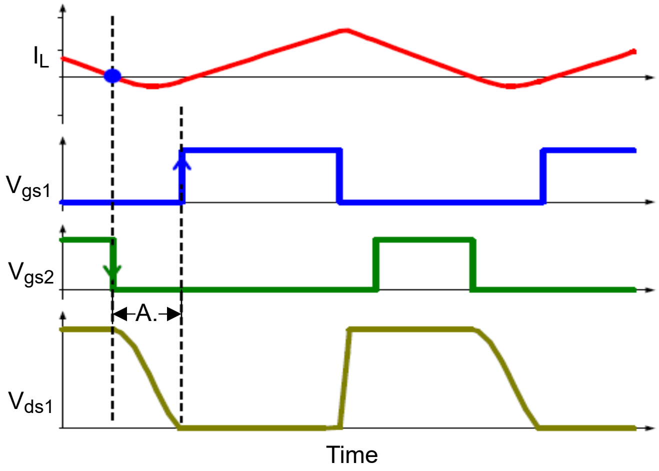


Figure 43. *Ideal ZCD timing waveforms.*

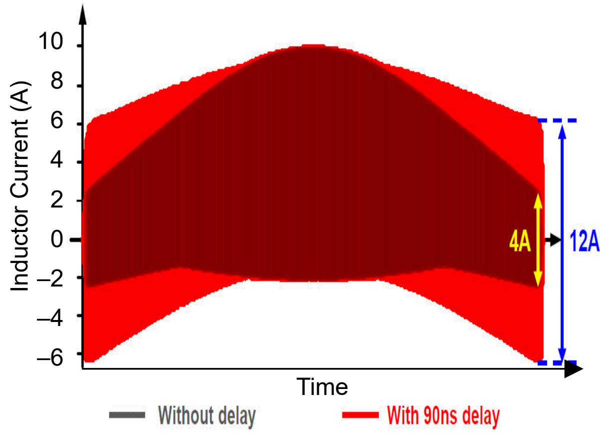


Figure 44. *ZCD ripple current distortion caused by timing errors.*

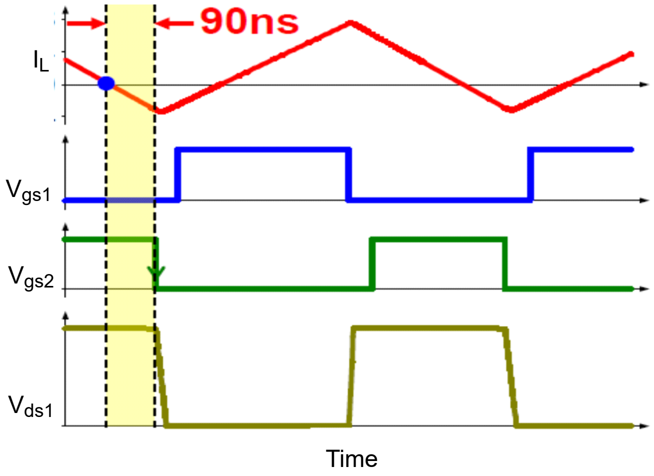


Figure 45. *Actual ZCD timing waveforms.*

ZVD

The first step in the path toward simplifying the control is to take least one of the four timing parameters and make it a constant. It's not really an option to do this with the on- and off-time, as you've seen from the simulation, but perhaps it's possible to do something with the dead time. Looking at the resonant valley dead time, you will notice that it's quite complex and nonintuitive. What about forcing this dead time to be equal to a constant – essentially setting the dead time to a value that it is equal to at the end points of the ZCD control profile? This happens to be equivalent to one-fourth of a resonant period, as expressed by **Equation 5**:

$$\frac{1}{4} \times f_r = \left(\frac{1}{4} \times \frac{1}{2\pi \times \sqrt{L_g \times 2 \times C_{OSS}}} \right) \qquad (5)$$

For more information, see **Figure 46**.

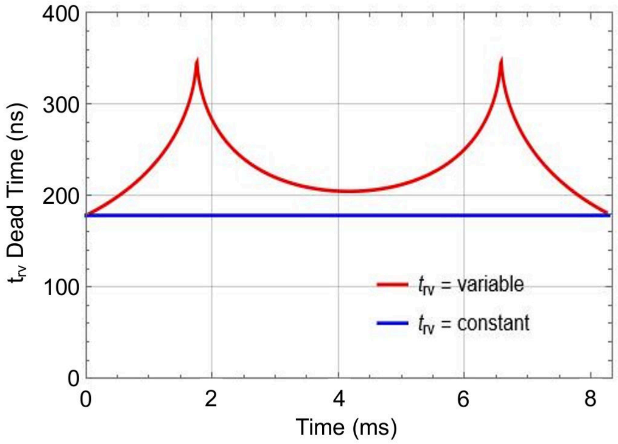


Figure 46. *t_{RV} timing simplification.*

Looking at the performance of the system with this simplification in **Figure 47** through **Figure 50**, you can see that the frequency variation in the original ZCD control and simplified control are very similar. In addition, the ripple current envelopes are also similar. Both are achieving a theoretical power factor of 1. This simplification really makes a lot of sense, since it simplifies the algorithm without really compromising anything on performance.

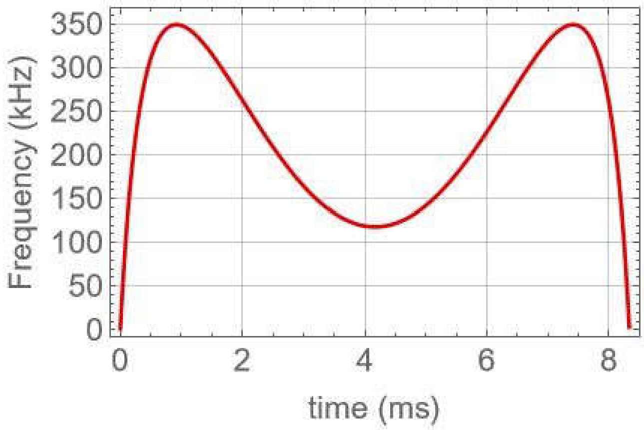


Figure 47. *Constant t_{RV}, frequency variation.*

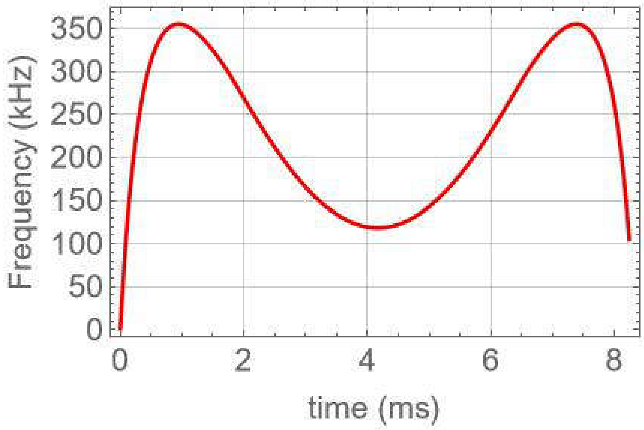


Figure 48. *Variable t_{RV}, frequency variation.*

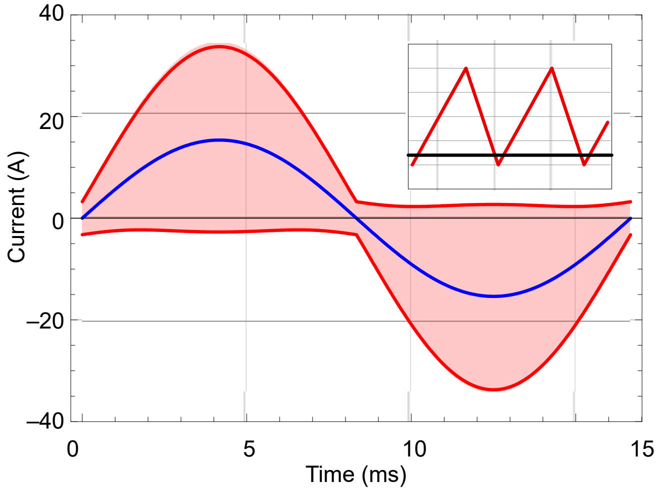


Figure 49. *Constant t_{RV}, ripple current envelope.*

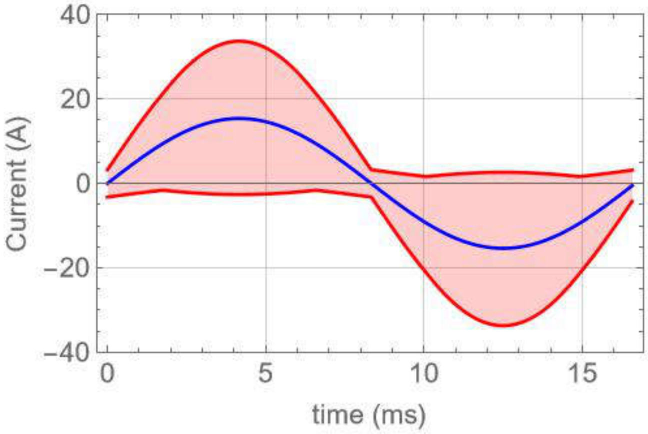


Figure 50. *Variable t_{RV}, ripple current envelope.*

Figure 51 through **Figure 59** show how the waveforms behave on a cycle-by-cycle basis with this new control method. The only differences between these figures and **Figure 28** through **Figure 36** are that t_{RV} is constant, and the t_{ON}, t_{OFF} and t_{RP} control times are recalculated to account for the constant t_{RV} dead time. The waveforms look pretty reasonable. There is ZVS every switching cycle. And as you saw from **Figure 47** through **Figure 50**, the power factor is excellent.

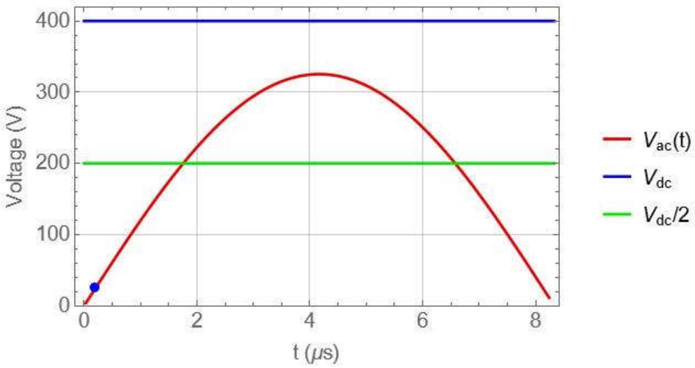


Figure 51. *V_{IN}<<1/2 V_{OUT}, ZVD AC line cycle location.*

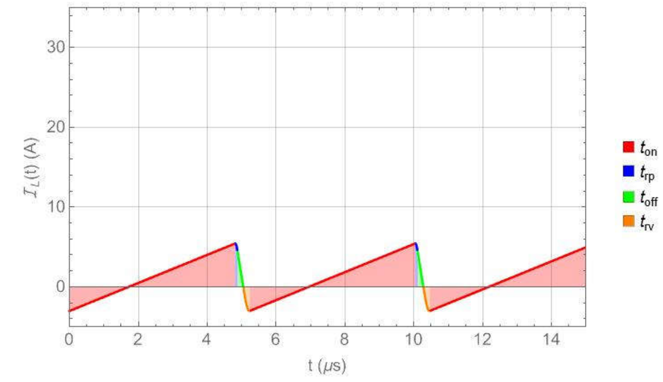


Figure 52. *V_{IN}<<1/2 V_{OUT}, ZVD inductor current.*

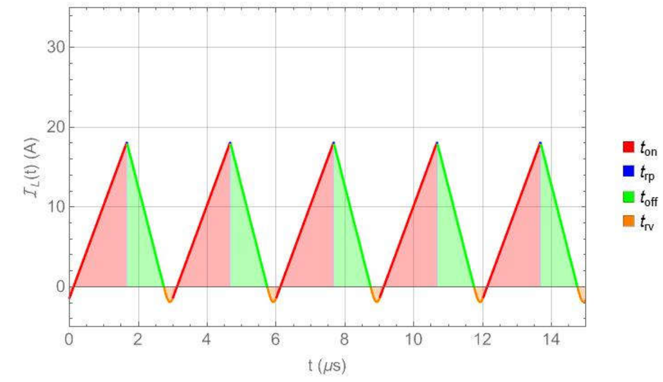


Figure 55. *V_{IN} < 1/2 V_{OUT}, ZVD inductor current.*

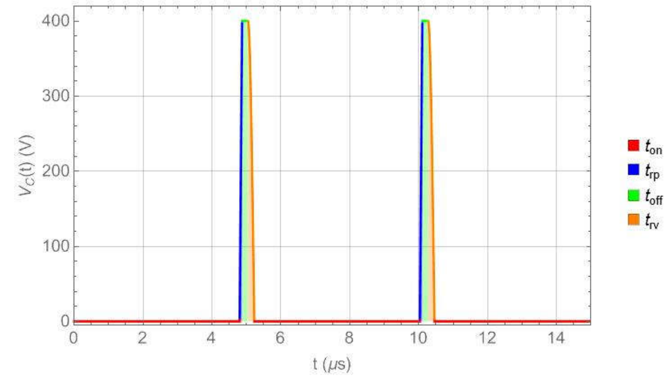


Figure 53. *V_{IN} << 1/2 V_{OUT}, ZVD FET V_{DS}.*

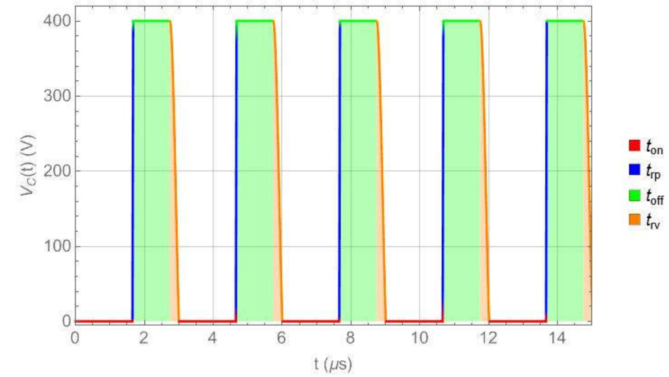


Figure 56. *V_{IN} < 1/2 V_{OUT}, ZVD FET V_{DS}.*

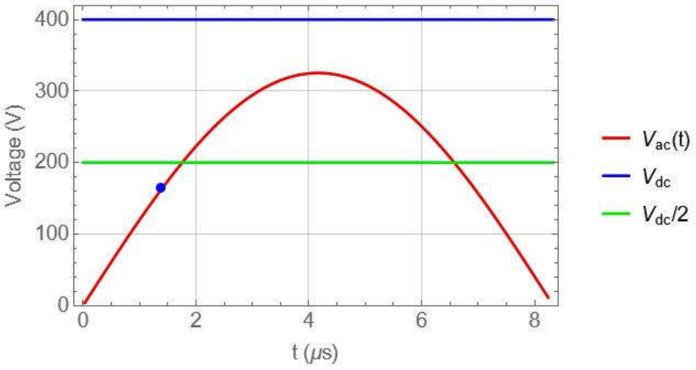


Figure 54. *V_{IN} < 1/2 V_{OUT}, ZVD AC line cycle location.*

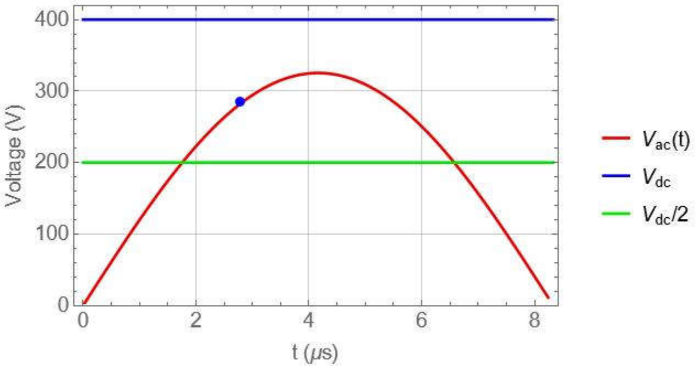


Figure 57. *V_{IN} > 1/2 V_{OUT}, ZVD AC line cycle location.*

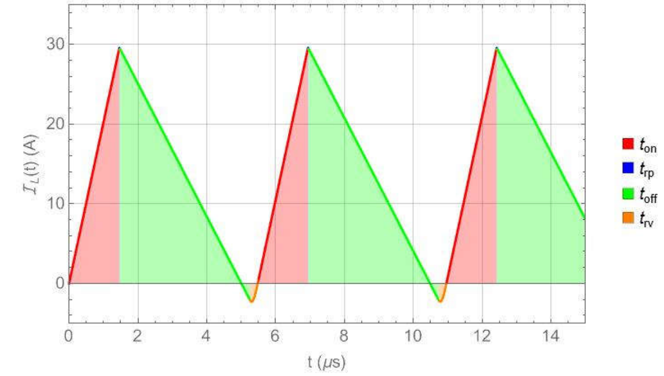


Figure 58. *$V_{IN} > 1/2 V_{OUT}$, ZVD inductor current.*

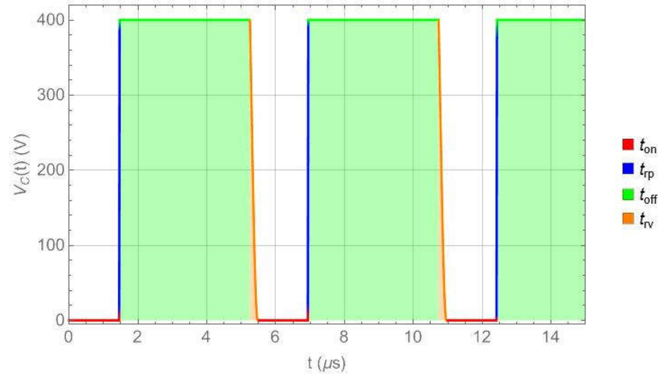


Figure 59. *$V_{IN} > 1/2\ V_{OUT}$, ZVD FET V_{DS}.*

Unfortunately, there is still a problem; this system has no exact solution. The equations left after this simplification are still too complex to solve in real time.

Fortunately, all is not lost; there is something else to try.

The final step in the path to a practical solution for TCM control is to implement a ZVD-based feedback loop. Figure 60 through Figure 62 illustrate what I mean by ZVD feedback. Essentially, I'm going to add a status bit that reports back to the microcontroller anytime the switch turns on with ZVS. For example, take a look at Figure 61 and Figure 62. Figure 61 shows the inductor current, the switch-node voltage and the low-side ZVD flag. Since the system is clearly turning on with ZVS every switching cycle, the ZVD flag is asserted. Figure 62 shows the same waveforms; however, adjusting the frequency loses ZVS. As such, there is no ZVD flag.

The ZVD flag works by asserting a high signal if the switch turns on with ZVS; if it does not, it asserts nothing. The other important observation about this signal is that you don't even need to know precisely when ZVS happened – you only need to know if it happened. This gives you some flexibility on the timing requirements for this function.

In practice, you would implement this ZVD signal inside of a TI GaN switch. While that is not a requirement for this method to work, it makes the implementation extremely simple.

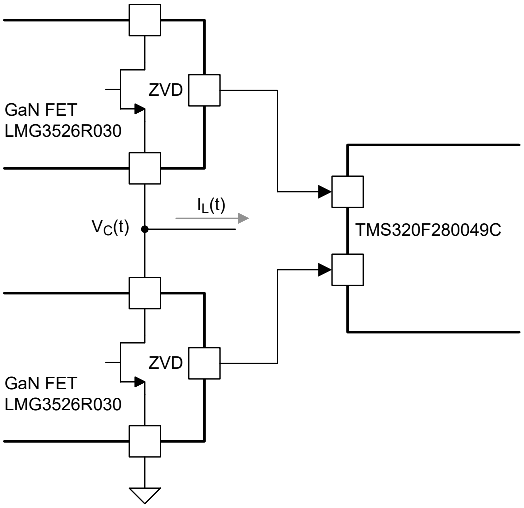


Figure 60. *GaN switch ZVD feedback.*

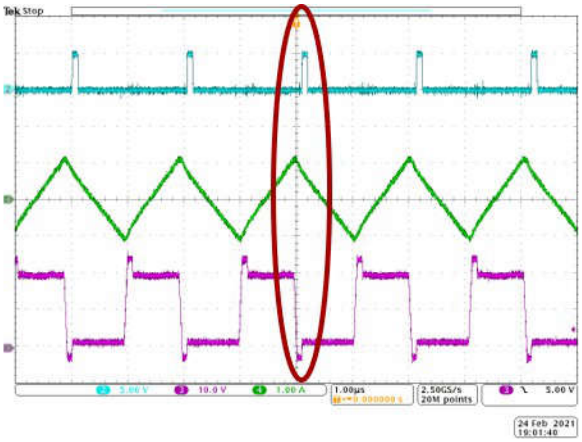


Figure 61. *ZVD detection showing ZVS.*

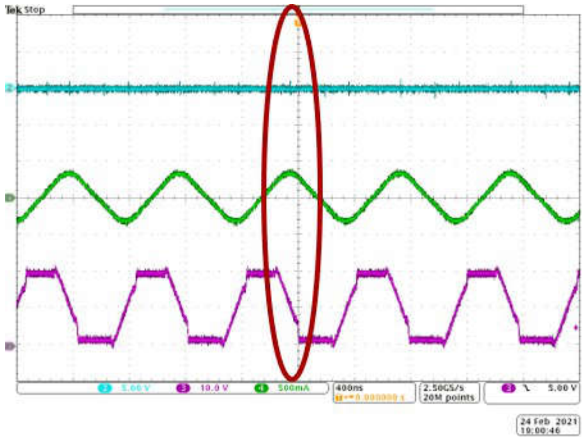


Figure 62. *ZVD detection showing loss of ZVS.*

To help clarify how the ZVD signal can actually help eliminate another control variable calculation, see **Figure 63** through **Figure 67**.

The block diagram in **Figure 63** shows the new system, with the waveforms labeled and color-coded to the plots in **Figure 65** through **Figure 67**. At the top of the plot in **Figure 65** through **Figure 67**, you can see the two gate-drive signals and associated ZVD signals for each FET. Below each is the switch-node current and switch-node voltage. I've also provided a reference waveform to better help visualize when the system is providing an average current commensurate with a power factor of 1.

Figure 65 through **Figure 67** show three different operating points. **Figure 65** shows the operating frequency running lower than the ideal. **Figure 67** runs at the ideal frequency, and **Figure 68** runs faster than the ideal frequency. The only time the ZVD signals are both present is when the modulated waveform syncs up with the target waveform. In fact, you really only need to look at one of the ZVD signals during each one-half cycle. For example, if during the positive half cycle you adjust the period such that the low-side FET is always on the threshold of getting or losing ZVS, you will meet the control objectives.

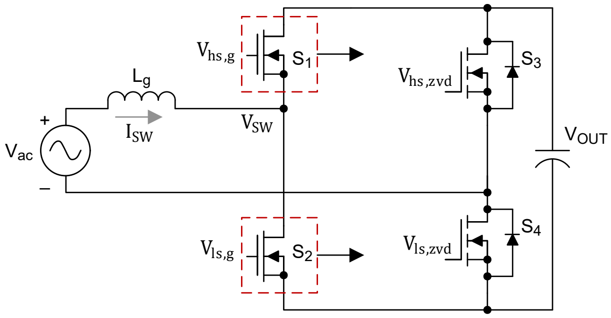


Figure 63. *ZVD feedback schematic.*

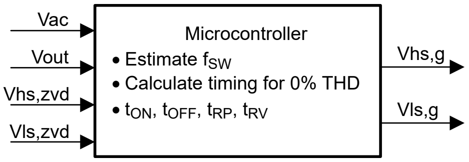


Figure 64. *Microcontroller signals.*

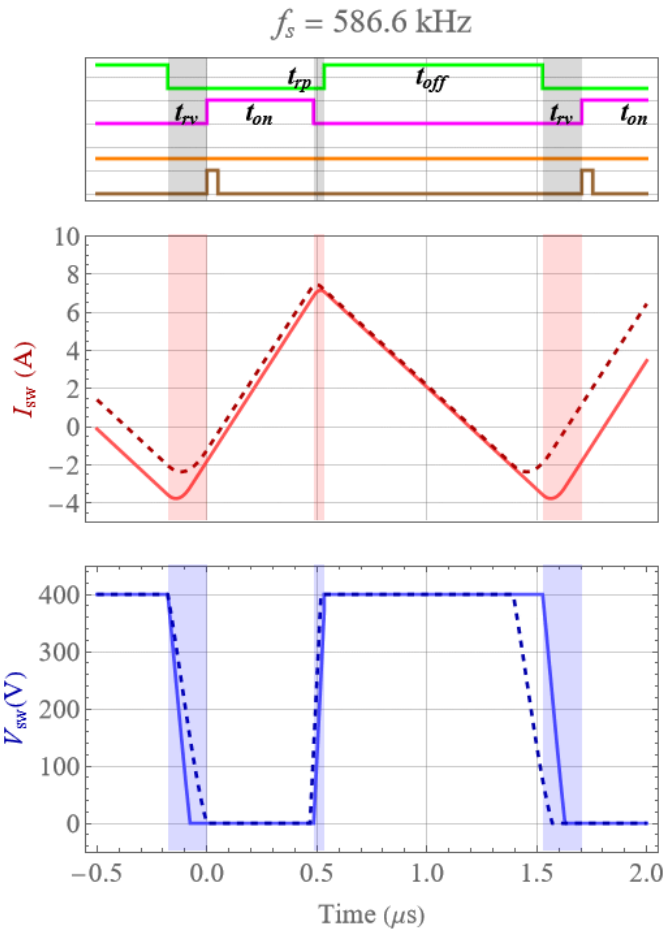


Figure 65. *ZVD feedback loss of ZVS on the high side.*

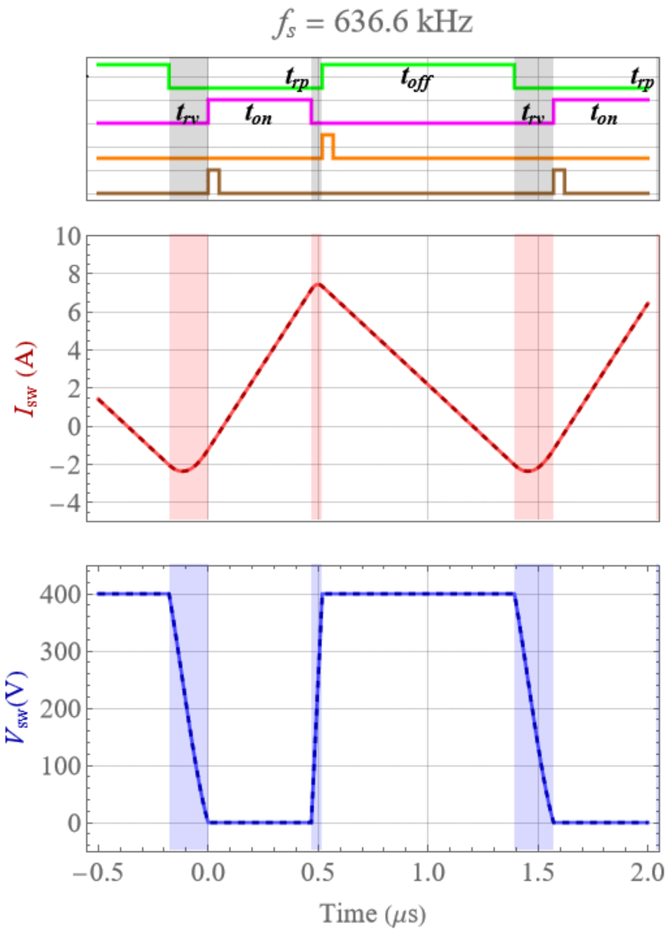


Figure 66. *ZVD feedback loss full ZVS.*

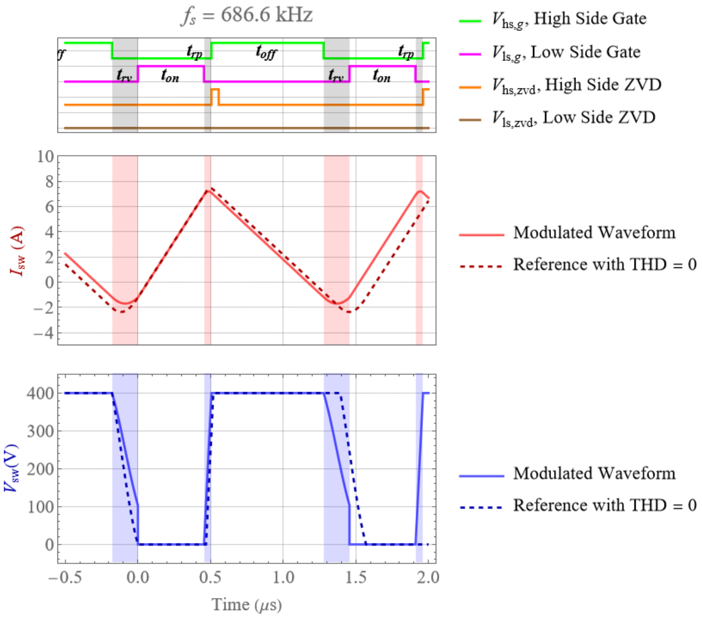


Figure 67. *ZVD feedback loss of ZVS on the low side.*

Control Summary

Before leaving this topic, let's take a high-level view of how ZVD-based control compares to a couple of different ZCD implementations; see **Table 5**. On the left is ZVD control. To the right, I've added a shunt resistor-based current sense; next to that is a current transformer.

From an implementation standpoint, the ZVD-based control can be very simple. All you need to add is an additional channel to an existing isolator. In contrast, the resistor method requires a resistor, operational amplifier and comparator. The current transformer method requires multiple current transformers, comparators and some additional snubbing circuits. Both the resistor and current transformer methods are more expensive.

ZVD detection is also more efficient, since you don't have to add any additional loss-inducing components such as resistors or snubbers.

Lastly, the control is much simpler, and therefore more accurate for ZVD-based control.

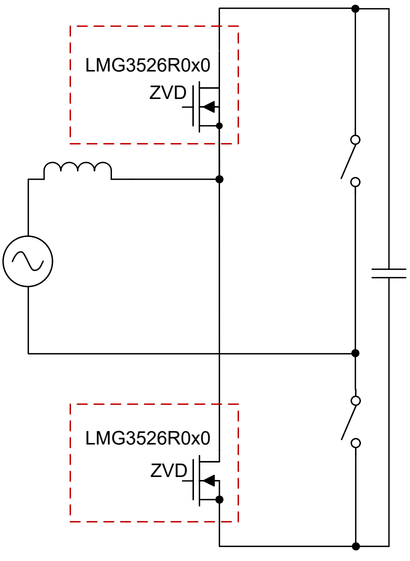
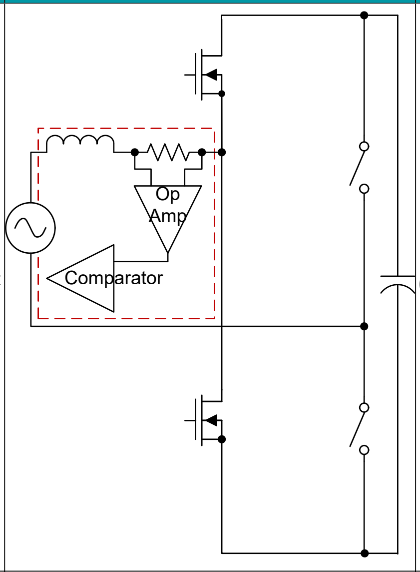
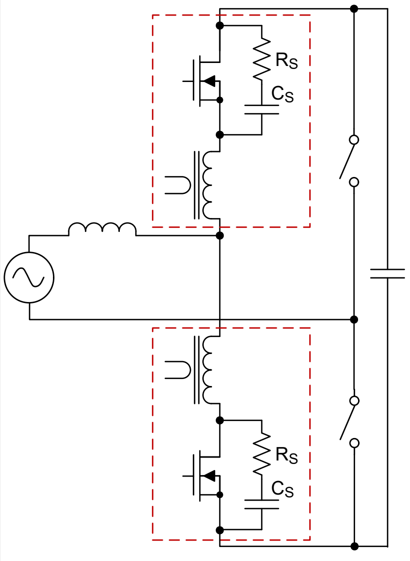
	TI GaN ZVD feature in the LMG3526R030	**Shunt resistor method**	**Current transformer method**
Circuit diagram			
Periphery circuit	**One added channel to an isolator.**	• One shunt resistor. • One high-bandwidth operational amplifier. • One fast comparator.	• Two current transformers. • Two comparators. • Clamping circuits: two high-voltage capacitors, two resistors.
Periphery circuit cost	**$**	$$$	$
Efficiency impact	**No impact**	Reduced efficiency from shunt losses	Reduced efficiency from current transformer and snubber circuit losses
Footprint size	**Almost no additional footprint**	Large	Large
Control complexity	**Simple**	Complex	Complex

Table 5. *ZVD benefits and comparison to other solutions.*

Design Example

Figure 68 shows the schematic of the hardware prototype developed to demonstrate the new control algorithm. **Figure 69** is a photograph of the design, and **Table 6** lists its specifications.

The topology of this design uses a two-phase integrated TCM (iTCM) power-stage design. The converter is designed to operate at a 230-V input with an output voltage of 400 V. The low-frequency inductor is 140 μH and the high-frequency inductor is 14 μH, which gives you an equivalent TCM inductance of about 14 μH. The operating frequency varies from 75 kHz to 1.2 MHz. The microcontroller is a TMS320F280049C and the GaN switches use the integrated ZVD reporting function. Overall, this design is about 120 W/in^3.

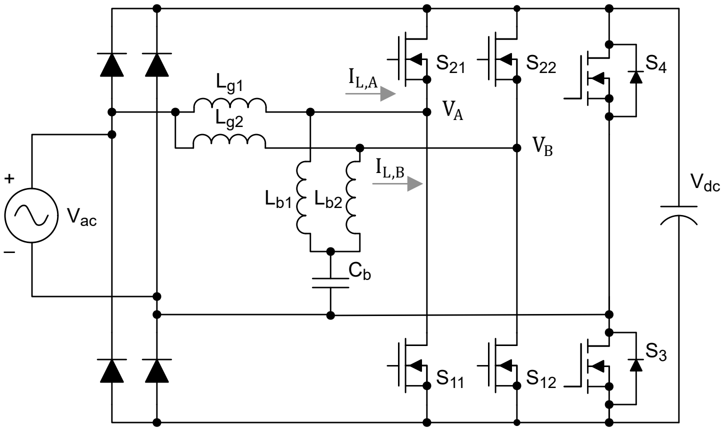


Figure 68. *Design example hardware schematic.*

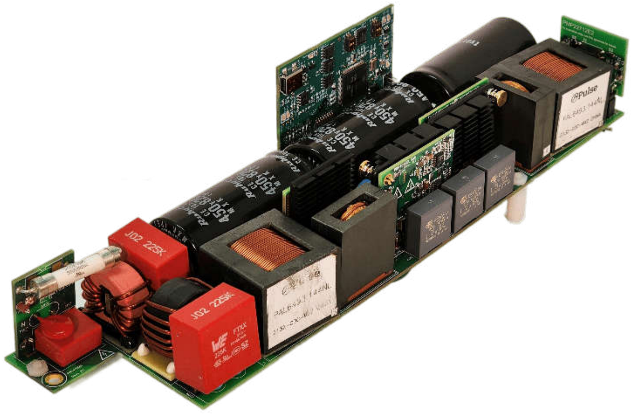


Figure 69. *Design example board photo.*

Parameters	Value
AC input	208 V-264 V
Line frequency	50-60 Hz
DC output	400 V
Maximum power	5 kW
Holdup time at full load	20 ms
Low-frequency inductor (L_g)	140 µH
High-frequency inductor (L_b)	14 µH
High-frequency blocking capacitor (C_b)	1.5 µF
THD	<5%
EMI	European Standard (EN) 55022 Class A
Operating frequency	Variable; 75 kHz-1.2 MHz
Microcontroller	TI: TMS320F280049C
High-frequency GaN FETs (S_{11}, S_{12}, S_{22}, S_{21})	TI: LMG3526R030
Internal dimensions	38 mm × 65 mm × 263 mm
Power density	120 W/in^3

Table 6. *Design example specifications.*

Figure 70 through **Figure 72** include a schematic comparison between a single-phase TCM and iTCM topology. The iTCM topology splits the TCM inductor into two separate inductors: low-frequency inductor L_g and high-frequency inductor L_b. **Equation 6** mathematically relates these two inductors to the TCM inductor:

$$L_{g,TCM} = L_{g,\ iTCM} = \| L_b \tag{6}$$

Adding C_b to the iTCM converter ensures that only high-frequency current passes through the L_b branch. The differential voltage across C_b ends up being identical to the input voltage, V_{ac}.

To better understand how this converter works in **Figure 70** through **Figure 72**, I've added the ripple current envelopes of several of the most important current branches for both the TCM and iTCM converters. Looking at the TCM converter in **Figure 70**, you can see the ripple current envelope. In **Figure 71**, the iTCM converter takes this red waveform and splits it into two separate pieces: a low-frequency component shown in blue and a high-frequency component shown in orange. This component split allows you to optimize the two inductors in the iTCM converter separately. You can optimize the high-frequency inductor for high-frequency current without having the burden of carrying the large DC bias current present in the TCM inductor. Additionally, you can optimize the low-frequency iTCM inductor for low ripple current and high DC bias and possibly take advantage of lower-cost core materials such powered iron, whereas the TCM inductor must be ferrite.

An additional potential benefit of this topology is that the high-frequency current is all contained locally within the converter. This should have a much smaller impact on EMI and reduce the required differential-mode inductance in the EMI filter.

Finally, since the red current envelopes are the same in both converters, you can think of the TCM inductor as the parallel combination of the two inductors in the iTCM converter.

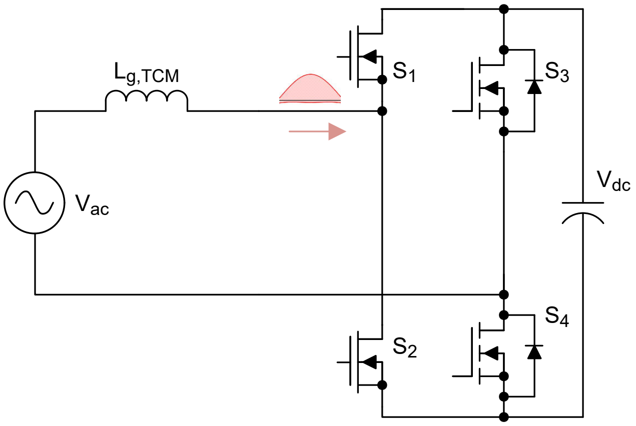


Figure 70. *TCM ripple current envelope.*

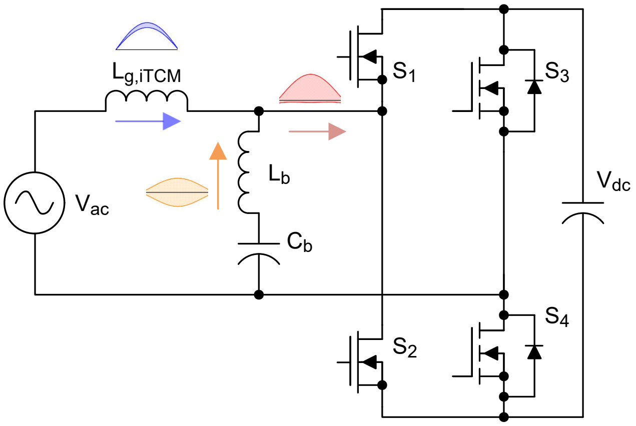


Figure 71. *iTCM ripple current envelope.*

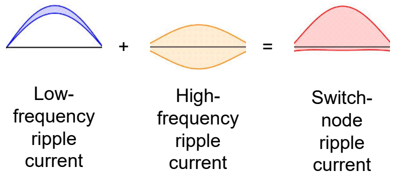


Figure 72. *TCM vs. iTCM ripple current relationships.*

Figure 73 through Figure 78 show the actual switching waveforms for three different input voltages. Figure 73 through Figure 75 show the input voltage waveform, with a blue dot highlighting the input voltage used for the figure below. Figure 76 through Figure 78 graph the current through L_g and L_b, as well as the sum of these currents (denoted as I_{sw}).

V_{IN} = 25

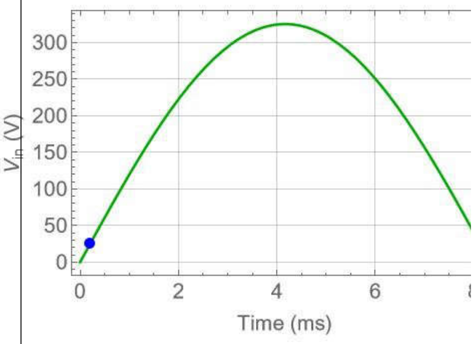


Figure 73. *iTCM/TCM $V_{IN} = 25$.*

V_{IN} = 150

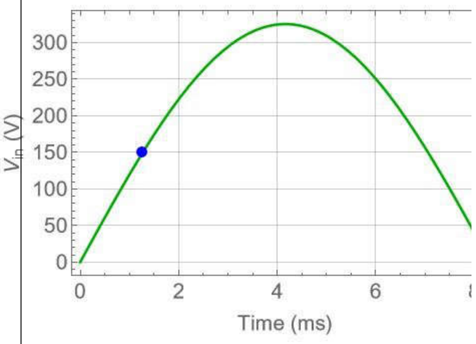


Figure 74. *iTCM/TCM $V_{IN} = 150$.*

V_{IN} = 300 V

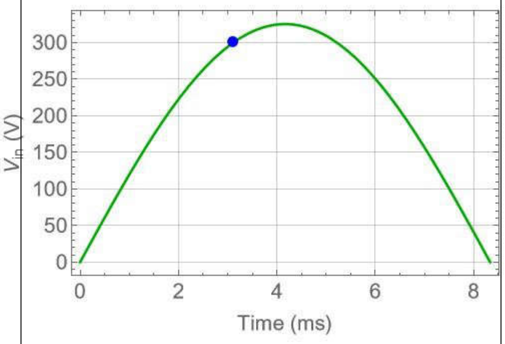


Figure 75. *iTCM/TCM $V_{IN} = 300$.*

V_{IN} = 25

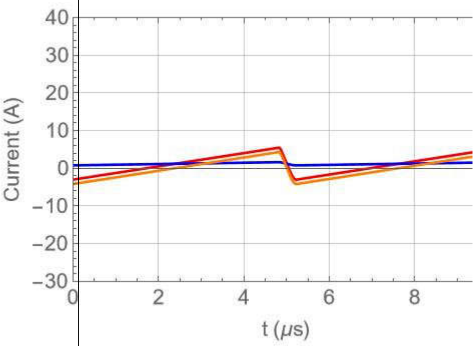


Figure 76. iTCM/TCM V_{IN} = 25, current waveforms.

V_{IN} = 150

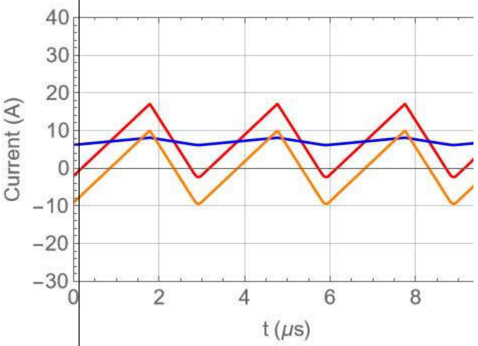


Figure 77. iTCM/TCM V_{IN} = 150, current waveforms.

V_{IN} = 300 V

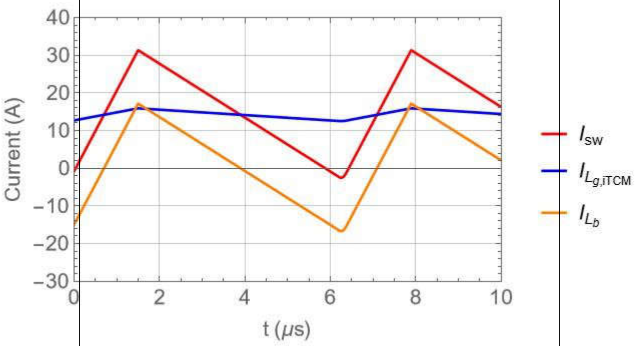


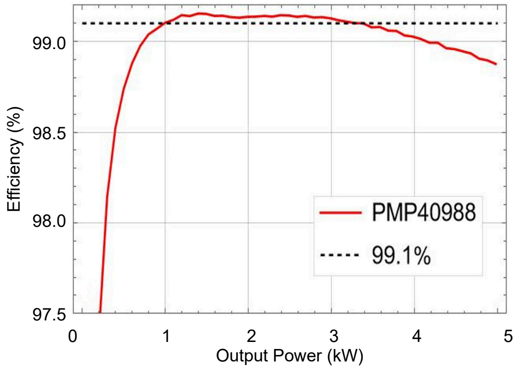
Figure 78. iTCM/TCM V_{IN} = 300, current waveforms.

Experimental Results

Figure 79 and **Figure 80** show efficiency (with automatic phase shedding) and THD performance. The peak efficiency is above 99.1% and the efficiency is above 99% for most of the load range. Phase shedding or adding occurs at around 2 kW.

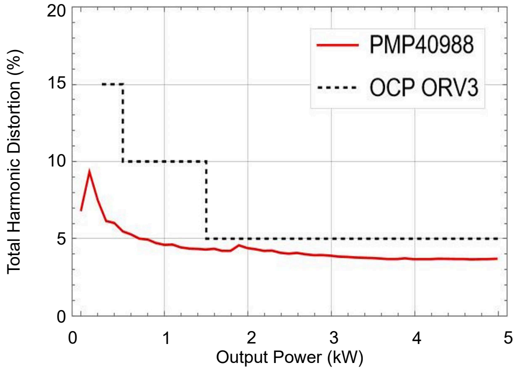
The THD, in my opinion, looks amazing; it is particularly amazing when you consider the absence of current feedback. The THD is below 10% everywhere and below 5% for most of the load range.

In fact, if you are measuring the THD under a no-load condition, the converter is running at about a 1-MHz switching frequency and easily regulating the output. There is about 5 W of loss, and with that, the control is still able to keep the THD under 9%. The control is able to wave-shape the current to a 9% THD with a 5-W load on a 5-kW converter. Personally, I have never heard or seen anything that works this well.



V_{IN} = 230 V   Phase shed/add: 1.8 kW

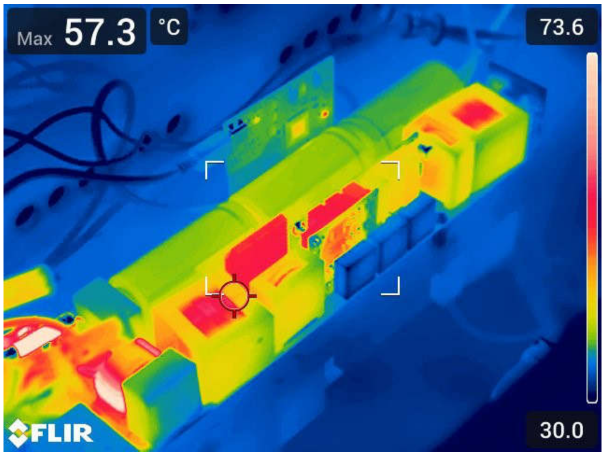
Figure 79. Measured efficiency.



V_{IN} = 230 V   Phase shed/add: 1.8 kW

Figure 80. Measured THD.

Figure 81 and Figure 82 are thermal scans of the unit running under full power with airflow applied. Overall, the unit is running quite cool. All FETs and inductors appear to be below approximately 60°C, which is expected given the high efficiency and low power losses.



V_{IN} = 230 V

$V_{AC} = V_{OUT}$ = 400 V

I_{OUT} = 12.5 A

Airflow = 38 CFM

Figure 81. *Thermal scan, view 1.*

V_{IN} = 230 V

$V_{AC} = V_{OUT}$ = 400 V

I_{OUT} = 12.5 A

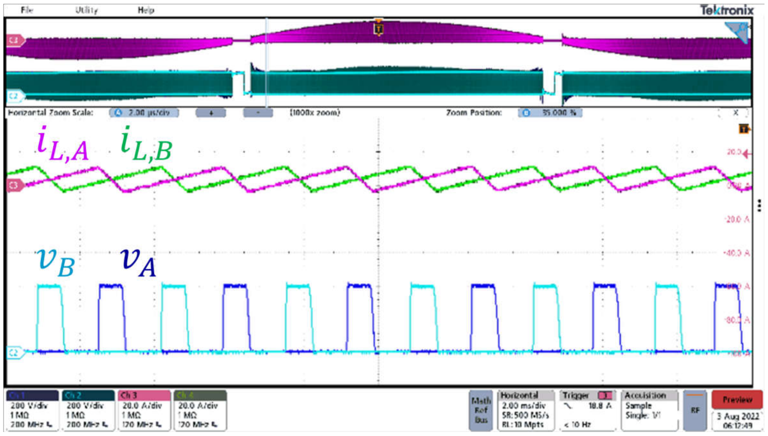
Airflow = 38 CFM

Figure 82. *Thermal scan, view 2.*

Figure 83 through Figure 85 are waveforms of the system with the new control running under full-load operation with a 230-V_{AC} input and a 400-V_{DC} output. For the schematic, see Figure 68. In each figure, you can see the totem-pole half-bridge switch current for each phase, as well as the switch-node voltage. The figures show three conditions corresponding to three different regions where designers traditionally need to give special consideration to achieve ZVS. These regions are when $V_{IN} < ½ V_{OUT}$, $V_{IN} = ½ V_{OUT}$ and $V_{IN} > ½ V_{OUT}$.

Figure 83 through Figure 85 illustrate several things:

- The achievement of ZVS for both FETs under all input voltage conditions.
- A perfectly interleaved system with variable frequency operation.
- A very sinusoidal current envelope.



$V_{IN} < ½ V_{OUT}$

V_{IN} = 230

$V_{RMS} = V_{OUT}$ = 400 V

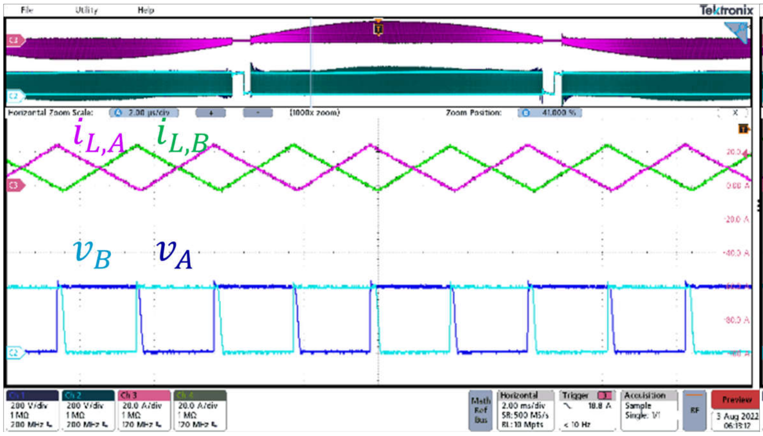
P = 5 kW

$v_A = v_B$ = 200 V/div

$i_{L,A} = i_{L,B}$ = 20 A/div

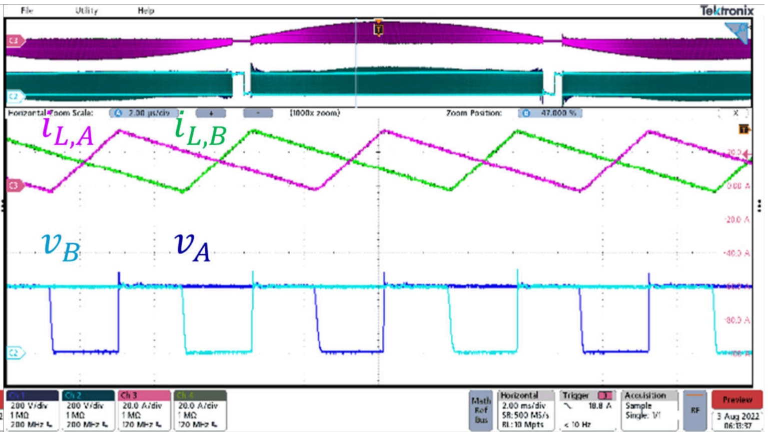
Time = 2 µs/div

Figure 83. *Full power waveforms*



$V_{IN} = ½ V_{OUT}$	$V_{IN} = 230$
$V_{RMS} = V_{OUT} = 400$ V	P = 5 kW
$v_A = v_B = 200$ V/div	$i_{L,A} = i_{L,B} = 20$ A/div
Time = 2 µs/div	

Figure 84. *Full power waveforms.*

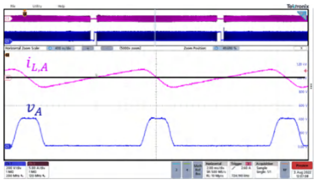


$V_{IN} >> ½ V_{OUT}$	$V_{IN} = 230$
$V_{RMS} = V_{OUT} = 400$ V	P = 5 kW
$v_A = v_B = 200$ V/div	$i_{L,A} = i_{L,B} = 20$ A/div
Time = 2 µs/div	

Figure 85. *Full power waveforms.*

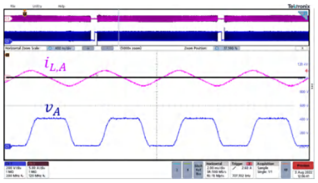
Figure 86 through **Figure 88** show the same information under a no-load operating condition. Because the load is so small, it is operating with only one phase.

In some sense, these figures are even more impressive given the true no-load operational condition. You can see clearly that the new control algorithm has adaptively adjusted both dead times based on the ZVD signal to achieve near-ideal ZVS for both GaN FETs. This is evident because both resonant transitions are the same, indicating that the resonant peak dead time has changed to be equal to the resonant valley dead time. The later of course is a constant equal to $\pi/2$.



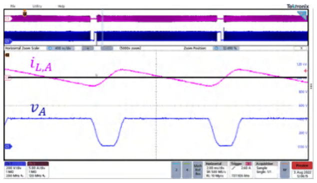
$V_{IN} << ½ V_{OUT}$	$V_{IN} = 230$
$V_{RMS} = V_{OUT} = 400$ V	P = 0 kW
$v_A = 200$ V/div	$i_{L,A} = 20$ A/div
Time = 2 µs/div	

Figure 86. *No-load waveforms.*



$V_{IN} = ½ V_{OUT}$	$V_{IN} = 230$
$V_{RMS} = V_{OUT} = 400$ V	P = 0 kW
$v_A = 200$ V/div	$i_{L,A} = 20$ A/div
Time = 2 µs/div	

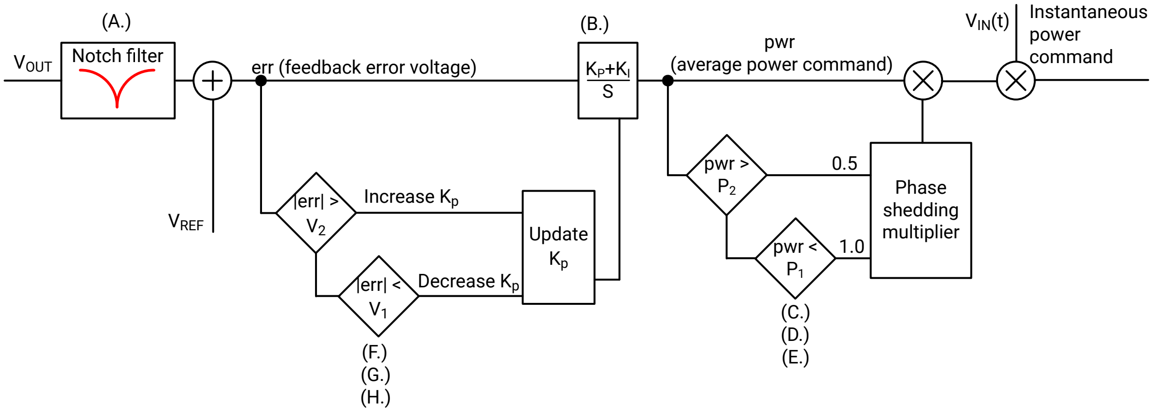
Figure 87. *No-load waveforms.*



$V_{IN} >> ½ V_{OUT}$	$V_{IN} = 230$
$V_{RMS} = V_{OUT} = 400$ V	P = 0 kW
$v_A = 200$ V/div	$i_{L,A} = 20$ A/div
Time = 2 μs/div	

Figure 88. *No-load waveforms.*

Figure 89 shows the control loop for the PFC voltage compensator. Starting from the left side, you can see a 120-Hz notch filter. This filter enables a faster voltage-loop bandwidth than normal because the notch filter prevents the control loop from trying to eliminate any 120-Hz content. Next is a nonlinear control loop that dynamically adjusts the K_p value of the standard proportional-integral (PI) controller. The output of the PI controller is proportional to the power demand of the system, which is used to determine how many phases should be operating. If two phases are operating, you would divide the power command delivered to each phase by 2. Finally, multiplying the output of the phase shedding stage by the measured input voltage creates a cycle-by-cycle power command for the control algorithm.



A. Notch filter removes 120-Hz ripple

B. Standard PI controller, equivalent to an integrator with an added zero

C. P2 = Phase adding threshold

D. P1 = Phase shedding threshold

E. Feedforward adjusts the power command to each phase depending on how many phases are running

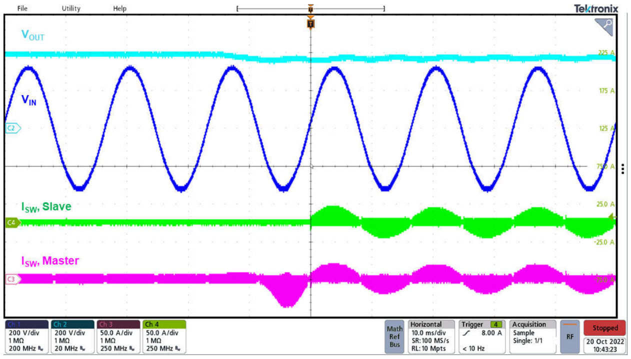
F. V2 = Upper error threshold

G. V1 = Lower error threshold

H. Dynamically change K_P to enable faster transient response when the output is far from its target

Figure 89. *Voltage-loop control loop.*

Figure 90 shows a load transient from approximately no load to 50%, showing V_{IN}, V_{OUT} and the two-phase switch-node currents. The figure clearly shows the system seamlessly transitioning from one- to two-phase operation, with minimal disturbance to the output voltage.



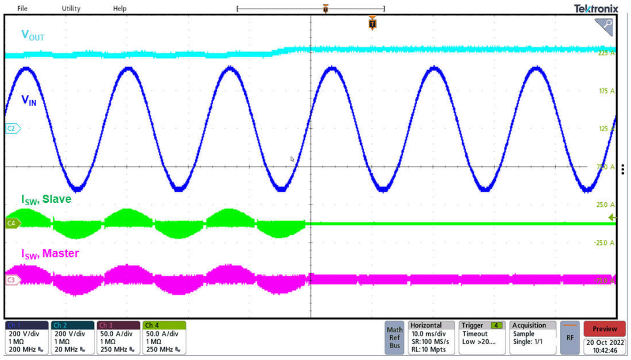
V_{IN} = 230

V_{AC} = V_{OUT} = 400 V

I_{OUT} from 0.1 A to 6.25 A

Figure 90. *Load transient.*

Figure 91 shows a load release from 50% load to approximately a no-load condition. The system seamlessly transitions from two phases to one phase with minimal disturbance to the output voltage.



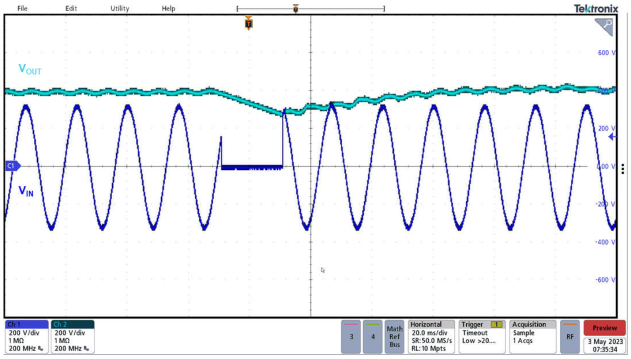
V_{IN} = 230

V_{AC} = V_{OUT} = 400 V

I_{OUT} from 6.25 A to 0.1 A

Figure 91. *Load transient.*

Figure 92 shows a full-load 20-ms AC dropout event with the phase shift of the dropout event adjusted so that when the AC voltage returns, it is at its highest value. This condition creates the worst-case current surge after the inrush. The output voltage recovers smoothly and quickly from the event.



V_{IN} = 230

V_{AC} = V_{OUT} = 400 V

I_{OUT} = 12.5 A

Dropout time = 20 ms

Phase = 30°

Figure 92. *AC dropout*

Conclusions

It is possible to design a computationally simple transition mode-controlled PFC that achieves ZVS under all operating conditions, with outstanding THD and cost savings realized by not needing a current sensor for control. In addition, the solution uses a two-phase iTCM converter with near-ideal interleaving. Overall, the converter achieved over 99.1% efficiency and a THD <6%.

Additional Resources

1. Fernandes, Ryan, and Olivier Trescases. "A Multimode 1-MHz PFC Front End with Digital Peak Current Modulation." Published in IEEE Transactions on Power Electronics 31, no. 8 (August 2016): pp. 5694-5708. doi: 10.1109/TPEL.2015.2499194.
2. Lim, Shu Fan, and Ashwin M. Khambadkone. "A Multimode Digital Control Scheme for Boost PFC with Higher Efficiency and Power Factor at Light Load." Published in 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Feb. 5-9, 2012, pp. 291-298. doi: 10.1109/APEC.2012.6165833.

3. Rothmund, Daniel, Dominik Bortis, Jonas Huber, Davide Biadene, and Johann W. Kolar. “10kV SiC-Based Bidirectional Soft-Switching Single-Phase AC/DC Converter Concept for Medium-Voltage Solid-State Transformers.” Published in 2017 IEEE 8th International Symposium on Power Electronics for Distributed Generation Systems (PEDG), April 17-20, 2017, pp. 1-8. doi: 10.1109/PEDG.2017.7972488.
4. Liu, Zhengyang. 2017. “**Characterization and Application of Wide-Band-Gap Devices for High Frequency Power Conversion**.” Ph.D. dissertation, Virginia Polytechnic Institute and State University.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated