TL5002 Provides DDR Bus Termination Power Supply

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ABSTRACT

Double data rate (DDR) bus termination power requirements bring new challenges to the power supply by requiring voltage tracking of a reference supply, requiring both sourcing and sinking current, and maintaining a high efficiency over a wide current range. This paper address these issues while presenting an example DDR design of 12 A of output current with voltage outputs between 0.9 V and 1.25 V. Issues and their solutions are provided for the power supply operating as a tradition buck power stage in the sourcing mode as well as for operating as a synchronous boost regulator in the sinking mode. Regulation and control loop characteristics of the examples are presented for both current sinking and sourcing modes of operation. Transient load response is also presented showing output voltage variation, as the current is transitioned from sourcing to sinking. Sufficient design detail is provided to form the basis for a successful DDR power supply.

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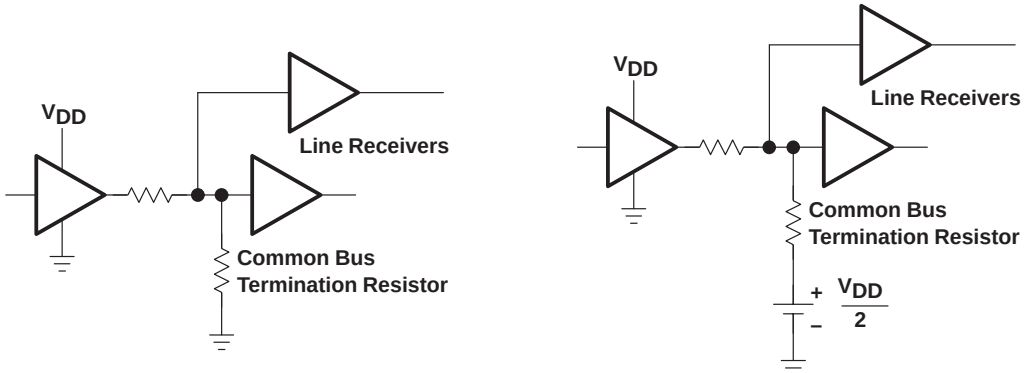
1 Introduction

Power dissipation within CMOS logic systems is related to the clock frequency, the input capacitance of the various gates within the system, and the supply voltage. As device feature sizes and, hence, supply voltages have been reduced, significant gains have been made in lowering system power dissipation. These reduced dissipations and higher operation speeds of the lower voltage devices have allowed system clock frequencies to be pushed up into the 100's of Megahertz. At these very high clock frequencies, clock distribution changes from the digital world back into the analog world. Controlled impedances, properly terminated busses, and minimal cross coupling provide a high fidelity clock signal. Traditionally, logic systems have been designed to clock data on only one edge of the clock, while the new double data rate (DDR) memories clock on both the leading and falling edge of the clock. This doubles the data rate while slightly increasing system power dissipation.

The increased data rate requires that the clock distribution network be carefully designed to minimize ringing and reflections which may inadvertently clock logic devices. Two possible bus termination schemes are presented in Figure 1. In the first schematic, bus termination resistors are placed at the end of the distribution network and are connected to ground. If the bus driver is in the low state, the resistors have zero dissipation. In the high state, the resistors dissipate power equal to the supply voltage (V_{DD}) squared divided by the bus resistance. With a random voltage on the bus, the average loss is the supply voltage squared divided by twice the bus resistance. In the second scheme shown in Figure 1, the termination resistor is connected to a supply voltage (V_{TT}) that is one half the V_{DD} voltage. The dissipation in the termination resistor is then constant regardless of the supply voltage and is equal to V_{TT} (or (V_{DD}/2) squared divided by the termination resistance. This results in a factor of two power savings when compared with the first approach (in case a bus signal is high 50% of the time and low 50% of the time), but at the cost of an additional power supply. However, the requirements on this power supply are a little unique. First, its output needs to be one half the driver voltage (V_{DD}). Second, it needs both source and sink current. When the driver output voltage is low, current flows from the V_{TT} supply into the driver. However, when the driver is high, current flows from the driver into the supply. Finally, the supply needs to go from either operating mode into the other mode as the system data changes.



Bus Termination Scheme 1 (Termination Resistors Tied to Ground)

Bus Termination Scheme 2 (Termination Resistors Tied to V_{TT})

Figure 1. Bus Termination Schemes

2 Topology

Figure 2 presents the power supply topology proposed for DDR applications. Depending on output current demands, the circuit operates in two modes. With a sourcing requirement, the circuit operates as a synchronous buck power stage taking input power from the source and providing it to the load. However, with a sinking requirement, the circuit operates as a synchronous boost power stage taking power from the output and returning it to the input. These two different operating modes create challenges in maintaining good efficiency and good transient response.

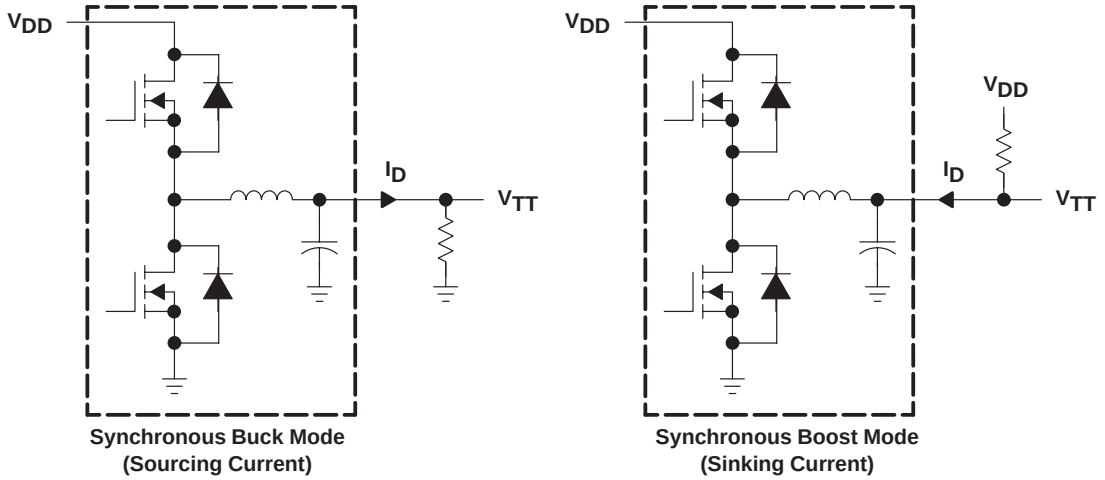


Figure 2. Two Operating Modes of the DDR Power Supply

With the DDR supply operating as a boost and buck converter, a new scheme to control switching of the power switches is needed. In the more recent synchronous buck control schemes, the transition from where the high side MOSFET conducts to where the low side MOSFET conducts and the transition from where the low side MOSFET conducts to where the high side MOSFET conducts have been handled differently. The high side to low side transition can be made almost lossless. The high side switch can be turned off, allowing the inductor to swing the phase voltage to 0 V. A comparator can be used to sense the phase voltage and turn the bottom switch on with 0 V across it resulting in zero voltage switching of both devices. The other transition is hard switched and incurs losses as the phase voltage must be switched positive, resulting in cross conduction and capacitive loss. In the boost mode of operation, the zero voltage switching transition occurs at the low side to high side transition and the hard switching occurs as the inductor node is pulled low. This means that a control strategy is needed to respond to the two operating modes to maintain good efficiency. Figure 3 and Figure 4 show waveforms with two operating modes. The waveform in Figure 3 shows the phase voltage during the buck mode of operation. At the left side, the bottom switch is on. Later, the current starts to transition to its internal diode and the top switch is turned on. The top switch conducts at the proper duty factor and is then turned off. The inductor then drives the phase voltage toward the low rail, the bottom catch diode (body diode of the synchronous FET) limits the voltage at which time the bottom switch is turned back on. The waveform in Figure 4 shows the phase voltage during the boost mode of operation and starts with the bottom switch on. The bottom synchronous FET is then turned off and the phase voltage is driven positive by the inductor. The top diode conducts for a brief amount of time before the top switch is turned on. This transition provides lossless turn on and off of both switches. The high to low transition begins with the top switch turning off and current transitioning to its internal diode.

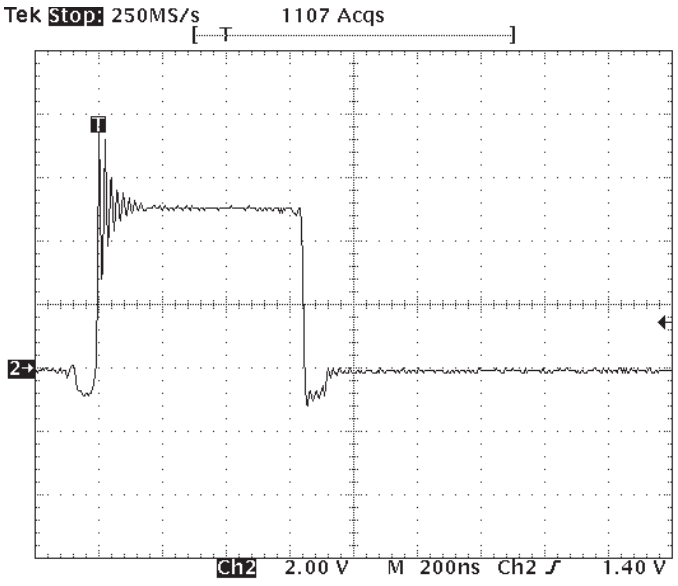


Figure 3. Phase Voltage While Sourcing Current

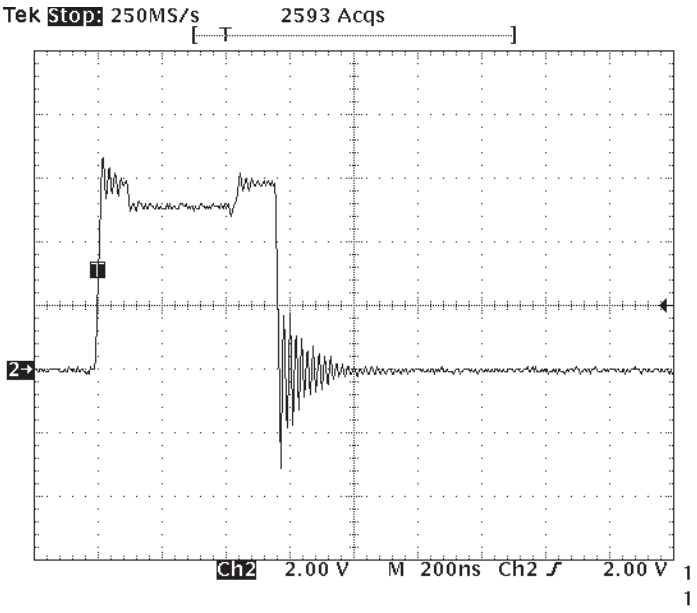


Figure 4. Phase Voltage While Sinking Current

With two modes of operation, it is not intuitive what the control characteristics of the supply should be. In the buck operating mode, the supply will maintain an output voltage (V_{TT}) independently of the output current and the input voltage. In the boost operating mode, the supply will maintain the input voltage (V_{TT}) independent of the output voltage and the output current. Realizing the supply is just a buck converter operating at a less than positive output current is the proper visualization. As shown in Figure 5, loop gain is essentially independent of the operating mode.

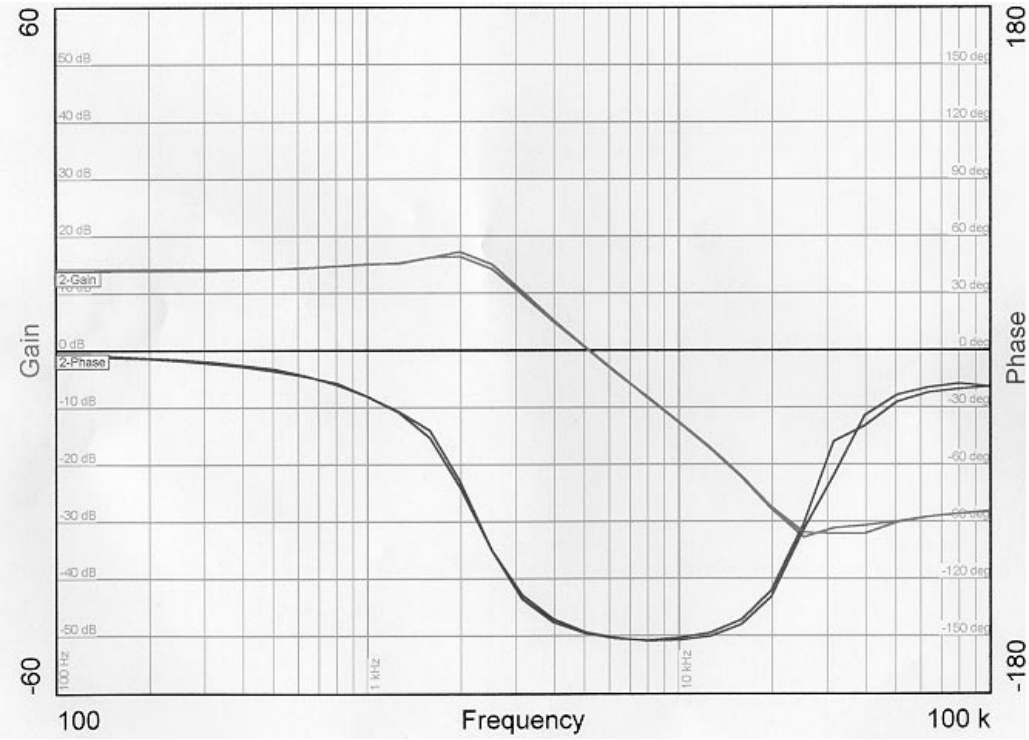


Figure 5. Power Stage Gain Characteristics (Sourcing and Sinking Modes)

3 TL5002 Controller

Figure 6 presents the block diagram of a new, very simple, and inexpensive IC available for DDR control. Rated for 3.6-V to 40-V operations, it can be used in a number of applications besides DDR. The monolithic chip contains minimal circuitry to perform frequency generation, voltage regulation, and pulse width modulation. Operating frequency can be programmed by a single external resistor up to 500 kHz. An error amplifier with uncommitted inputs is provided to compare the V_{TT} output voltage to one half the V_{DD} supply. The amplifier has a gain bandwidth product of near 3 MHz, allowing a wide, control-loop bandwidth. The output of the error amplifier is internally compared against a sawtooth waveform generated by the oscillator and it sets the pulse width during normal operation. A third input to the comparator provides a soft start function during the initial turnon interval and can be used to set a maximum pulse width. An internal current source provides this feature with minimal external components. An undervoltage lockout circuit prevents spurious operation during a low-input voltage condition by gating an output and a gate. The output of the chip is an open-collector transistor, that is easily interfaced to a number of drive circuits.

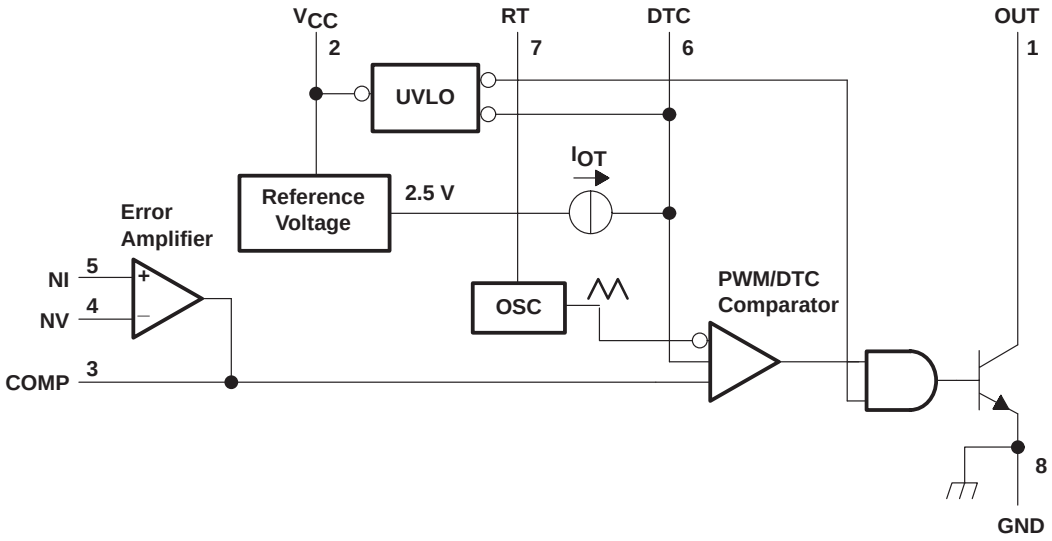


Figure 6. TL5002 Block Diagram

4 Prototype Performance

The schematic of a power supply that can be used to power DDR memory is shown in Figure 7. This circuit is available as an evaluation module from Texas Instruments (part number SLVP180). The top and bottom power MOSFETs are switched on and off by the TPS2837, a high/low side synchronous-MOSFET driver, while the TL5002 controller maintains the output voltage regulation. The TL5002's regulation method differs from that of a typical controller that contains a fixed internal reference voltage. In the TL5002, an external voltage is used in place of the internal reference voltage. The reference voltage input to the tracking regulator (designated V_{DDQ}) is typically scaled by 0.5 to provide an output voltage equal to one half of V_{DDQ}. The TL5002 then compares this scaled voltage to the sensed-output voltage and creates an error signal that is used to adjust the on time of the top side MOSFETs.

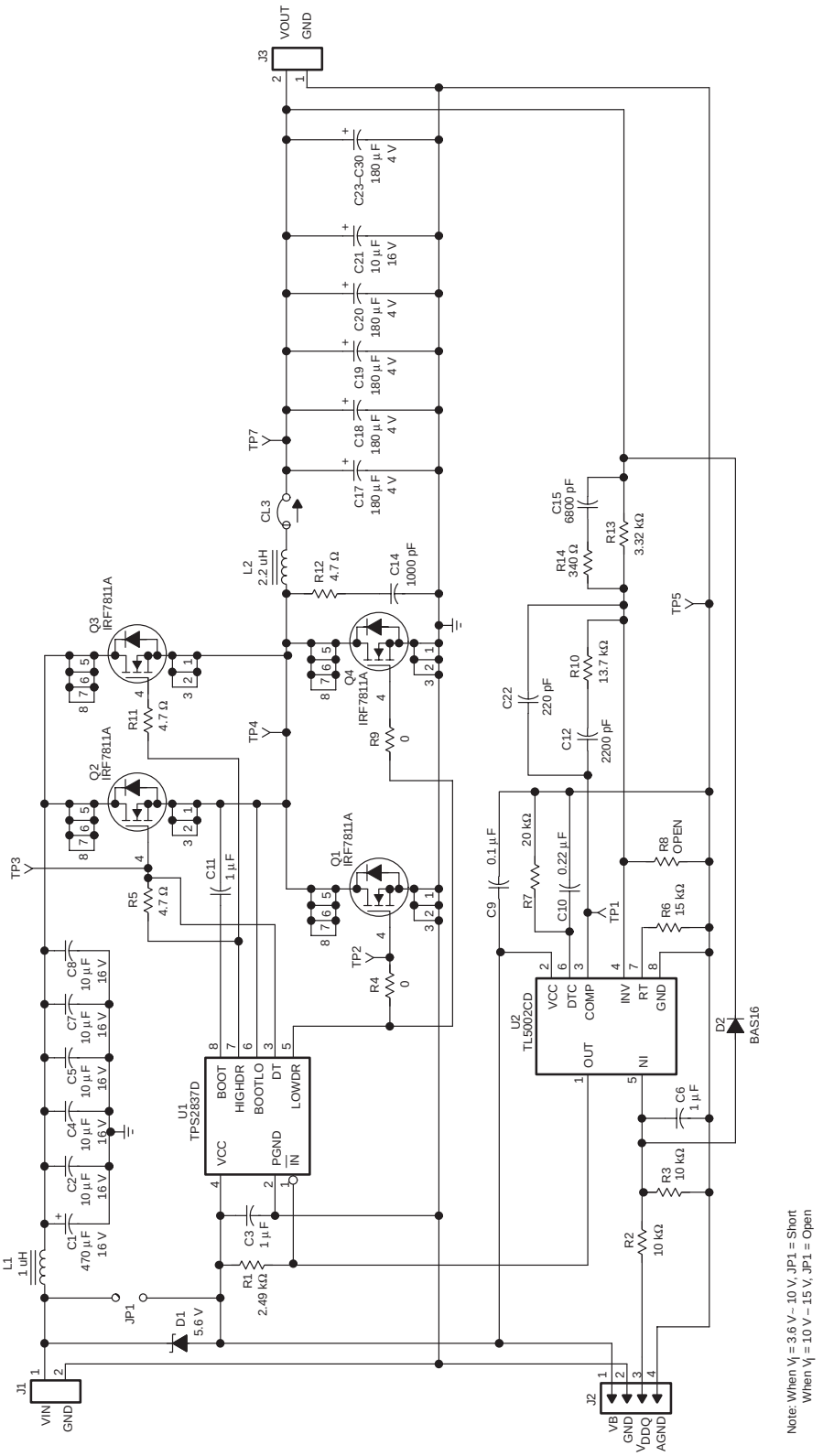


Figure 7. TL5002 EVM Schematic

The TL5002 EVM DDR tracking regulator operates in a voltage mode control and has a nominal switching frequency of 400 kHz. The high side and low side switches are each implemented with two parallel connected SO–8 package FETs to reduce the power dissipation in each device to an acceptable level for an SO–8 package. Heavy copper etch is used on multiple layers to spread the heat away from the MOSFETs and distribute across the PWB. An input filter inductor minimizes the ripple voltage imposed back on the input voltage source. Two high-side MOSFETs and two low-side MOSFETs provide the optimal combination to handle the power dissipated as switching and conduction losses in the MOSFETs. Although this design is optimized for 12 A, changing the quantity of the top and bottom FETs can generate more or less output current. If a total of one top and one bottom FET is used, the output current capability would be approximately 6 A. However, several other design factors would need to be taken into account. Fewer input capacitors are needed to handle the input ripple current and an output inductor rated for less current reduces the overall circuit area. If higher output currents are desired, more MOSFETs and a larger inductor are required to handle the increased current requirement. In addition, a second TPS2837 FET driver may be required due to the power dissipation limits of the driver package. A 40-A design utilizing a second TPS2837 driver and a total of 10 top and bottom FETs has been built and successfully tested. Thus, this design is scalable to the output current needed by increasing the power dissipation capability of the power stage.

Figure 8 shows the transient-output voltage performance. The bottom waveform shows the output current transitioning from a sinking –12 A, to a sourcing 12 A of current. The top waveform shows the resulting output voltage transients. The power supply maintains voltage regulation within an acceptable window of 40 mV at these extreme conditions. The current being sourced from or sunk into the tracking regulator is a function of the address data states being driven and the amount of memory being addressed. This test is an extreme of all the data lines simultaneously changing from one state to another (see the test setup (Figure 3–1 and 3–2) in the DDR power supply EVM user's guide, literature number SLVU044, from Texas Instruments). Actual operating conditions likely will not be as severe.

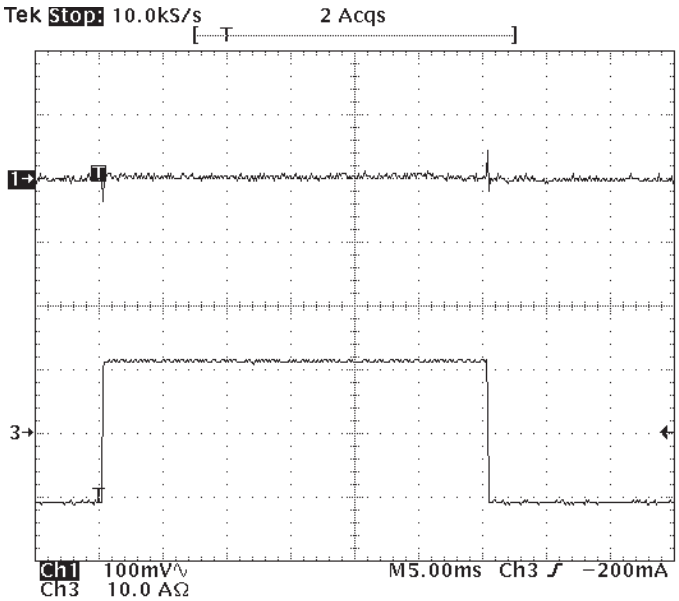


Figure 8. Full Sourcing to Full Sinking Transient Response

Figure 9 shows the measured efficiency of the TL5002 EVM while operating as a tracking regulator with a 5-V input and 1.25-V output (V_{DDQ} is equal to 2.5 V). Efficiency is good and approaches 86%, even with the low-voltage output of 1.25 V. Higher efficiency is possible with an increase in MOSFET count and cost. The efficiency when sourcing current is higher than it is when sinking current. Improvements in the sinking current mode can be made with the introduction of faster power switches or a different control method. In the present implementation, the gate drive voltage of the top FET controls the turn on of the bottom FET during the high side to low side transition. The gate drive timing during the low-side to high-side transition is controlled by a simple delay. This method takes advantage of the zero voltage switching of the buck mode of operation, but results in lower efficiency for the boost mode.

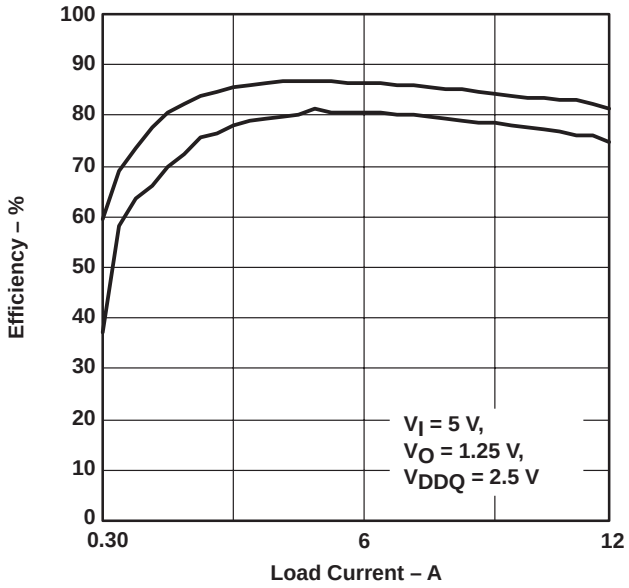


Figure 9. TL5002 EVM Efficiency as a V_{TT} Tracking Regulator

The power stage was also designed to be a dedicated synchronous buck regulator with an output as high as 3.3 V when powered from a 5-V input voltage. This is accomplished by replacing the TL5002 controller with the TL5001 pulse width modulator controller and making minimal component changes. Figure 10 shows the efficiency of the TL5001 implementation configured for a fixed 2.5 V_O when powered from a 5-V input. The improvement in efficiency can be attributed to the increased output voltage.

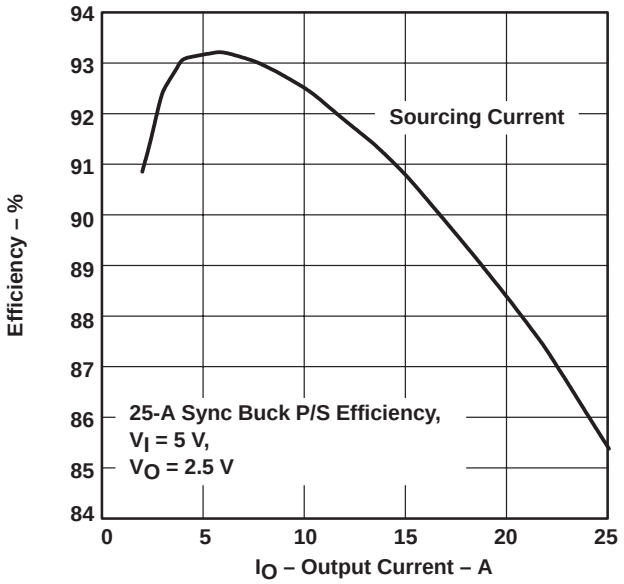


Figure 10. TL5002 EVM Efficiency as a 2.5-V V_{DD} Regulator

A summary of the specifications for the DDR power supply are listed in Table 1.

Table 1. Prototype Operating Specifications

SPECIFICATIONS		MIN	TYP	MAX	UNITS
Input voltage range, V_I		3.6	5	15	V
V_{DDQ} voltage range		1.8	2.5	3	V
Output voltage range, V_O		$\frac{V_{DDQ}}{2} - 40$ mV	$\frac{V_{DDQ}}{2}$	$\frac{V_{DDQ}}{2} + 40$ mV	V
Output current range, I_O		–12		12	A
Operating frequency, f			400		kHz
Output ripple	Steady state			5†	mV
	At load transient of 0.4 A/µsec	–35‡		35‡	mV
Efficiency			85§	86.3§	%

† V_I = 5 V, V_O = 1.25 V, I_O = 12 A
‡ V_I = 5 V, V_O = 1.25 V, I_O = ±12 A
§ *V_I = 5 V, V_O = 1.25 V, I_O = 4.6 A

5 Conclusions

A new control IC has been introduced to address the needs of the DDR bus termination power. The controller provides voltage tracking of a reference supply and both sourcing and sinking current, while maintaining a high efficiency over a wide current range. An example DDR design with an output current of 12 A and voltage outputs between 0.9 V and 1.25 V was presented. Issues and their solutions were provided for the power supply operating as a traditional buck-power stage in the sourcing mode, as well as operation as a synchronous boost regulator in the sinking mode. Control loop characteristics were found to be identical in both sinking and sourcing modes of operation that allowed fast transient load. The design is scalable with an output current range of 1 A to 40 A. Sufficient design detail was provided to form the basis for a successful DDR power supply.

6 References

1. Y.R. Kim, *DDR, Today and Tomorrow*, Platform conference, Silicon Conference Center, San Jose, CA, July 18–19, 2000
2. *TL5002, Pulse Width Modulator Control*, Texas Instruments, Dallas, TX
3. EIA/JEDEC Standard*, Stub Series Terminated Logic for 2.5 V (SSTL–2), EIA/JESD8–9, Electronic Industries Alliances*, September 1998

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