TPS25741 Power Multiplexing Introduction and Design Considerations

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ABSTRACT

The TPS25741 is a USB Type-C™ *Power Delivery* (PD) *Downstream Facing Port* (DFP) controller that supports multiplexing two existing input voltage rails onto VBUS. The TPS25741 adopts a special control scheme to ensure smooth voltage transitions per USB Power Delivery Specification while preventing reverse current between the two input rails. This application note describes the TPS25741 multiplexer control scheme and also presents a solution to avoid common issues when using P-FETs for multiplexing.

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1   Introduction of Power Multiplexing

In USB Type-C PD source implementations, the Type-C controller needs to work with the upstream DC-DC to provide voltage to the sink. In many cases, TPS25741 uses CTL1 and CTL2 to control upstream DC-DC to provide requested voltages as Figure 1 shows. This topology is used in applications where the upstream DC-DC is dedicated for USB charging ports like an adaptor or power hub.
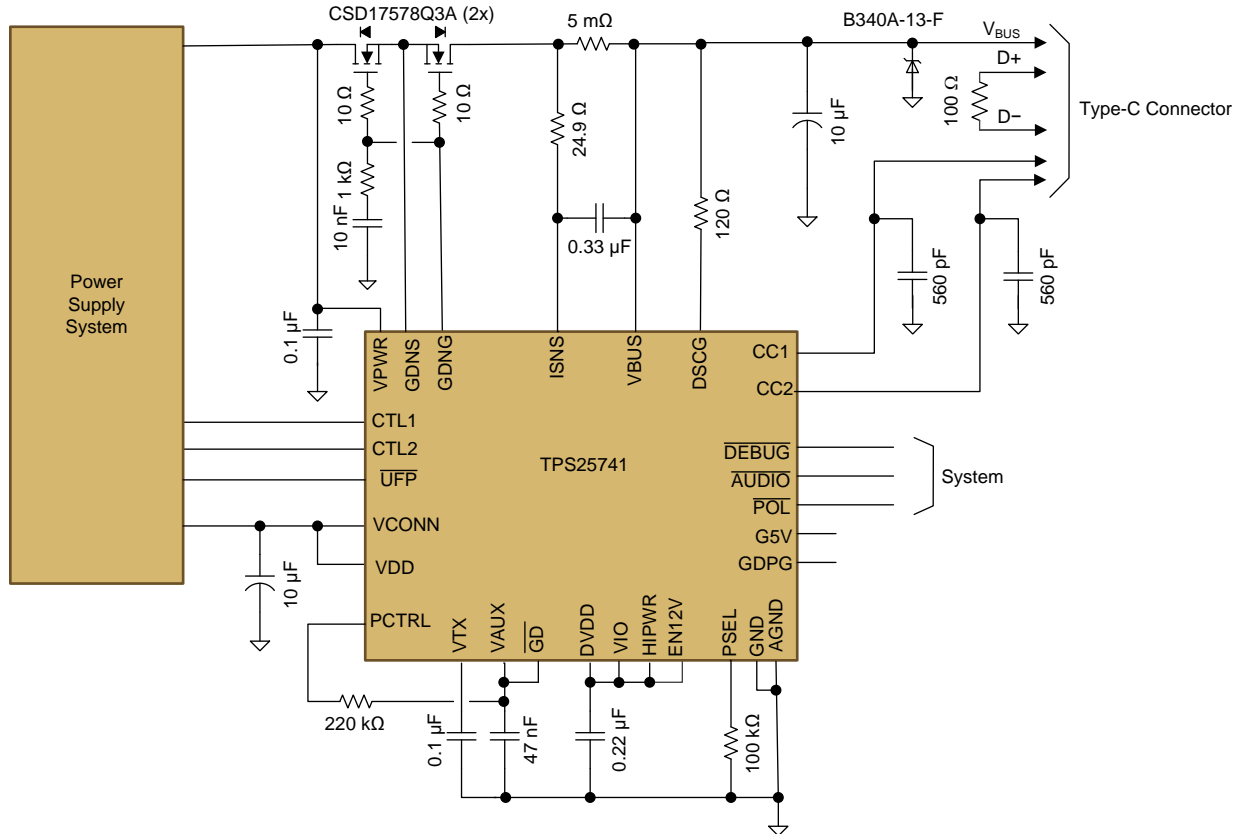
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Figure 1. Adapter-Like Application Architecture

However, in complex applications like desktops where two voltages already exist in the system, a new architecture is proposed in Figure 2. In such a system, 5 V and 12 V already exist for other circuits. The TPS25741 can multiplex either one of them onto VBUS, based on different sink requests. This architecture is called power multiplexing. BOM cost and PCB size are reduced because the dedicated USB port DC-DC is not required.
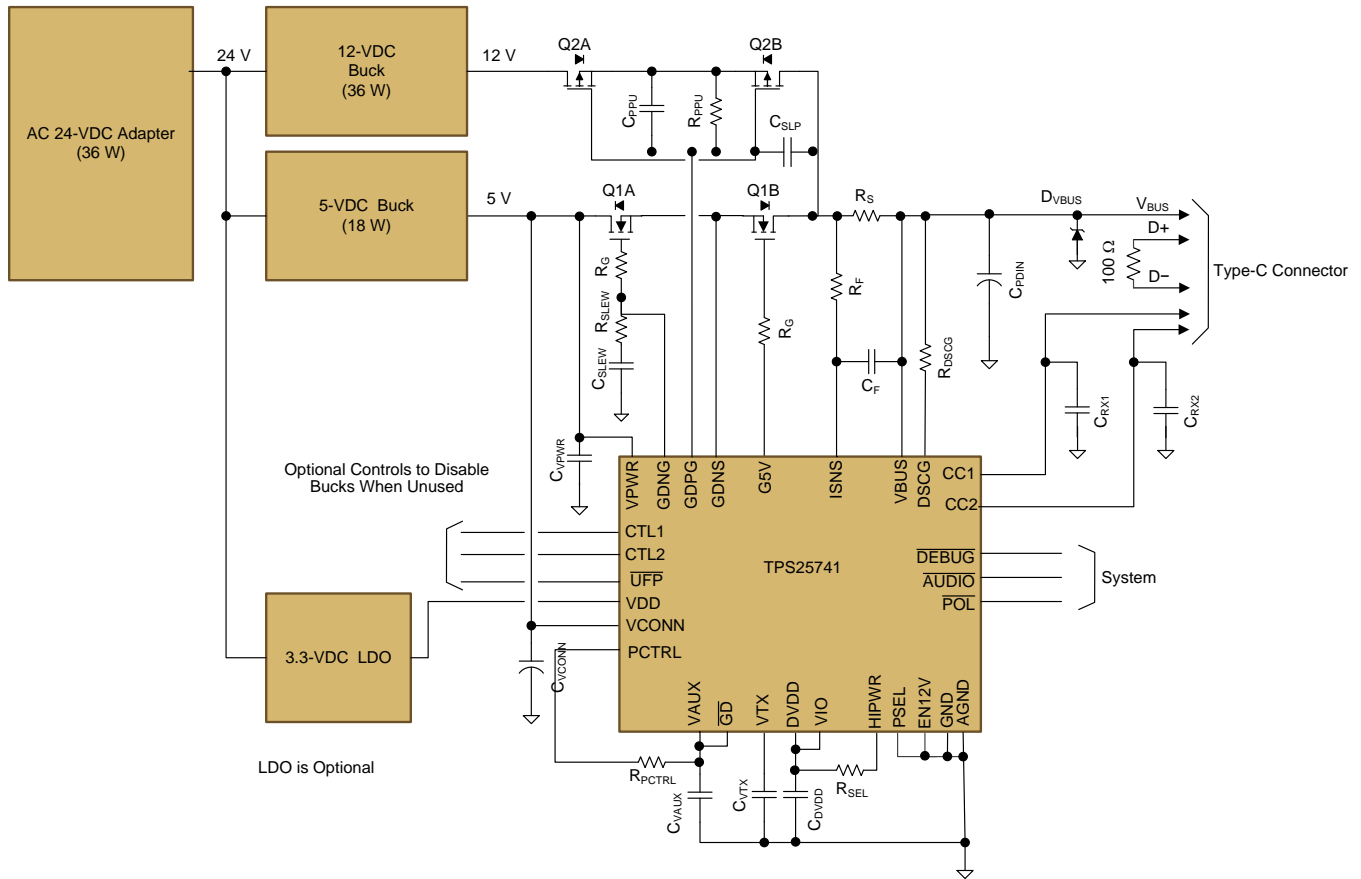
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Figure 2. Desktop-Like Application Architecture: Power Multiplexing

2 Power Multiplexing Design Consideration

2.1 *Power Multiplexing Risks*

During the multiplexing between two rails, the voltage transition on VBUS should follow the USB Power Delivery Specification[2]. The two specifications that are commonly violated, if the multiplexing is not properly handled are:

- During voltage transition, the voltage on the VBUS should not drop below vSrcValid(min), which is 4.25 V, according to the PD specification.
- During voltage transition, the slew rate should not exceed vSrcSlewPos (vSrcSlewNeg), which is 30 mV/µs according to the PD specification.

The two rules are applied to both positive and negative transitions.

The other consideration is that during the negative voltage transition, timing should be strictly controlled to make sure that no high voltage leaks back to the 5-V DC-DC output. If not, upstream circuits including DC-DCs may be damaged by this high voltage because they may be rated for 5 V only.
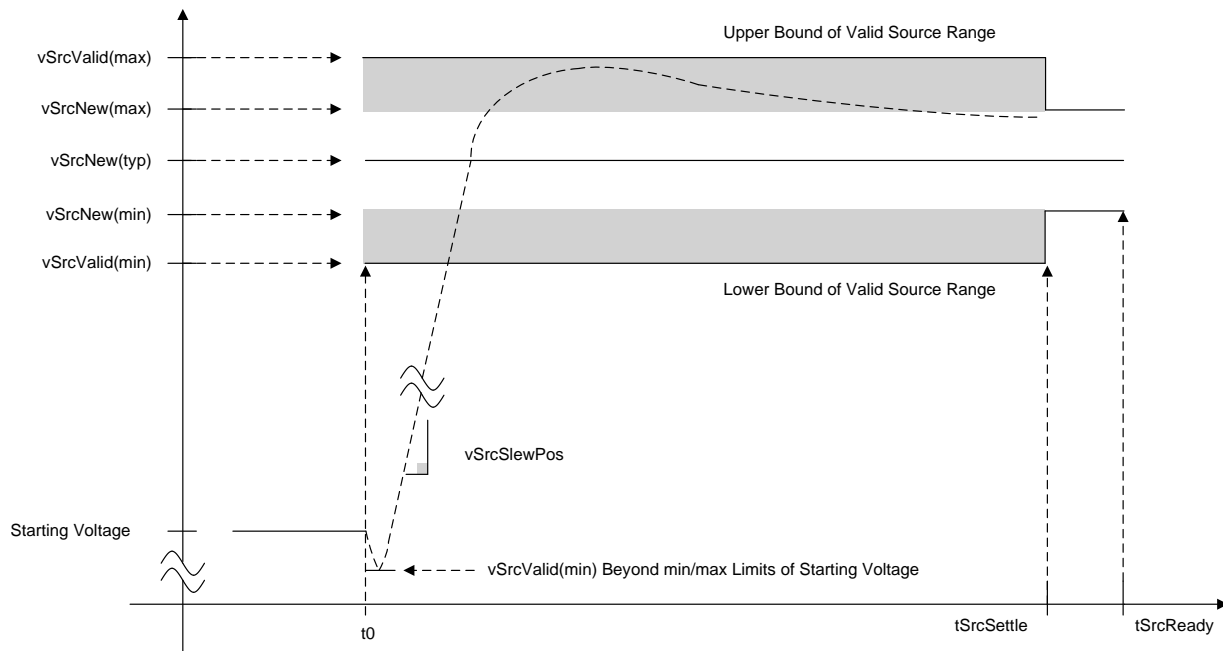
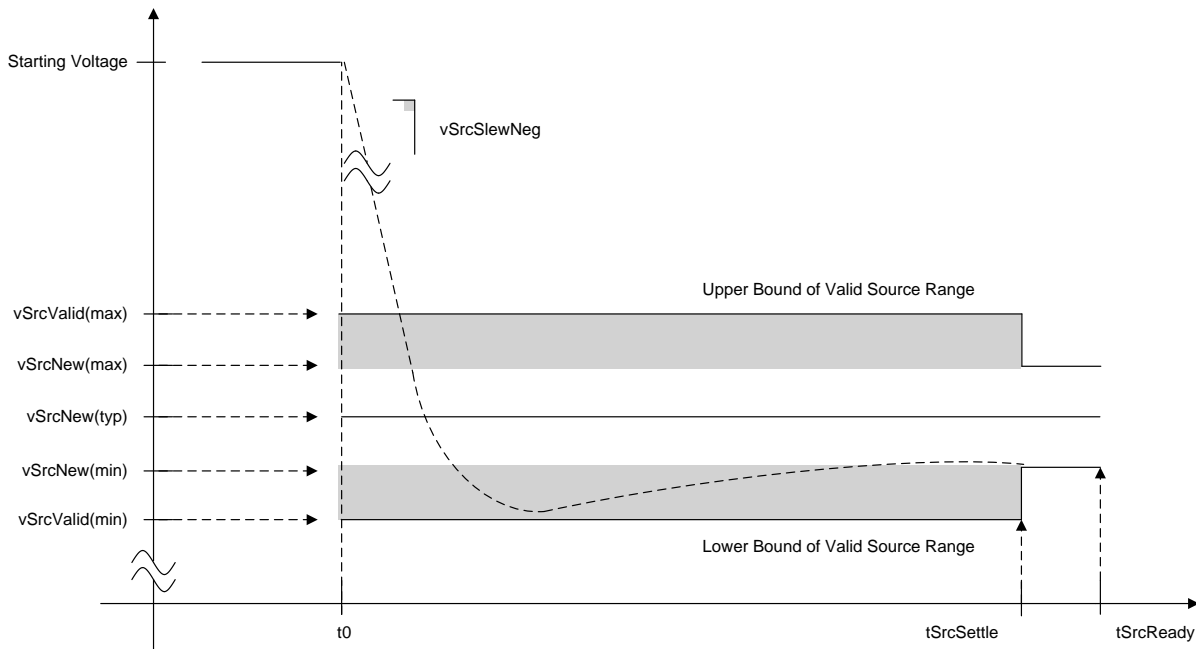**Figure 3. PD Specification on Positive Voltage Transition**

Figure 4. PD Specification on Negative Voltage Transition

2.2 Power Multiplexing With the TPS25741

The TPS25741 adopts a special timing control scheme to make sure the system follows the PD specification and operates safely during power multiplexing with minimum external circuits as Figure 4 shows.

The TPS25741 has 2 N-FET gate drivers to Q1A and Q1B, and one P-FET gate driver to control Q2A and Q2B. Q1 and Q2 are all open when no valid sink is attached. When a 5-V contract is made, Q1A/Q1B are turned on and Q2A/Q2B remain open. So 5 V is applied onto VBUS. When a 12-V contract is made, Q1A remains closed while Q1B is turned off (by the G5V pin). After Q1B is open, then Q2A/Q2B is turned on (by the GDPG pin) applying 12 V onto VBUS. During the dead time between Q1B open and Q2 closed, 5-V current is sourced onto VBUS through the body diode of Q1B so that the voltage drop is small. If the voltage drop must be smaller, then an external Schottky (DQ1B) can be added in parallel with Q1B to achieve minimum voltage drop above vSrcValid(min), which is 4.25 V, according to the USB Power Delivery Specification[2].
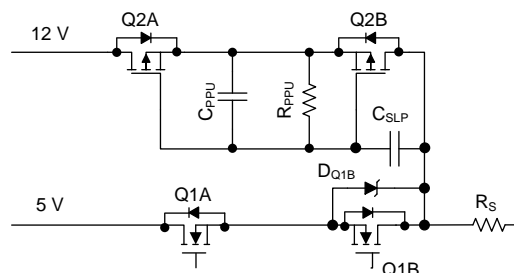
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Figure 5. Implementing Power Multiplexing

When a 5-V contract is made again, VBUS will have a negative transition from 12 V to 5 V. In order to apply 5 V onto VBUS, Q2 should be turned off first and then Q1B should be turned on. However, Q2 requires more time to be turned off than the turn-on time for Q1B. As a result, there is a chance that Q2 is not completely off before Q1B turns on. For this case, 12 V can leak back to the 5-V rail, potentially damaging upstream devices.

The TPS25741 can eliminate the problem by perfectly handling the negative transition. The TPS25741 continuously monitors the voltage on VBUS and only turns on Q1B after VBUS drops below V_{SOVP}, which is 5.65 V. Compared with competitor solutions, such control topology ensures safe operation of power multiplexing with minimum external components.

2.3 Problem Description

With the timing control scheme described in the previous section, the TPS25741 makes sure that system operates properly and safely. As is shown in Figure 6, according to the PD specification, the source bulk capacitance can be as large as 10 µF, and the bulk capacitance on VBUS, a sink is allowed after a successful negotiation is up to 100 µF. It means there could be 110-µF capacitor on the VBUS during the transition.
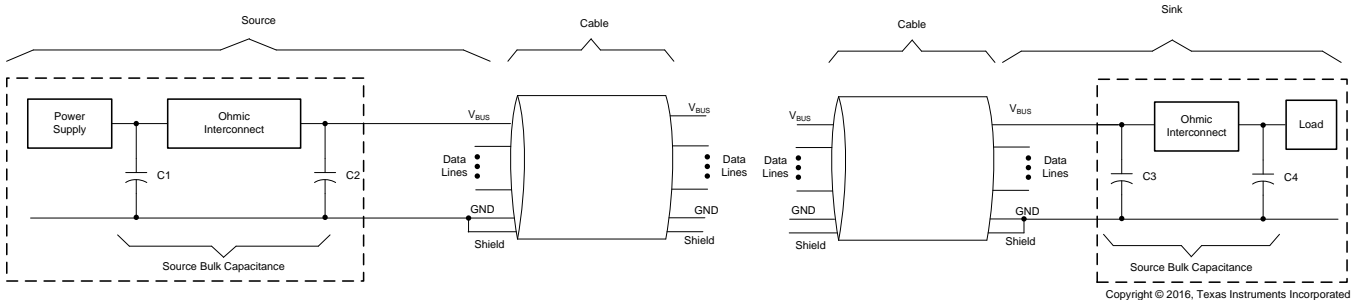

Figure 6. Bulk Capacitor on the VBUS

The larger the capacitor is, the larger the inrush current. When the inrush current goes above the OCP threshold of the TPS25741, gate drivers are shut down. Figure 7 shows when VBUS bulk capacitance is 110 µF, the system will hit OCP protection during positive voltage transition.
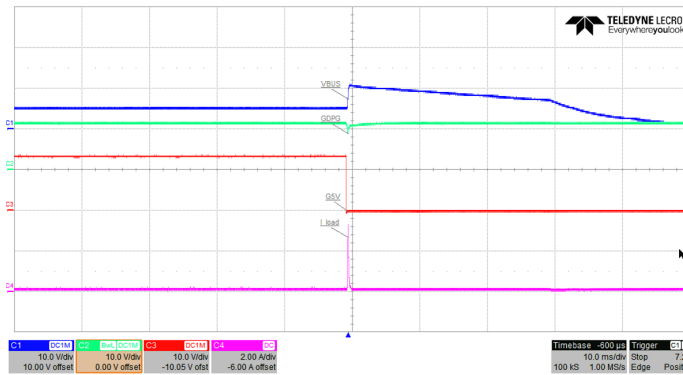

Figure 7. Large In-Rush Current Causes OCP

In order to resist inrush current and also maintain the slew rate within 30 mV/µs, the turn-on time of P-FETs should be slowed down by adding slew rate circuits. Conversely, if the turn-on behavior gets slowed down by slew rate circuits, so does the turn-off behavior, as Figure 8 shows. However, when it comes to fault conditions like short circuits, OVP, OCP, P-FETs are usually expected to be turned off very fast in order to protect the system. With the slew rate control circuits, it may not be practical to make P-FETs turn off fast enough. In order to solve this issue, a solution is proposed in Section 2.4 to show how to achieve slow turn-on during positive voltage transition and fast turn-off after faults happen.
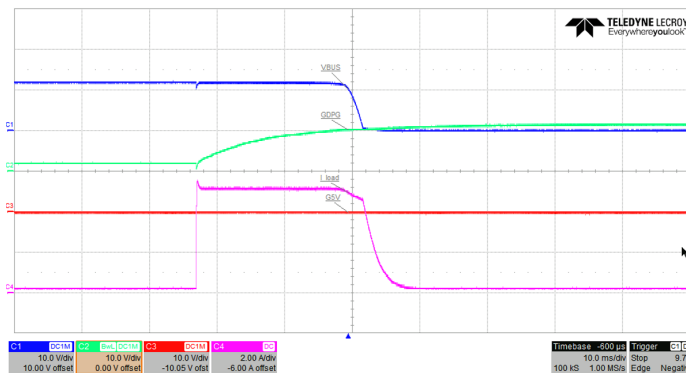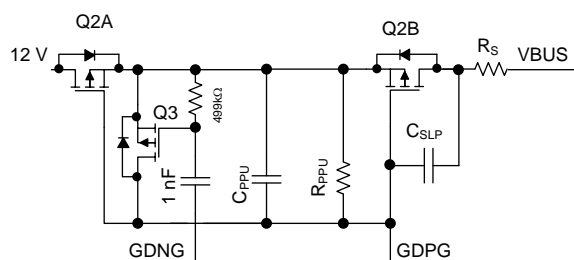
Figure 8. Slew Rate Circuits Cause Delay of Protection

2.4 Solution

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Figure 9. Solution to Achieve Slow Turn-On and Fast Turn-Off

R_{PPU}: R_{PPU} is the Q2 gate-drive pullup resistor. The TPS25741 applies a sink current of 40 mA typical to turn on Q2 and R_{PPU} should be large enough to fully enhance Q2 but not too large as it also discharges C_{SLP} during turn off. The CSD25404Q3 lists an acceptable $R_{DS(on)}$ with V_{GS} = −4.5 V and ID = −10 A. Using $I_{GMV(min)}$ = 34 mA and V_{GS} = −4.5 V yields R_{PPU} = 132 kΩ. Use a standard 1% resistor = 133-kΩ resistor for R_{PPU}.

C_{SLP}: C_{SLP} provides slew rate and inrush current limiting from the 12-V supply during VBUS transition from 5 V to 12 V. While the sink is attached, there could be as much as 110 µF on VBUS. The slew time must be > 233 µs and the inrush current must be < 3.85 A ($V_{ITRIP(min)}$ / R_S). For this design, target an inrush current of 2 A during 5- to 12-V slew. The charge rate across C_{SLP} is the same as for the 110-µF load capacitor such that I_{LOAD} / C_{LOAD} = I_{CSLP} / C_{SLP}. Using the CSD25404Q3 gate charge curve, a plateau threshold voltage of V_{PTH} at approximately 1.8 V can be used to calculate C_{SLP} with the following equations.

$$C_{SLP} = C_{LOAD} \times \frac{I_{CSLP}}{I_{LOAD}} = C_{LOAD} \times \frac{I_{GDPG} - \frac{V_{PTH}}{R_{PPU}}}{I_{LOAD}}$$

where

- C_{LOAD} = 110 µF
- I_{GDPG} = 40 µA
- V_{PTH} = 1.8 V
- R_{PPU} = 133 kΩ
- I_{LOAD} = 2 A

$$\tag{1}$$

$$C_{SLP} = 110\ \mu F \times \frac{40\ \mu A - \frac{1.8\ V}{133\ k\Omega}}{2A} = 1.46\ nF$$

$$\tag{2}$$

$$\text{Choose} \, C_{SLP} = 1.5 \, \text{nF} \tag{3}$$

$$\text{Slew time} = C_{SLP} \times \frac{12 \, \text{V} - 5 \, \text{V}}{I_{GDPG} - \dfrac{V_{PTH}}{R_{PPU}}} = 1.5 \, \text{nF} \times \frac{7 \, \text{V}}{40 \, \mu\text{A} - \dfrac{1.8 \, \text{V}}{133 \, \text{k}\Omega}} = 397 \, \mu\text{s} \tag{4}$$

C$_{PPU}$: C_{PPU} contributes a small Q2 turn-on delay just prior to the 5- to 12-V transition, but the primary function is to inhibit Q2 output turn on during ramp up of the 12-V power supply. When the 12-V power supply is OFF, C_{SLP} is discharged. As the 12-V power supply ramps up, the common sources of Q2 rise and C_{SLP} is charged through R_{PPU}. C_{PPU} is required to prevent Q2 V_{GS} from exceeding the turn-on threshold and prematurely charging VBUS for the case where the 12-V bus ramps up quickly. C_{PPU} and C_{SLP} form a capacitive divider network with $V_{GS(th)} \gg 12 \, \text{V} \times C_{SLP} / (C_{SLP} + C_{PPU})$. Choose $C_{PPU} \gg (12 \, \text{V} / V_{GS(th)} - 1) \times C_{SLP}$. For this example, $V_{GS(th)} = 0.9 \, \text{V}$ and $C_{PPU} = 18 \, \text{nF}$. If the 12-V power supply is enabled while the 5-V supply is on, then C_{PPU} can be smaller, set by the voltage difference between the 12- and 5-V supply. Always validate the final design on the test bench.

For faster fault turn off, Q3 can be connected as shown and triggered using the GDNG pin. Whenever a fault happens, the TPS25741 pulls GDNG to 0 V. With a small capacitor in series between the gate of Q3 and GDNG, the gate of Q3 is pulled down by GDNG; therefore, Q3 is closed and shorts the GS of Q2, resulting in a fast shut-off of Q2.

Note that such circuits can also be applied to 5- to 20-V transition applications, and Q3 must have a ±20 V $V_{GS(max)}$ rating for 20-V multiplexing applications.

3   Testing

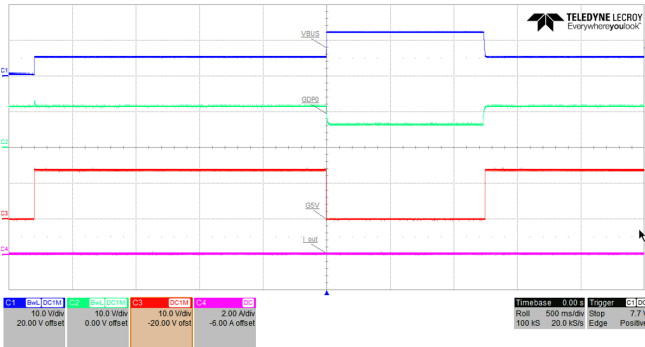Figure 10 through Figure 17 illustrate the test results for this report.

Figure 10. Mux Between 5 V and 12 V at No Load
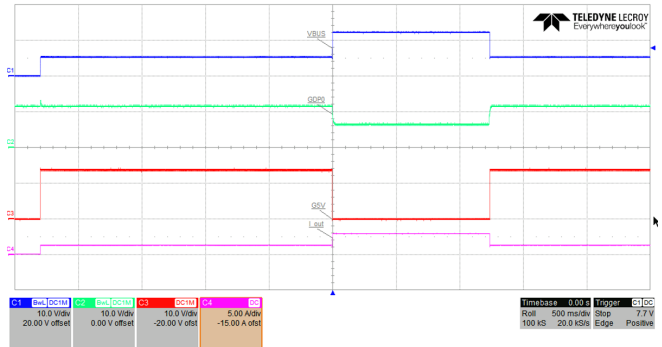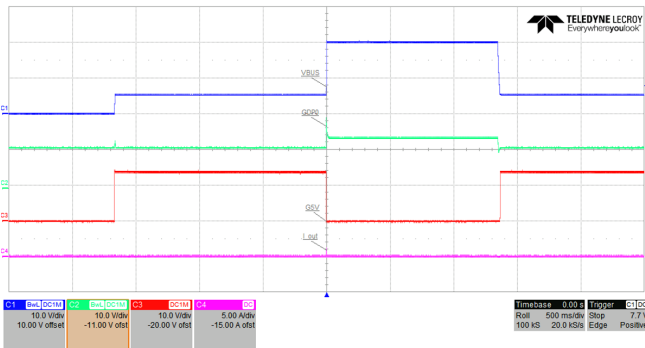

Figure 11. Mux Between 5 V and 12 V at 3 A

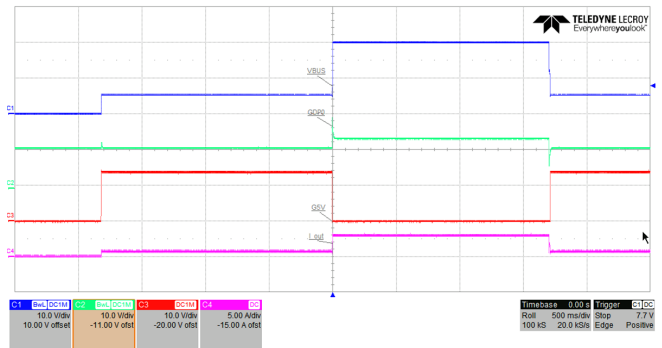
Figure 12. Mux Between 5 V and 20 V at No Load

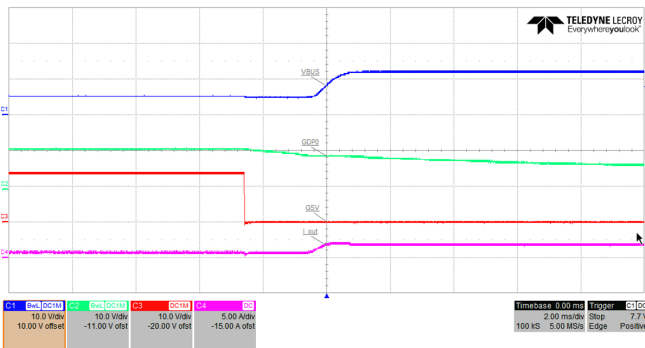
Figure 13. Mux Between 5 V and 20 V at 3 A

Figure 14. 5- to 12-V Transition
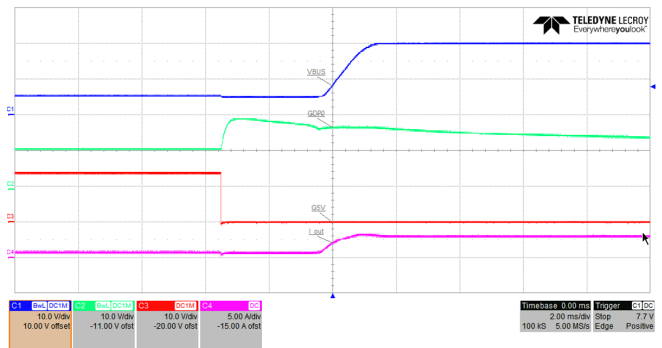
Figure 15. 5- to 20-V Transition
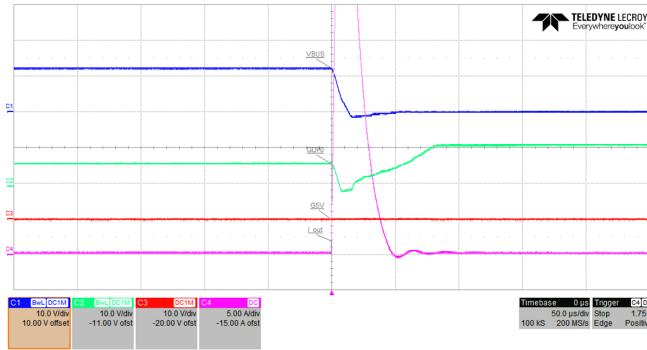
Figure 16. Hot Short on Output 12 V
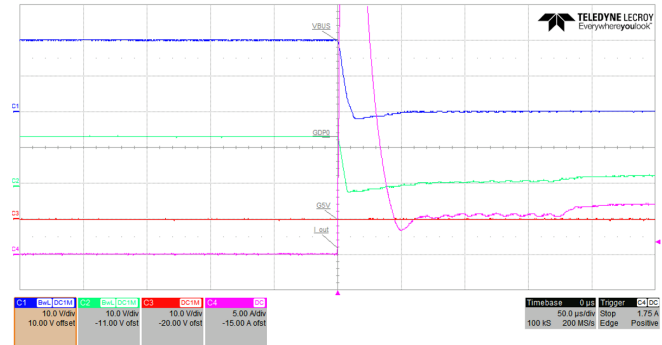
Figure 17. Hot Short on Output 20 V

4   Conclusion

The guidelines in this application report describe how the TPS25741 handles power multiplexing to make sure the system operates safely and follows the USB Power Delivery Specification. It also provides a solution to achieve a slow turn-on of PFETs to resist inrush current during positive voltage transition while achieving fast shut-down during fault conditions.

5   References

1. *TPS25741, TPS25741A USB Type-C™ and USB Power Delivery Host Port Controllers*, data sheet (SLVSDJ5)
2. USB Power Delivery Specification Rev. 2.0 (part of USB 3.1 download)
3. *TPS25741EVM-802 and TPS25741AEVM-802 EVM User's Guide for Desktops* (SLVUAS7)

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