User's Guide
SLVU387–July 2010

TPS7A80xxDRBEVM

This user's guide describes the characteristics, operation, and use of the TPS7A8001DRBEVM (HPA562). This evaluation module (EVM) demonstrates the Texas Instruments TPS7A8001 Low-Dropout (LDO) linear regulators in a 3-mm x 3-mm, SON-8 package which is capable of a 1-A output current. This user's guide includes setup instructions, a schematic diagram, thermal guidelines, a bill of materials, and printed-circuit board layout drawings for the evaluation module.

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1 Introduction

The TPS7A8001DRBEVM evaluation module (EVM) helps designers evaluate the operation and performance of the TPS7A8001 adjustable output LDO. Because the TPS7A8001 is adjustable, the EVM has been designed to provide several common output voltages which can be selected using an onboard jumper. The EVM can provide output voltages of 1.8, 2.5, 2.8 or 3.3 V using the jumper. Other output voltage can be evaluated but requires changing the feedback resistors.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS7A8001DRBEVM.

2.1 Input/Output Connector Descriptions

2.1.1 J1 – VIN

This is the positive input supply voltage. The connector for J1 is not populated on the TPS7A8001DRBEVM. This footprint allows the mounting of an SMA-style connector for more accurate PSRR measurements. See the bill of materials (BOM) for the manufacturer and part number of the corresponding connector.

2.1.2 J2 – VOUT

This is the output voltage. The connector for J2 is not populated on the TPS7A8001DRBEVM. This footprint allows the mounting of an SMA-style connector for more accurate PSRR measurements. See the BOM for the manufacturer and part number of the corresponding connector.

2.1.3 J3 – VIN and GND

Pin 1: This is the positive input supply voltage. Twist the leads to the input supply and keep them as short as possible to minimize EMI transmission. Additional bulk capacitance must be added between pins 1 and 2 if the supply leads are greater than six inches. An additional 47-µF or greater capacitor improves the transient response of the TPS7A8001DRB and helps to reduce ringing on the input when long supply wires are used.

Pin 2: This is the input supply return (GND).

2.1.4 J4 – VOUT and GND

Pin 1: This is the positive output voltage.

Pin 2: This is the output voltage return (GND).

2.1.5 J5 – ENABLE

This jumper is used to enable or disable the output of the TPS7A8001DRB. Placing a shorting jumper between pins 1 and 2 (*ON* position) enables the TPS7A8001DRB. Placing the shorting jumper between pins 2 and 3 (*OFF* position) disables the TPS7A8001DRB.

2.1.6 J6 – Output Voltage Select

This jumper is used to set the desired output voltage from the TPS7A8001DRB. Placing a shorting jumper between the appropriate pins gives the corresponding outputs. The output voltage of the TPS7A8001DRBEVM must only be changed when the TPS7A8001DRBEVM is not powered. Installing and removing the jumper with the board powered can lead to undesired or unregulated output voltages.

Short Pins	VOUT (V)
1 and 2	3.3
3 and 4	2.8
5 and 6	2.5
7 and 8	1.8

2.2 Fixed Output Voltage Versions

2.2.1 Evaluating Fixed Voltage Version Devices

The TPS7A8001DRBEVM is supplied with the adjustable voltage version of the TPS7A80xx. The board can be used to evaluate fixed voltage versions of the TPS7A80xx as well. The integrated circuit (IC) must be changed to the desired fixed output voltage version of the device. Remove any jumper on J6. Install a 0-Ω resistor or shorting wire in location R1. R6 is not needed for the fixed output versions and can be removed optionally to reduce quiescent current.

3 Operation

This section provides information about the operation of the TPS7A8001DRBEVM.

3.1 Operation

Ensure that the input power supply is off. Connect the positive input power supply to J3 pin 1. Connect the input power return (ground) to J3 pin 2. The TPS7A8001DRB has an absolute maximum input voltage of 7 V. The recommended maximum operating voltage is 6.5 V. The actual highest input voltage may be less than 6.5 V due to thermal conditions. See the Thermal Considerations section of this manual to determine the highest input voltage.

Connect the desired load between J4 pin 1 (positive lead) and J4 pin 2 (negative or return lead). Configure jumper J6 for the desired output voltage. Turn on the input power supply.

4 Thermal Guidelines

This section provides guidelines for the thermal management of the TPS7A8001DRBEVM board.

4.1 Thermal Considerations

Thermal management is a key design component of any power converter and is especially important when the power dissipation in the LDO is high. To better help you design the TPS7A8001DRB family into your application, use Equation 1 to approximate the maximum power dissipation at a particular ambient temperature:

$$T_J = T_A + P_d \times \theta_{JA} \quad (1)$$

where T_J is the junction temperature, T_A is the ambient temperature, P_d is the power dissipation in the IC and θ_{JA} is the thermal resistance from junction to ambient. All temperatures are in degrees Celsius.

The measured thermal resistance from junction to ambient for the TPS7A8001EVM has a typical value of 52°C/W. The recommended maximum operating junction temperature specified in the data sheet for the TPS7A8001 family is 125°C. With these two pieces of information, the maximum power dissipation can be found by using Equation 1.

Table 1 shows the maximum input voltage that can be applied to the input of the TPS7A8001DRBEVM and still provide the full 1 A of output current. Table 1 shows the input voltage versus the output voltage setting and two ambient temperatures (25°C and 85°C). The maximum input voltage shown provides the rated output current while keeping the junction temperature at or below the recommended 125°C.

Table 1. Maximum Input Voltage vs Ambient Temperature and Output Voltage

		Selected Output Voltage (V)			
Ambient Temp	**Iout (A)**	**1.8**	**2.5**	**2.8**	**3.3**
25	1.00	3.72	4.42	4.72	5.22
85	1.00	2.57	3.27	3.57	4.07

5 Board Layout

5.1 Layout

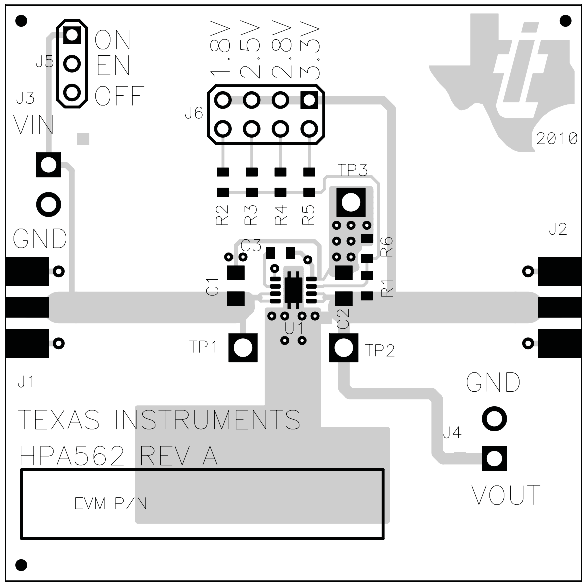

Figure 1. Top Layer Assembly

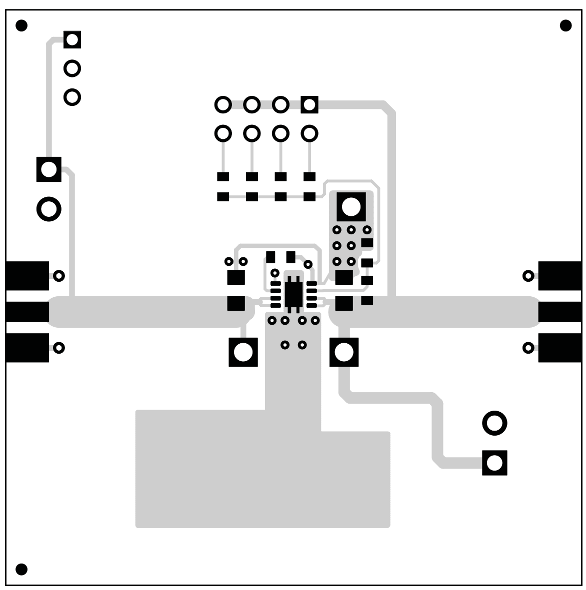

Figure 2. Top Layer Routing

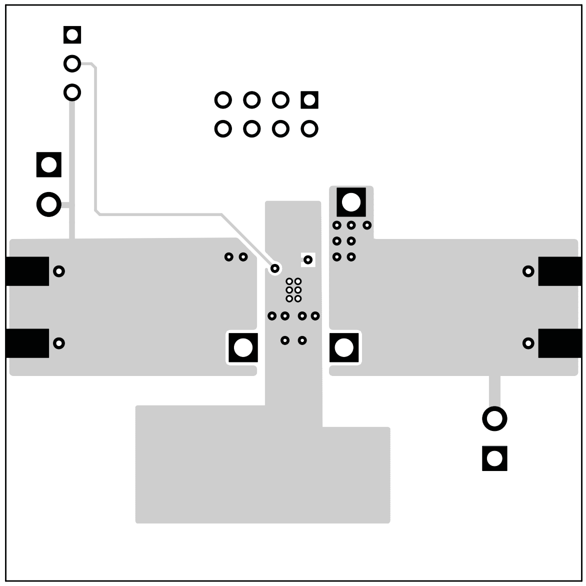

Figure 3. Bottom Layer Routing

6 Schematic and Bill of Materials

This section provides the TPS7A8001DRBEVM board schematic and BOM.

6.1 Schematic

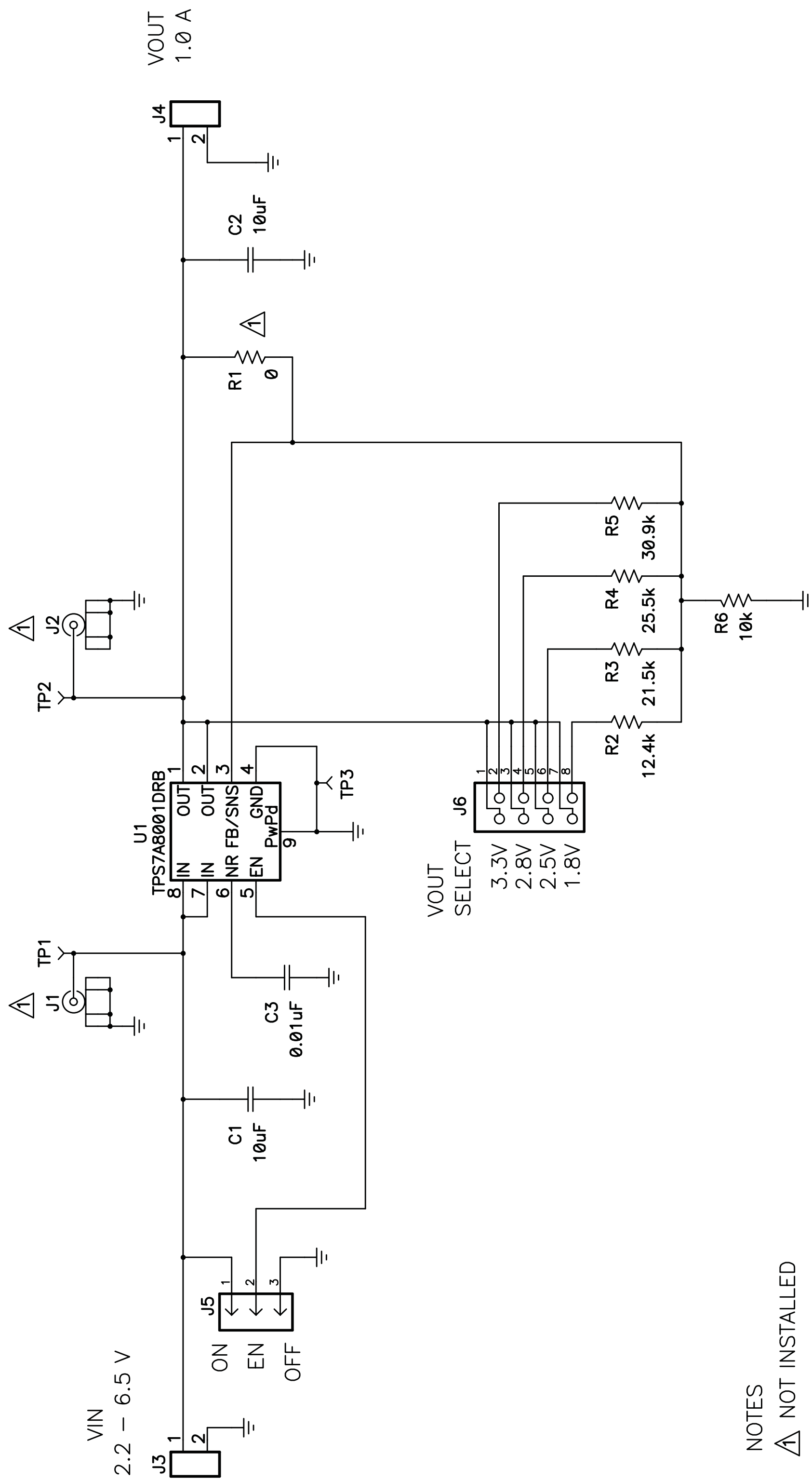

Figure 4. TPS7A8001DRBEVM Schematic

6.2 Bill of Materials

Table 2. Bill of Materials

Count	RefDes	Value	Description	Size	Part No.	MFR
2	C1, C2	10µF	Capacitor, Ceramic, 10V, X7R, 10%	0805	Std	Std
1	C3	0.01µF	Capacitor, Ceramic, 16V, X7R, 10%	0603	Std	Std
0	J1, J2	142-0711-821	CONNECTOR, SHIELDED, END LAUNCH JACK, GOLD PLATED, FOR 0.062 PCB, EDGE MOUNTED	0.250 SQ	142-0711-821	STD
2	J3, J4	ED550/2DS	Terminal Block, RA 2-pin, 6-A, 3.5mm	7.0 x 8.2 mm	ED550/2DS	OST
1	J5	PEC03SAAN	Header, Male 3-pin, 100mil spacing	0.100 inch x 3	PEC03SAAN	Sullins
1	J6	PEC04DAAN	Header, Male 2x4-pin, 100mil spacing	0.20 x 0.40 inch	PEC04DAAN	Sullins
0	R1	0	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R2	12.4k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R3	21.5k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R4	25.5k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R5	30.9k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	R6	10k	Resistor, Chip, 1/16W, 1%	0603	Std	Std
1	TP1	5010	Test Point, Red, Thru Hole	0.125 x 0.125 inch	5010	Keystone
1	TP2	5013	Test Point, Orange, Thru Hole	0.125 x 0.125 inch	5013	Keystone
1	TP3	5011	Test Point, Black, Thru Hole	0.125 x 0.125 inch	5011	Keystone
1	U1	TPS7A8001DRB	IC, Low Noise, High-Bandwidth PSRR LDO 1A Linear Regulator	DRB-8	TPS7A8001DRB	TI
1	–		PCB, 2 In x 2 In x 0.62 In		HPA562	Any
2		15-29-1025	Shunt, 2 pos 0.100 In Gold		15-29-1025	Molex

Notes: 1. These assemblies are ESD sensitive, ESD precautions shall be observed.

2. These assemblies must be clean and free from flux and all contaminants. Using unclean flux is unacceptable.

3. These assemblies must comply with workmanship standards IPC-A-610 Class 2.

4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 2.2 V to 6.5 V and the output voltage range of 0.8 V to 6 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 85° C. The EVM is designed to operate properly with certain components above 85° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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