TPS650380EVM-054

This user's guide describes the characteristics, operation, and use of the Texas Instruments TPS650380EVM-054 (PWR054-001) evaluation module (EVM). This EVM is designed to help the user evaluate and test the operation and functionality of the TPS650380. The EVM converts a 2.5-V to 5.5-V input voltage to 3 regulated output voltages that deliver 5 A, 2 A, and 1.8 A. The 5-A output operates 3 phases, the 2-A output operates 2 phases, and the 1.8-A output operates a single phase. The output voltages are programmable via the I²C™ interfaces in 10-mV steps between 0.5 V and 1.77 V. This user's guide includes setup instructions for the hardware, printed-circuit board layouts for the EVM, a schematic diagram, a bill of materials, and test results for the EVM.

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1 Introduction

1.1 Requirements

To operate this EVM, connect and properly configure the following components:

A personal computer (PC) with a USB port is required to operate this EVM. The TPS650380 interface software runs on the PC and communicates with the EVM via the PC's USB port. Commands can be sent to the internal registers of the TPS650380 through the USB port. The software has been tested with the PC requirements listed below. It may work with other operating systems and configurations, but this has not been verified.

Personal Computer Requirements

- Windows XP™ operating system
- .NET 2.0 or higher
- USB port
- 10 MB of free hard disk space
- 512 MB of RAM

USB-TO-GPIO Adapter

The USB-TO-GPIO adapter is the link that allows the PC and the EVM to communicate. One end of the USB-TO-GPIO adapter connects to the PC with the supplied USB cable. The other end of the USB-TO-GPIO adapter connects to the EVM with the supplied ribbon cable.

When a command is written to the EVM, the interface program running on the PC sends the commands to the PC USB port. The USB-TO-GPIO adapter receives the USB command, converts the signal to an I^2C protocol, and sends the I^2C signal to the TPS650380 EVM board.

Software

Texas Instruments provides software to assist in evaluating this EVM. This software can be downloaded from the TPS650380EVM-054 Product Page, located at: http://focus.ti.com/docs/toolsw/folders/print/TPS650380EVM-054.html.

Printed-Circuit Board Assembly

The board contains the TPS650380 IC and the required external components to evaluate it as a processor power supply solution.

1.2 Performance Specification Summary

A summary of the performance specifications is provided in Table 1. Specifications are given for an input voltage of 3.6 V and an output voltage of 0.96 V, unless otherwise specified. The TPS650380 is designed and tested for V_{IN} = 2.5 V to 5.5 V. The ambient temperature is 25°C for all measurements and the default register settings are used, unless otherwise noted.

Table 1. Performance Specification Summary

SPECIFICATION	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN} voltage range			2.5	3.6	5.5	V
Output voltage set point - each output rail	Programmable in 10 mV steps		0.5		1.77	V
Output current range - DCDC_A			0		5	A
Output current range - DCDC_B			0		2	A
Output current range - DCDC_C			0		1.8	A
Line regulation - each output rail	I_{OUTA} = 3.4A, I_{OUTB} = 1.85A, I_{OUTC} = 0.9A, DCDC_A = DCDC_B = DCDC_C = 0.96V			±0.15%		
Load regulation - DCDC_A	V_{IN} = 3.6V, DCDC_A = 0.96V, FPWM_A = 0			+0.65% / –0.15%		
Load transient response - DCDC_A	I_{OUTA} = 3A to 5A	Voltage change		50		mV
		Recovery time		4		µs
	I_{OUTA} = 5A to 3A	Voltage change		50		mV
		Recovery time		3		µs
Input ripple voltage - DCDC_A	V_{IN} = 3.6V, DCDC_A = 0.96V, I_{OUTA} = 5A, DCDC_B and DCDC_C disabled, measured across C13			35		mV_{PP}
Output ripple voltage - DCDC_A	V_{IN} = 3.6V, DCDC_A = 0.96V, I_{OUTA} = 5A, DCDC_B and DCDC_C disabled, measured across C6			14		mV_{PP}
Maximum efficiency - DCDC_A	V_{IN} = 3.6V, DCDC_A = 0.96V, I_{OUT} = 200mA			90.1%		

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up, and use the TPS650380EVM-054 (PWR054-001).

2.1 Connector and Jumper Descriptions

2.1.1 J1 – V_{IN}

This header is for the positive input supply voltage to the converter. Connect the input supply at this point if the input current remains below 1 A. If the input current will exceed 1A, use terminal block J16 instead. The leads to the input supply should be twisted and kept as short as possible to minimize EMI transmission and reduce inductive voltage droop during a load transient event. This voltage should be between 2.5 V and 5.5 V.

2.1.2 J2 – S+ and S-

Sense connector for V_{IN}. Connect input supply's sense leads to this point. Monitor the V_{IN} voltage at this point.

2.1.3 J3 – GND

This is the return connection for the input power supply of the converter. Connect the input supply at this point if the input current remains below 1 A. If the input current will exceed 1A, use terminal block J16 instead. The leads to the input supply should be twisted and kept as short as possible to minimize EMI transmission and reduce inductive voltage droop during a load transient event.

2.1.4 J4 – DCDC_A Output Voltage

This header connects to the DCDC_A output voltage. Connect the load (processor) at this point if the load current remains below 1 A. If the load current will exceed 1A, use terminal block J17 instead. The leads to the load should be twisted and kept as short as possible to minimize EMI transmission and reduce inductive voltage droop during a load transient event.

2.1.5 J5 – FB_A+ and FB_A-

Remote sense connector for the DCDC_A output voltage. As shipped, the EVM is configured for local sensing of the output voltage. If output voltage sensing at the load (remote sensing) is desired, see the Remote Sense Resistors section. This is a high impedance connection back to the TPS650380's remote sense inputs. Monitor the output voltage at this point.

2.1.6 J6 – GND

This is the return connection for the DCDC_A load. If the load current will exceed 1 A, do not use headers J4 and J6, but use terminal block J17 instead. The leads to the load should be twisted and kept as short as possible to minimize EMI transmission and reduce inductive voltage droop during a load transient event.

2.1.7 J7 – DCDC_B Output Voltage

This header connects to the DCDC_B output voltage. Connect the load (processor) at this point if the load current remains below 1 A. If the load current will exceed 1A, use terminal block J18 instead. The leads to the load should be twisted and kept as short as possible to minimize EMI transmission and reduce inductive voltage droop during a load transient event.

2.1.8 J8 – FB_B+ and FB_B-

Remote sense connector for the DCDC_B output voltage. As shipped, the EVM is configured for local sensing of the output voltage. If output voltage sensing at the load (remote sensing) is desired, see the Remote Sense Resistors section. This is a high impedance connection back to the TPS650380's remote sense inputs. Monitor the output voltage at this point.

2.1.9 J9 – GND

This is the return connection for the DCDC_B load. If the load current will exceed 1 A, do not use headers J4 and J6, but use terminal block J18 instead. The leads to the load should be twisted and kept as short as possible to minimize EMI transmission and reduce inductive voltage droop during a load transient event.

2.1.10 J10 – DCDC_C Output Voltage

This header connects to the DCDC_C output voltage. Connect the load (processor) at this point. The leads to the load should be twisted and kept as short as possible to minimize EMI transmission and reduce inductive voltage droop during a load transient event.

2.1.11 J11 – FB_C+ and S-

Pin 1 is the remote sense connector for the DCDC_C output voltage. As shipped, the EVM is configured for local sensing of the output voltage. If output voltage sensing at the load (remote sensing) is desired, see the Remote Sense Resistors section. This is a high impedance connection back to the TPS650380's remote sense input. Pin 2 is used for monitoring the DCDC_C voltage and is not required to be connected at the load. Monitor the output voltage at these points.

2.1.12 J12 – GND

This is the return connection for the DCDC_C load. The leads to the load should be twisted and kept as short as possible to minimize EMI transmission and reduce inductive voltage droop during a load transient event.

2.1.13 J13 – VDD

This header is used to provide the V_{DD} voltage (between 1.2 and 3.6 V) to the EVM if JP2 is not installed. If JP2 is installed, the V_{DD} voltage may be monitored at this header.

2.1.14 J14 – GND

This header is used to monitor the V_{DD} voltage if JP2 is installed. If JP2 is not installed, this header is the connection for the return connection of the applied V_{DD} voltage.

2.1.15 J15 – INT Pin Output

This header provides the INT pin output on pin 1 with a convenient ground reference on pin 2.

2.1.16 J16 – V_{IN} and GND Terminal Block

This terminal block is used instead of J1 or J3 when the input current exceeds 1 A. The leads to the input supply should be twisted and kept as short as possible to minimize EMI transmission and reduce inductive voltage droop during a load transient event. This voltage should be between 2.5 V and 5.5 V.

2.1.17 J17 – DCDC_A and GND Terminal Block

This terminal block is used, instead of J4 or J6, to connect to the load (processor) when the load current exceeds 1 A. The leads to the load should be twisted and kept as short as possible to minimize EMI transmission and reduce inductive voltage droop during a load transient event.

2.1.18 J18 – DCDC_B and GND Terminal Block

This terminal block is used, instead of J7 or J9, to connect to the load (processor) when the load current exceeds 1 A. The leads to the load should be twisted and kept as short as possible to minimize EMI transmission and reduce inductive voltage droop during a load transient event.

2.1.19 J19 – SYS I^2C Connection from USB-TO-GPIO Adaptor

This connects the USB-TO-GPIO adaptor to the SYS I^2C connection of the TPS650380. It provides the I^2C signals and a 3.3 V supply for powering V_{DD}. This connector is keyed to prevent incorrect installation. **Only install a USB-TO-GPIO adaptor in either J19 or J25 at the same time.**

2.1.20 J20 – SYS I^2C Monitor Point and Alternate Connection

This header is provided to connect to or monitor the SYS I^2C signals on the TPS650380EVM-054. If the I^2C signals are being sent via this header (and not via the USB-TO-GPIO adaptor), do not plug into the J19 or J25 headers and provide a separate V_{DD} supply between J13 and J14.

2.1.21 J21 – DVS I^2C Monitor Point and Alternate Connection

This header is provided to connect to or monitor the DVS I^2C signals on the TPS650380EVM-054. If the I^2C signals are being sent via this header (and not via the USB-TO-GPIO adaptor), do not plug into the J19 or J25 headers and provide a separate V_{DD} supply between J13 and J14.

2.1.22 J22 – DCDC_A Load Step Signal Input

This SMA connector accepts a signal input from a function generator that drives Q1 in order to evaluate DCDC_A's transient response. This connector is not normally installed. TP3 can be used instead to apply the signal.

2.1.23 J23 – DCDC_B Load Step Signal Input

This SMA connector accepts a signal input from a function generator that drives Q2 in order to evaluate DCDC_B's transient response. This connector is not normally installed. TP4 can be used instead to apply the signal.

2.1.24 J24 – DCDC_C Load Step Signal Input

This SMA connector accepts a signal input from a function generator that drives Q3 in order to evaluate DCDC_C's transient response. This connector is not normally installed. TP13 can be used instead to apply the signal.

2.1.25 J25 – DVS I^2C Connection from USB-TO-GPIO Adaptor

This connects the USB-TO-GPIO adaptor to the DVS I^2C connection of the TPS650380. It provides the I^2C signals and a 3.3 V supply for powering V_{DD}. This connector is keyed to prevent incorrect installation. **Only install a USB-TO-GPIO adaptor in either J19 or J25 at the same time.**

2.1.26 JP1 – EN

This jumper sets the EN pin to either a logic high (ON, jumper across pins 1 and 2) or a logic low (OFF, jumper across pins 2 and 3). When EN is low, the TPS650380 output will be off and not switching. Set EN to ON to turn on the output voltage.

2.1.27 JP2 – V_{DD} Control

This jumper is used to connect V_{DD} to a 3.3V rail provided by the USB-TO-GPIO adaptor when the jumper is installed. Alternatively, the user can provide their own V_{DD} voltage (1.2 - 3.6V) between J13 and J14. The JP2 jumper should not be installed in this case. For normal operation without an external supply voltage, the jumper should be installed.

2.2 Software Setup

The software is available at the TI website,

http://focus.ti.com/docs/toolsw/folders/print/TPS650380EVM-054.html.

Download and unzip the file. Run setup.exe and follow the on screen instructions to complete the installation.

NOTE: This installation page is best viewed with Microsoft Internet Explorer browser (it may not work correctly with other browsers)

The Microsoft .Net Framework 2.0 is required for the software to run.

After installation, the software should automatically run. To run the software later, go to

Start→All Programs→Texas Instruments→TPS65038x EVM→TPS65038x EVM.

During future use of the software, it may prompt you to install a new version if one becomes available on the Web.

NOTE: VeriSign™ Code Signing is used to prevent any malicious code from changing this application. If at any time in the future the binaries are modified, the code will no longer attempt to run.

2.3 Hardware Setup

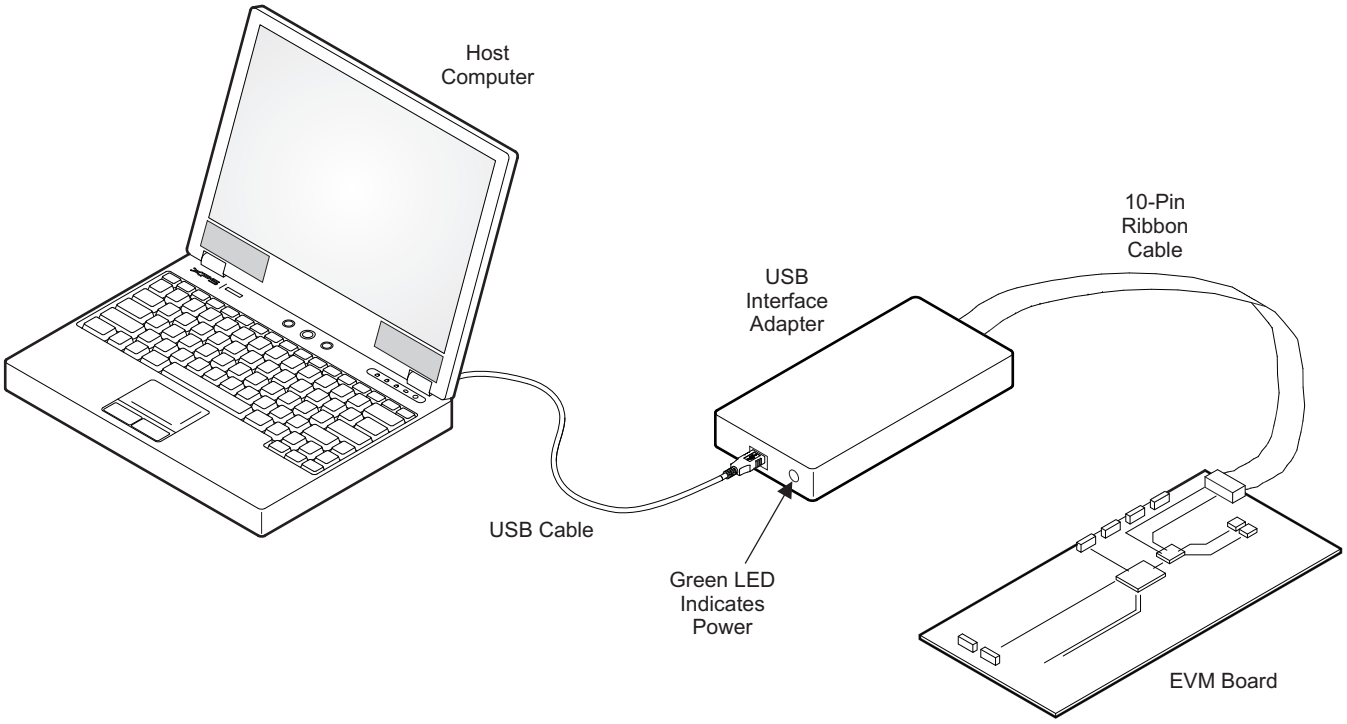
Table 2 shows the board default jumper settings.

Table 2. Default Jumper Settings

JUMPER	DEFAULT
JP1	Installed across pins 1 and 2
JP2	Installed across pins 1 and 2

Connect the USB-TO-GPIO adapter to your PC using the supplied USB cable. Connect the TPS650380EVM connector J19 or J25 to the USB-TO-GPIO adapter using the supplied 10-pin ribbon cable. The connectors on the ribbon cable are keyed to prevent incorrect installation. **Only install a USB-TO-GPIO adaptor in either J19 or J25 at the same time.**

USB Interface Adaptor Quick Connection Diagram



Connect the load (processor) to either the output headers J4 and J6, J7 and J9 (for currents below 1A), and J10 and J12 or to the output terminal blocks J17 and J18 (for currents greater than 1A). The leads should be short and twisted.

Install jumpers, JP1 through JP2 to the desired positions. Jumper JP1 must be across pins 1 and 2 for the TPS650380 to operate.

Connect at least a 5 A rated input power supply, set to provide between 2.5 V and 5.5 V, between J1 and J3 (for currents below 1 A) or to the terminal block J16 (for currents greater than 1 A). The leads should be short and twisted. Turn on the power supply.

3 Software Setup and Operation

This section provides descriptions of the EVM software and functionality.

The supplied software is used to communicate with the TPS650380EVM-054. Click on the icon on the host PC to start the software. The host PC software first checks the firmware version of the USB-TO-GPIO adapter. If an incorrect firmware version is installed, the software automatically searches on the Internet (if connected) for updates. If a new update is available, the software notifies the user of the update, downloads and installs the software. Note that after the firmware is updated, the user must disconnect and then reconnect the USB cable between the adapter and PC, as instructed during the install process. The host PC software also automatically searches on the Internet (if connected) for updates to the EVM software. If a new update is available, the software notifies the user of the update, downloads and installs the update.

V_{IN} and V_{DD} must be supplied for the software to detect the TPS650380 and run.

The software reads the registers on the TPS650380 and automatically determines which version of the IC is installed. Even if the IC is disabled via the EN pin (JP1), the user can still communicate with the TPS650380 if V_{IN} and V_{DD} are supplied.

The software displays the main panel for the user interface, shown in Figure 1.

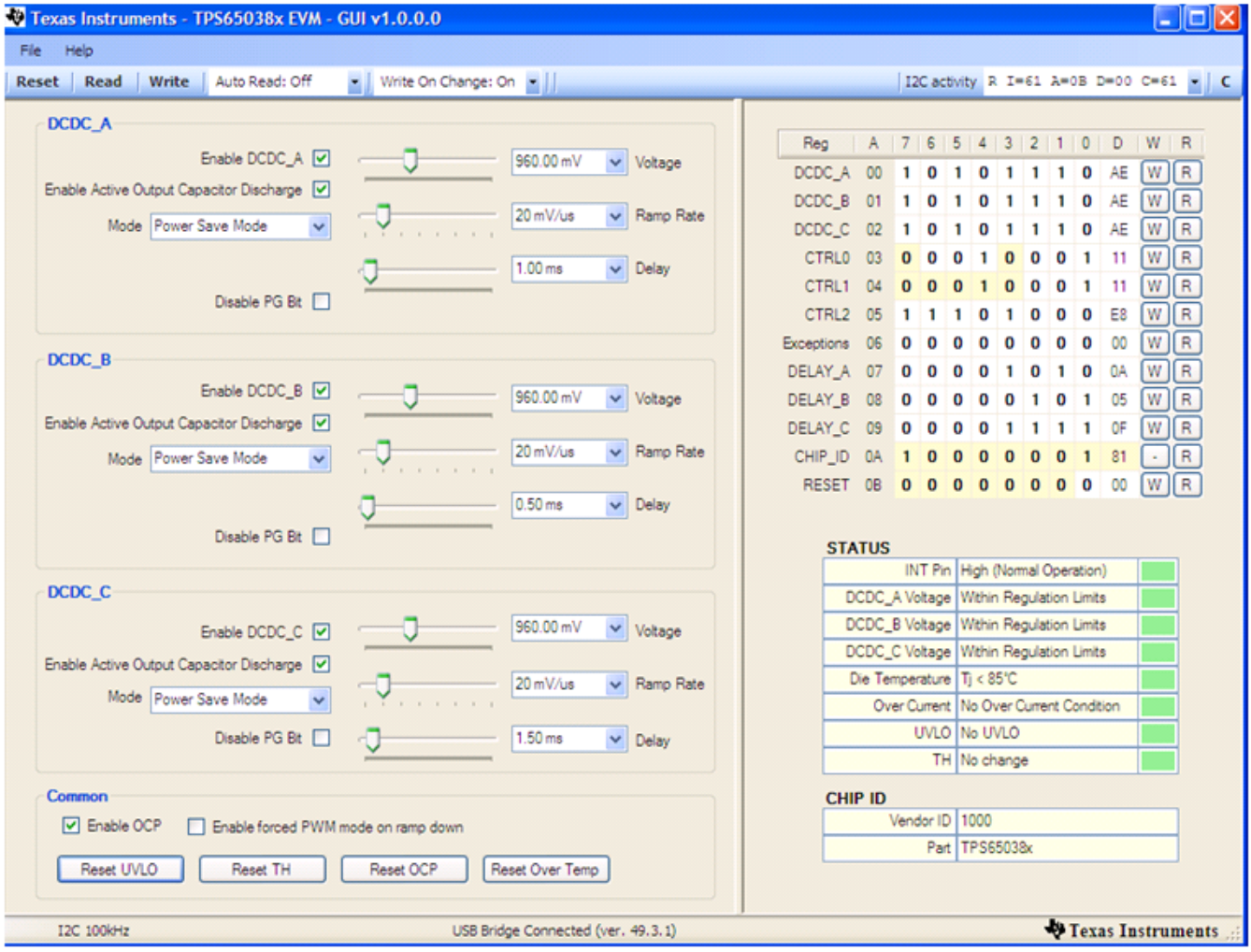


Figure 1. TPS650380 Software Main Panel

It is recommended that the user press the 'READ' button at the top of the screen immediately after loading the software to confirm that the software and cable connections are working properly. The message box at the top right of the main panel (I^2C Activity) displays all I^2C activity. The message box at the bottom (USB Bridge Connected) displays whether or not the USB-TO-GPIO connection is functional.

The software itself performs no calculations or computations and simply reads and writes to and from the IC's registers through the I^2C interface. Each register's bits can either be changed manually by changing the boxes corresponding to each bit in the panel's top right half, or they can be changed through the drop-down boxes and buttons in the rest of the panel. Some bits are reserved and not writeable. These will not allow you to click on them to change their setting. For example, the CHIP_ID register (0x0Ah) is read only and the TPS650380's main panel does not allow writes to those bits. The I^2C bus speed is fixed at 100 kbps and this is noted at the bottom of the screen.

Following any change to an individual bit, drop-down box, or button, the user must write the new values to the registers by either clicking the 'W' button to the left of each affected register or by clicking the 'WRITE' button at the top of the screen.

In order to reduce the amount of manual reading and writing required, the two drop-downs at the top left of the screen have been provided to do this automatically. The 'Auto Read' drop down allows the option of automatically reading all the registers at specific time intervals. The 'Write On Changes' drop-down allows the option of automatically writing a change to the registers as soon as it is made in the software.

The TPS650380 data sheet is available via the 'Help' menu (Internet access is required). The data sheet discusses the functionality of the various register bits, which is also briefly repeated here.

The left side of the software main panel is divided into three parts--one for each output voltage. In each of these sections, the output voltage, ramp rate, and sequencing timer time can be changed. In addition, there are settings for enabling each output, enabling each output voltage's active output capacitor discharge circuit on shutdown, changing the mode status of each output voltage (Forced PWM mode or Power Save Mode), as well as an option to disable the nPG_x bit for each output voltage individually. These settings correspond to all of registers 0x00h through 0x04h and 0x07h through 0x09h, as well as portions of registers 0x05h and 0x06h.

In the bottom left corner of the software main panel are various common controls, including enabling the over-current protection, forcing PWM mode on a ramp down of the output voltage, and resetting bits in the exceptions register that correspond to various faults. These functions correspond to the remaining bits in registers 0x05h and 0x06h.

The bottom right corner of the software main panel contains a status output screen. Displayed are the status of the TPS650380's INT pin (high or low), the status of the exceptions register (0x06h), and the contents of the CHIP_ID register (0x0Ah) which identifies the IC installed.

Finally, in the upper left corner of the software's main panel is a RESET button which writes a 1 to the RESET bit of register 0x0Bh.

Circuit Use and Modifications

Besides the required circuitry to operate the TPS650380 (outlined in a white silk screen border on the PCB), there are additional circuits present on the TPS650380EVM-054 that assist in evaluating the TPS650380 as a processor power supply solution. Additionally, there are modifications that can be made to adapt the circuit's performance to the needs of a particular application.

3.1 Load Step Circuit

The TPS650380EVM-054 contains a simple circuit that produces fast load current steps at the output of the TPS650380. This evaluates the response of the TPS650380 to various load transients that might occur in the system. An identical circuit is included for each output voltage. To operate the circuit on the output of DCDC_A, connect a function generator to TP3. The output of the function generator should be a square wave with a small duty cycle. The output high level controls the gate to source voltage of the power transistor, Q1, and should be adjusted to generate the desired step current high level. The output low level sets the step current low level. Good settings to start with are a square wave signal running at 100 Hz and 5% duty cycle going from 0V to 3V. These settings can be adjusted in order to generate the desired load step.

Resistor R16 is present to observe the load step current by measuring the voltage across TP1 and TP2. Oscilloscope settings of 100 mV / div translate to a current in R16 of 1 A / div. R19 and R20 might be installed if large load current steps at low output voltages are desired.

3.2 Measuring the Control Loop

A bode plot of each output can be easily taken with a small modification to the EVM. To measure the control loop response of DCDC_A, for example, R1 is replaced with a 10-Ω resistor. Then, the injection signal is applied and the loop response measured across this resistor. Figure 14 shows the results of this test.

3.3 Circuit Modifications

Modifications may be made to the circuit. Any modifications will affect the performance of the EVM and must remain within the limits of the TPS650380 IC, as detailed in the data sheet.

CAUTION

As shipped, the EVM is configured for local sensing of the output voltages. If remote sensing at the loads is desired, modification of the EVM is required as described in the Remote Sense Resistors section.

3.3.1 Output Capacitors

There are locations for extra output capacitors to be installed on each output voltage in order to reduce output ripple or lessen the voltage drop due to a load transient. Some capacitors are located near the TPS650380 IC, while others can be installed closer to the point of load, which is simulated by the load step circuit. The total output capacitance on each output must remain below the maximum capacitance allowed in the data sheet.

3.3.2 Remote Sense Resistors

R1, R2, R3, R4, and R9 come populated with 0-Ω resistors that provide local output voltage sensing. Each output voltage is regulated at the output connector on the EVM. If it is desired to regulate the output voltage at the load, these resistors should be removed and wires used to connect the J5, J8, and J10 headers to each load. These wires should be twisted and kept as short as possible to minimize noise pickup. Use of the EVM without the local sense resistors or remote sense wires installed may damage the load or EVM.

3.3.3 I^2C Pull-up Resistors

R5, R6, R7, and R8 are locations for optional pull-up resistors for the I^2C signals. They are required when not using the USB-TO-GPIO adaptor but are not recommended when using the adaptor. If used, their typical value is around 2.2 kΩ.

4 Test Results

This section provides typical performance waveforms for the TPS650380EVM-054. The default register settings were used unless otherwise noted.

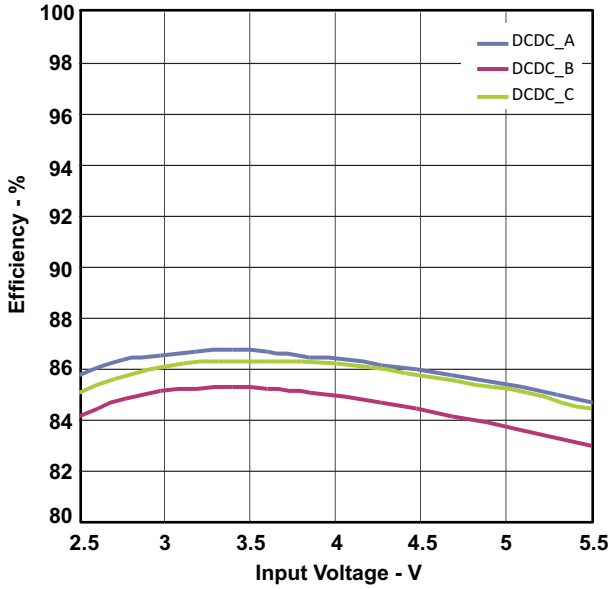


Figure 2. Efficiency vs. Input Voltage
(DCDC_A = DCDC_B = DCDC_C = 0.96 V, I_{OUTA} = 3.4 A, I_{OUTB} = 1.85 A, I_{OUTC} = 0.9 A)

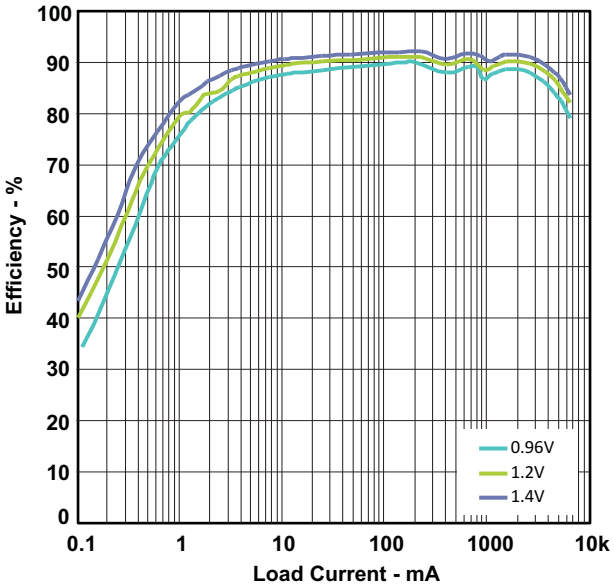


Figure 3. Efficiency of DCDC_A vs. Output Current (V_{IN} = 3.6 V)

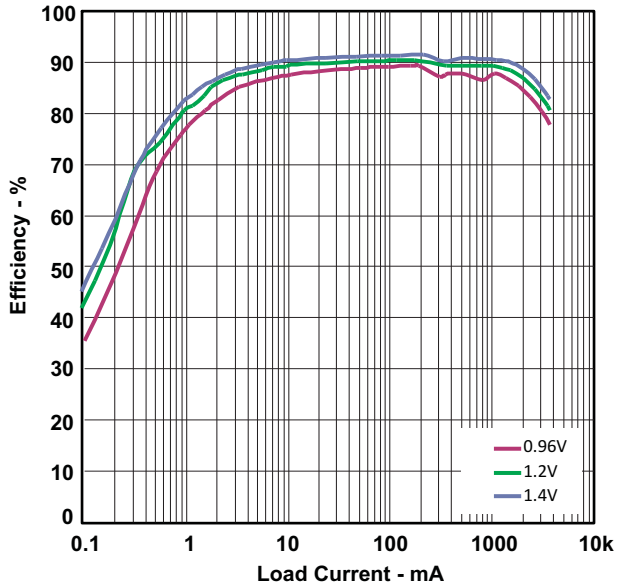


Figure 4. Efficiency of DCDC_B vs. Output Current (V_{IN} = 3.6 V)

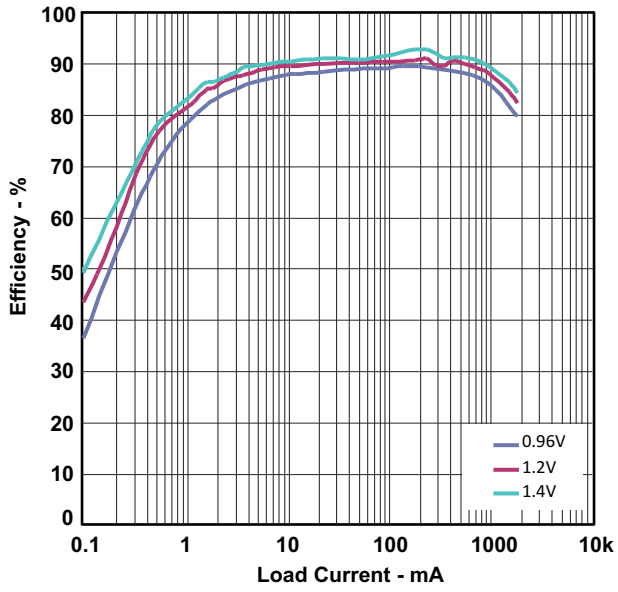


Figure 5. Efficiency of DCDC_C vs. Output Current (V_{IN} = 3.6 V)

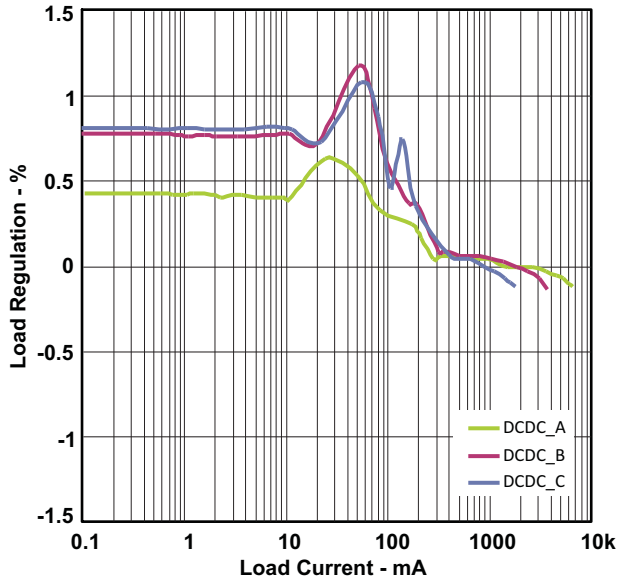


Figure 6. Load Regulation (V_{IN} = 3.6 V, DCDC_A = DCDC_B = DCDC_C = 0.96 V)

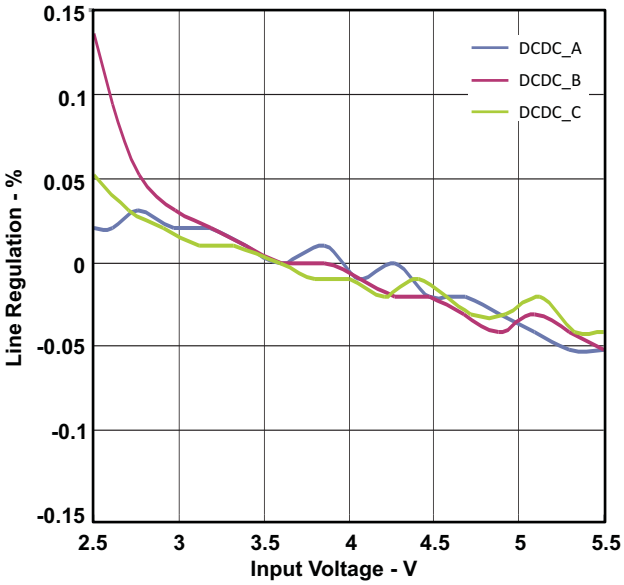


Figure 7. Line Regulation
(DCDC_A = DCDC_B = DCDC_C = 0.96 V, I_{OUTA} = 3.4 A, I_{OUTB} = 1.85 A, I_{OUTC} = 0.9 A)

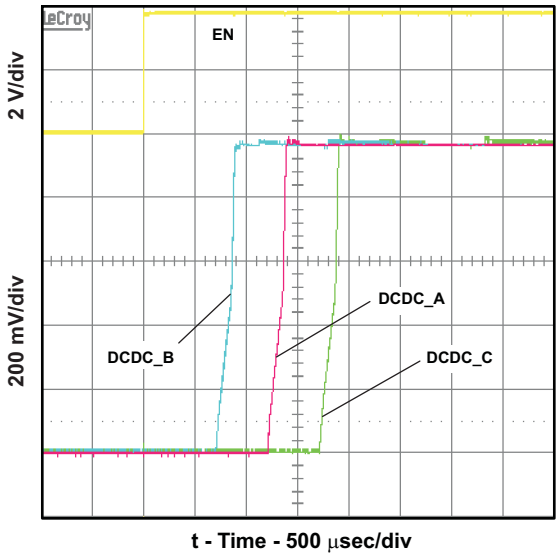


Figure 8. Start-up (V_{IN} = 3.6 V, DCDC_A = DCDC_B = DCDC_C = 0.96 V, I_{OUTA} = I_{OUTB} = I_{OUTC} = 0 A)

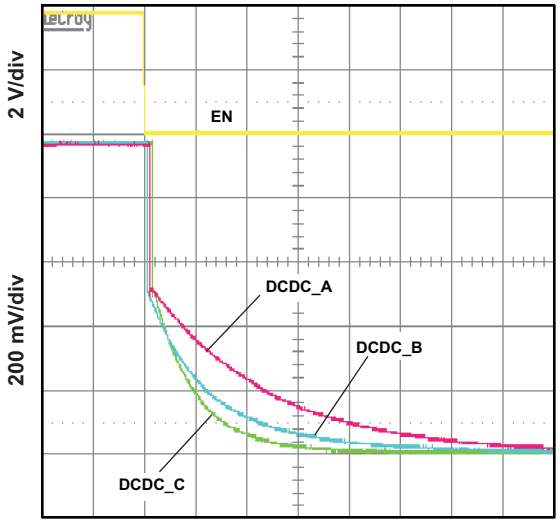


Figure 9. Shutdown (V_{IN} = 3.6 V, DCDC_A = DCDC_B = DCDC_C = 0.96 V, I_{OUTA} = I_{OUTB} = I_{OUTC} = 0 A, Active Output Capacitor Discharge Enabled)

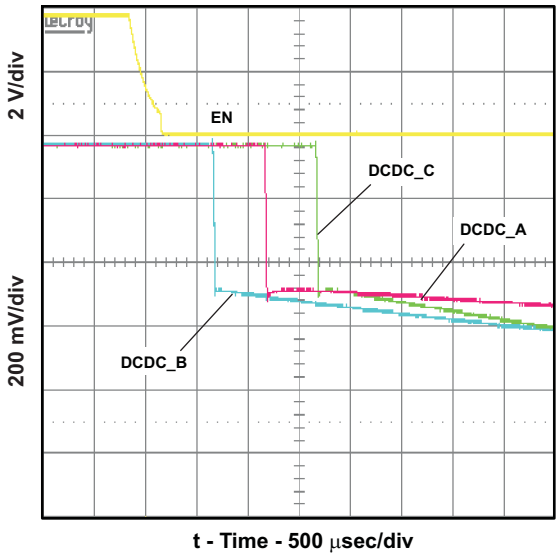


Figure 10. Shutdown (V_{IN} = 3.6 V, DCDC_A = DCDC_B = DCDC_C = 0.96 V, I_{OUTA} = I_{OUTB} = I_{OUTC} = 0 A, Active Output Capacitor Discharge Enabled)

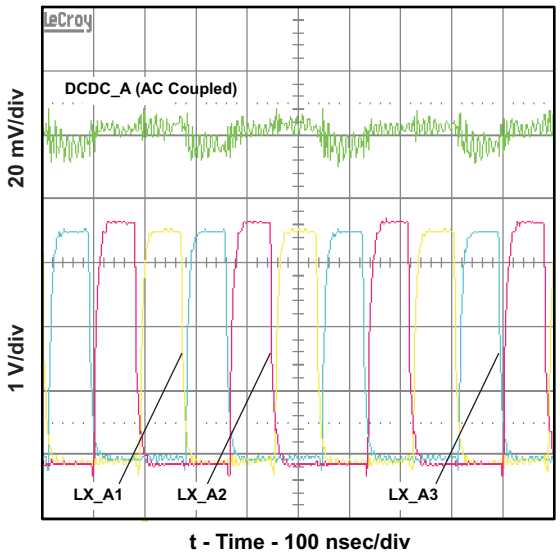


Figure 11. Output Voltage Ripple Measured Across C6 (V_{IN} = 3.6 V, DCDC_A = 0.96 V, DCDC_B = DCDC_C = disabled, I_{OUTA} = 5 A)

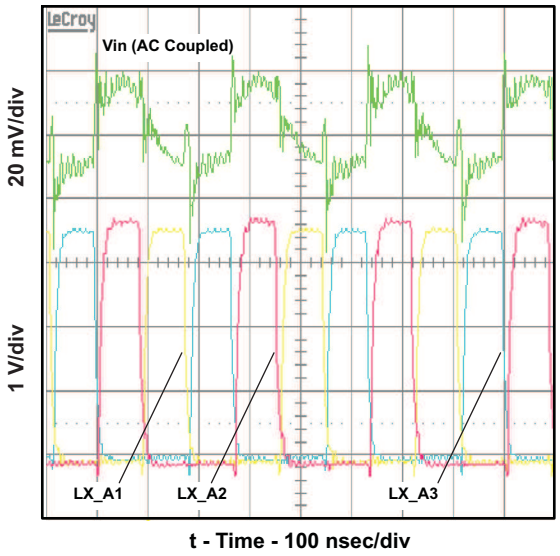


Figure 12. Input Voltage Ripple Measured Across C13
(V_{IN} = 3.6 V, DCDC_A = 0.96 V, DCDC_B = DCDC_C = Disabled, I_{OUTA} = 5 A)

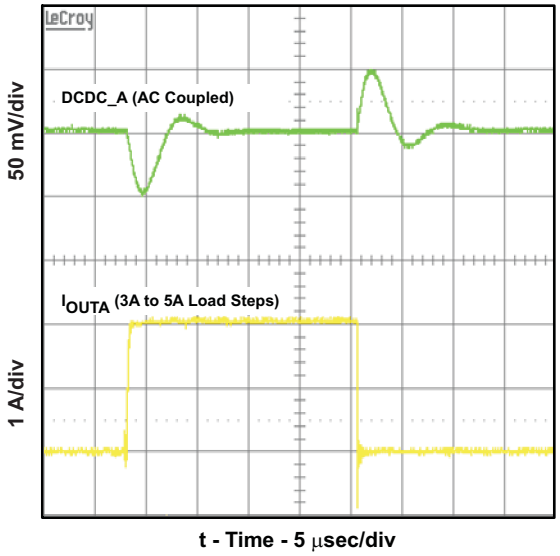


Figure 13. Load Transient Response
(V_{IN} = 3.6 V, DCDC_A = 0.96 V, DCDC_B = DCDC_C = Disabled, I_{OUTA} = 3 A to 5 A step)

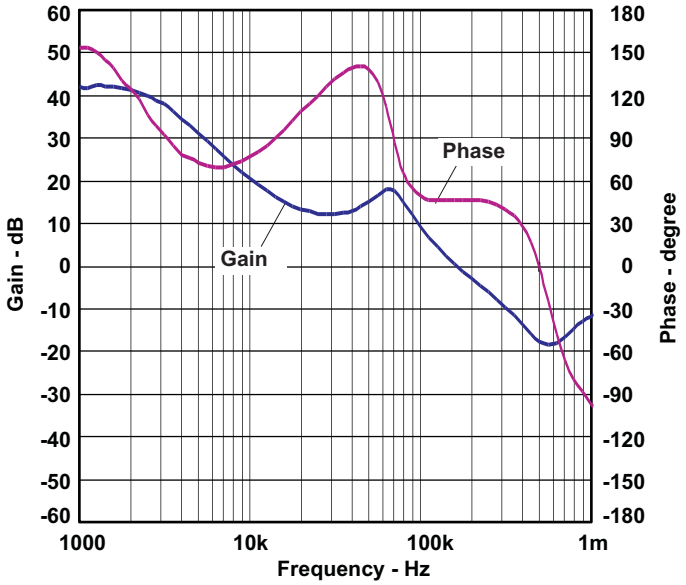


Figure 14. Loop Response (V_{IN} = 3.6 V, DCDC_A = 0.96 V, DCDC_B = DCDC_C = Disabled, I_{OUTA} = 5 A)

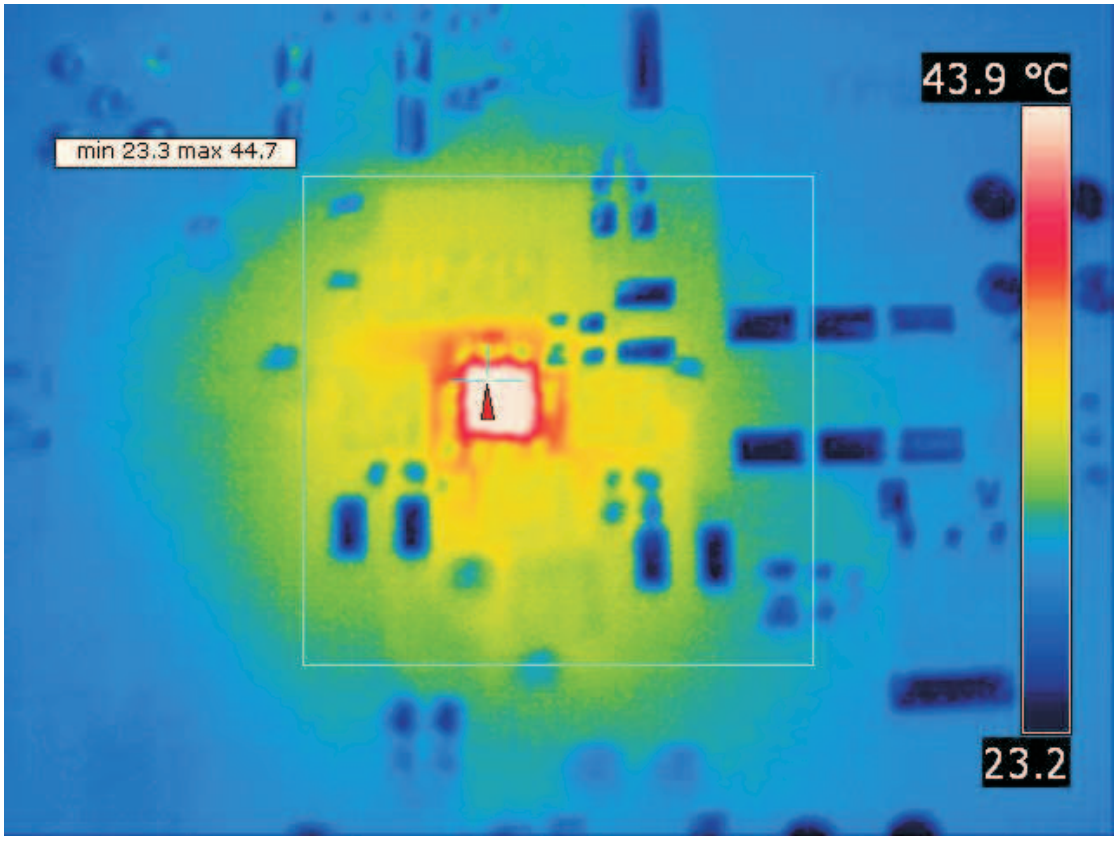


Figure 15. Thermal Performance
(V_{IN} = 3.6 V, DCDC_A = DCDC_B = DCDC_C = 0.96 V, I_{OUTA} = 3.4 A, I_{OUTB} = 1.85 A, I_{OUTC} = 0.9 A)

5 Board Layout

This section provides the TPS650380EVM-054 board layout and illustrations.

Board layout is critical for all high-frequency, switch-mode power supplies. Figure 16 through Figure 20 show the board layout for the TPS650380EVM-054 PCB. The nodes with high-switching frequencies and currents are kept as short as possible to minimize trace inductance. Careful attention has been given to the routing of high-frequency current loops and a single-point grounding scheme is used. Also, the majority of the heatsinking for this device occurs through the top layer traces and vias pulled from the IC's solder bumps that carry high currents. See the data sheet for specific layout guidelines.

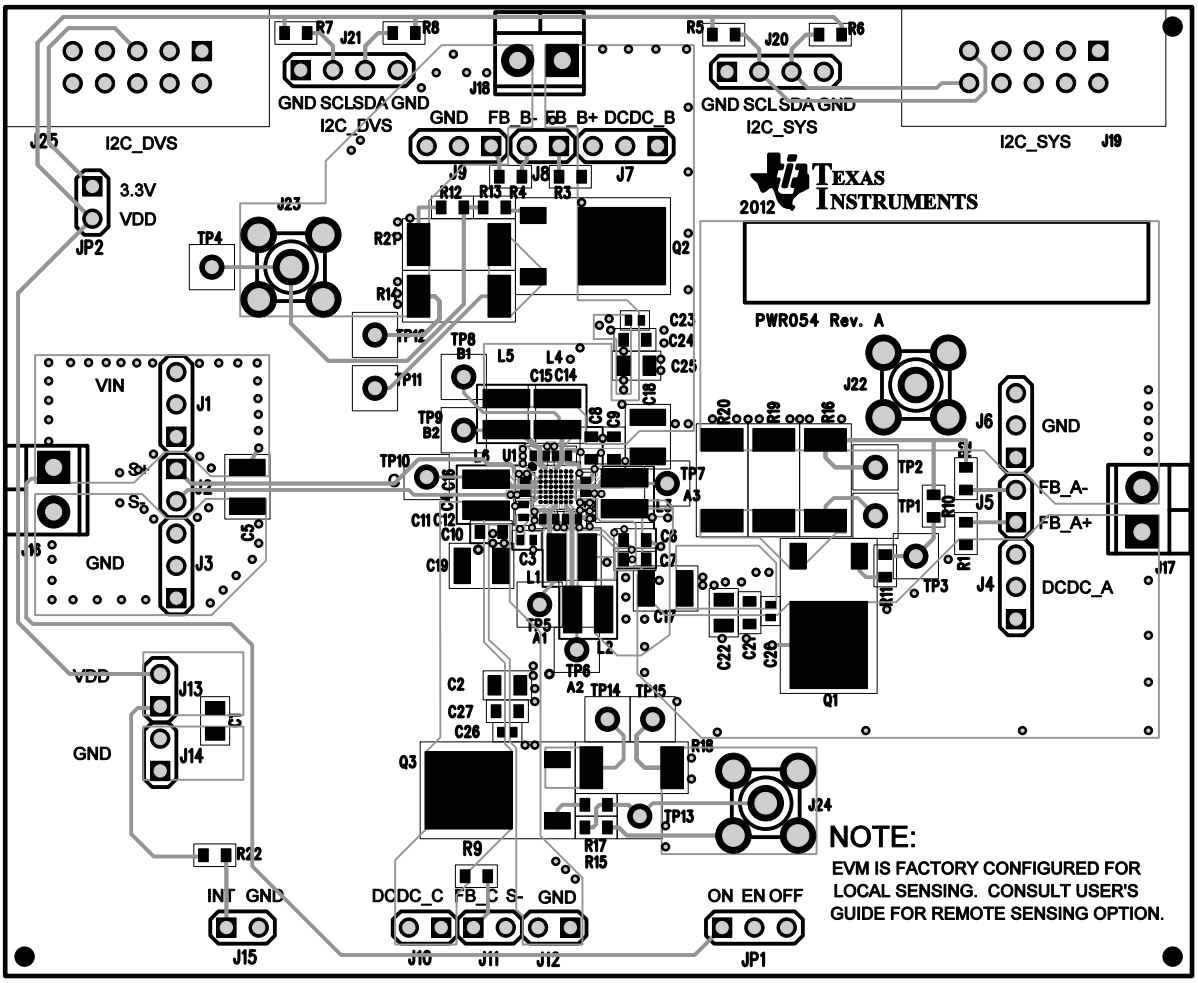


Figure 16. Assembly Layer

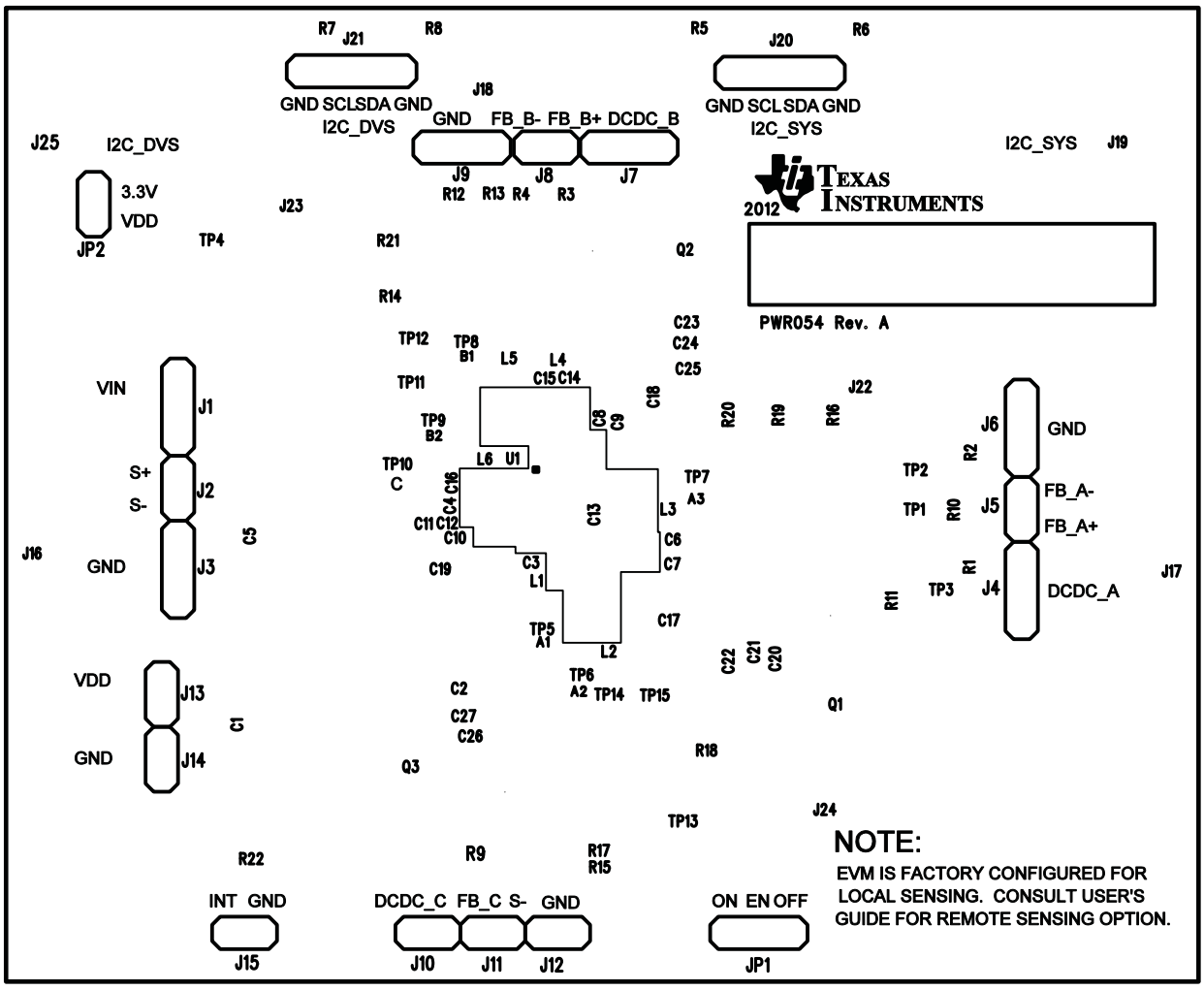


Figure 17. Top Silk Layer

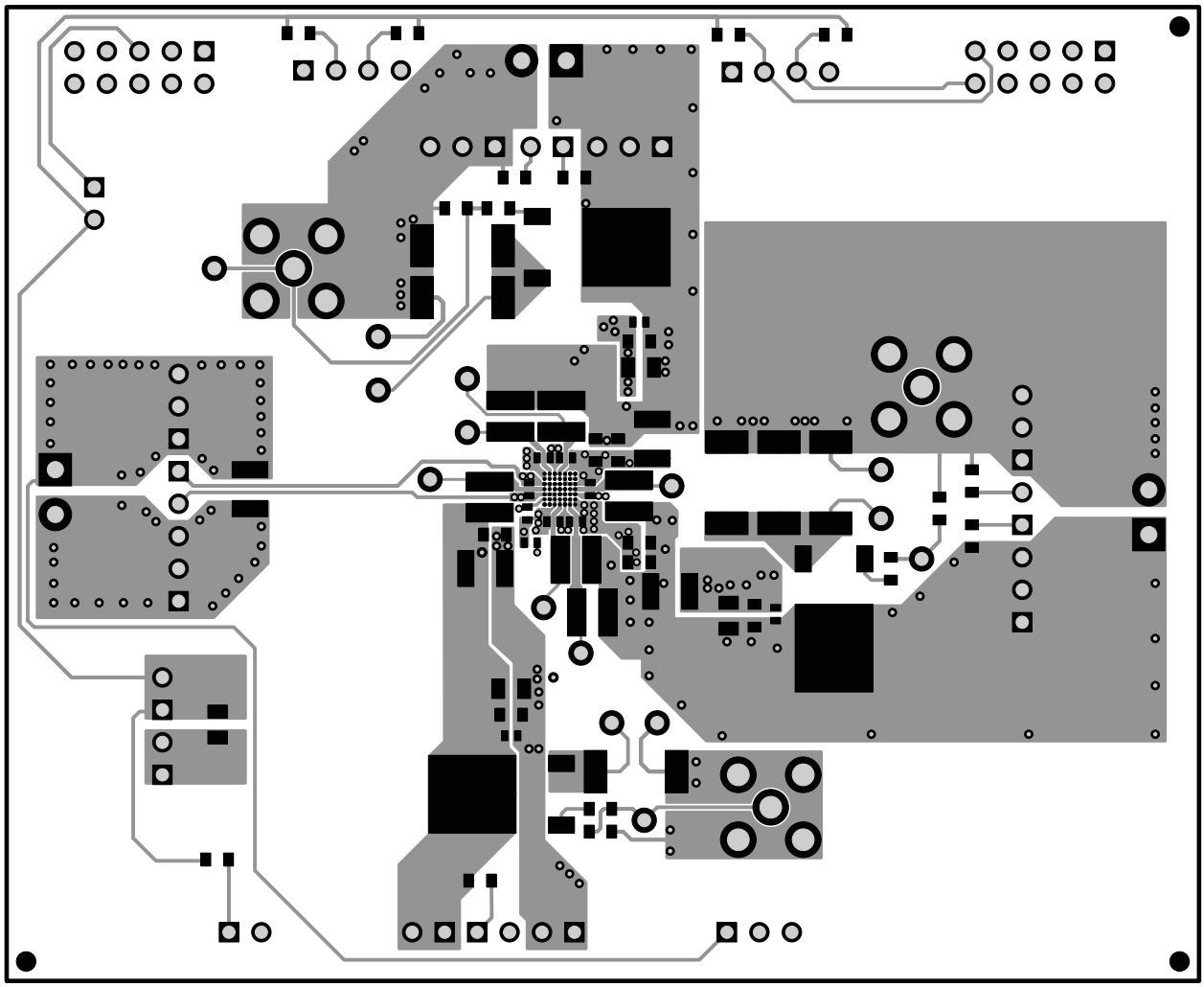


Figure 18. Top Layer

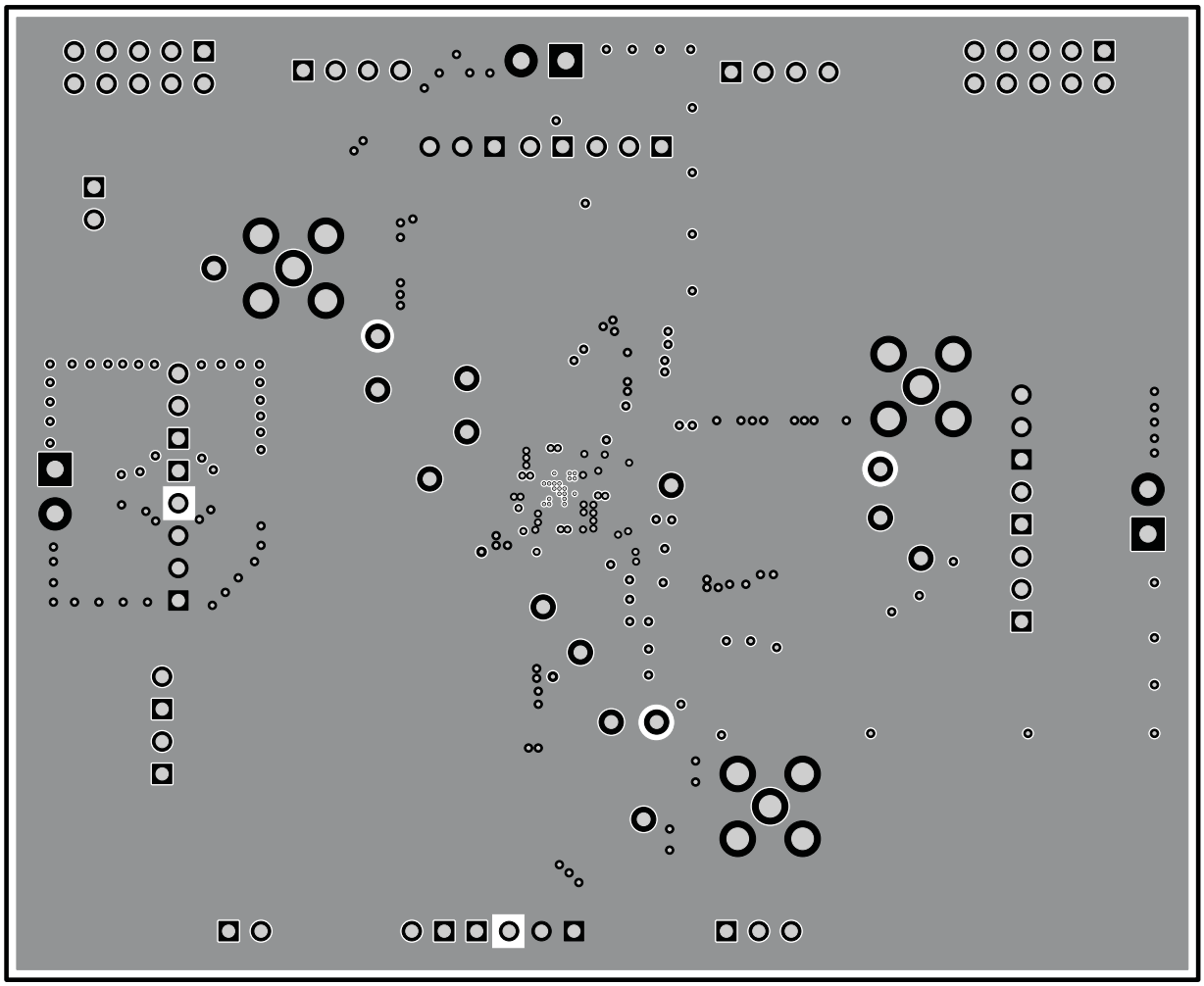


Figure 19. Layer 2

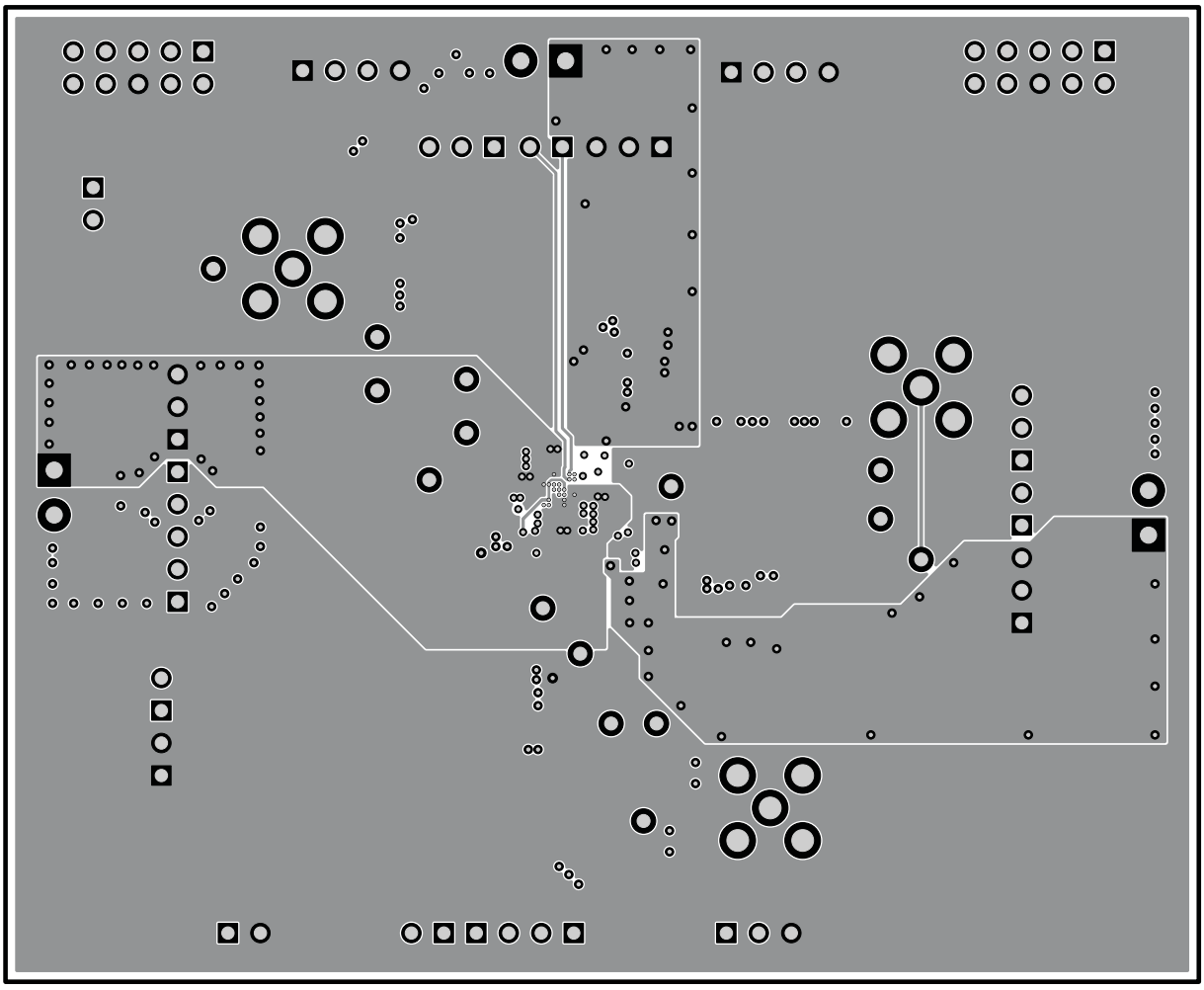


Figure 20. Layer 3

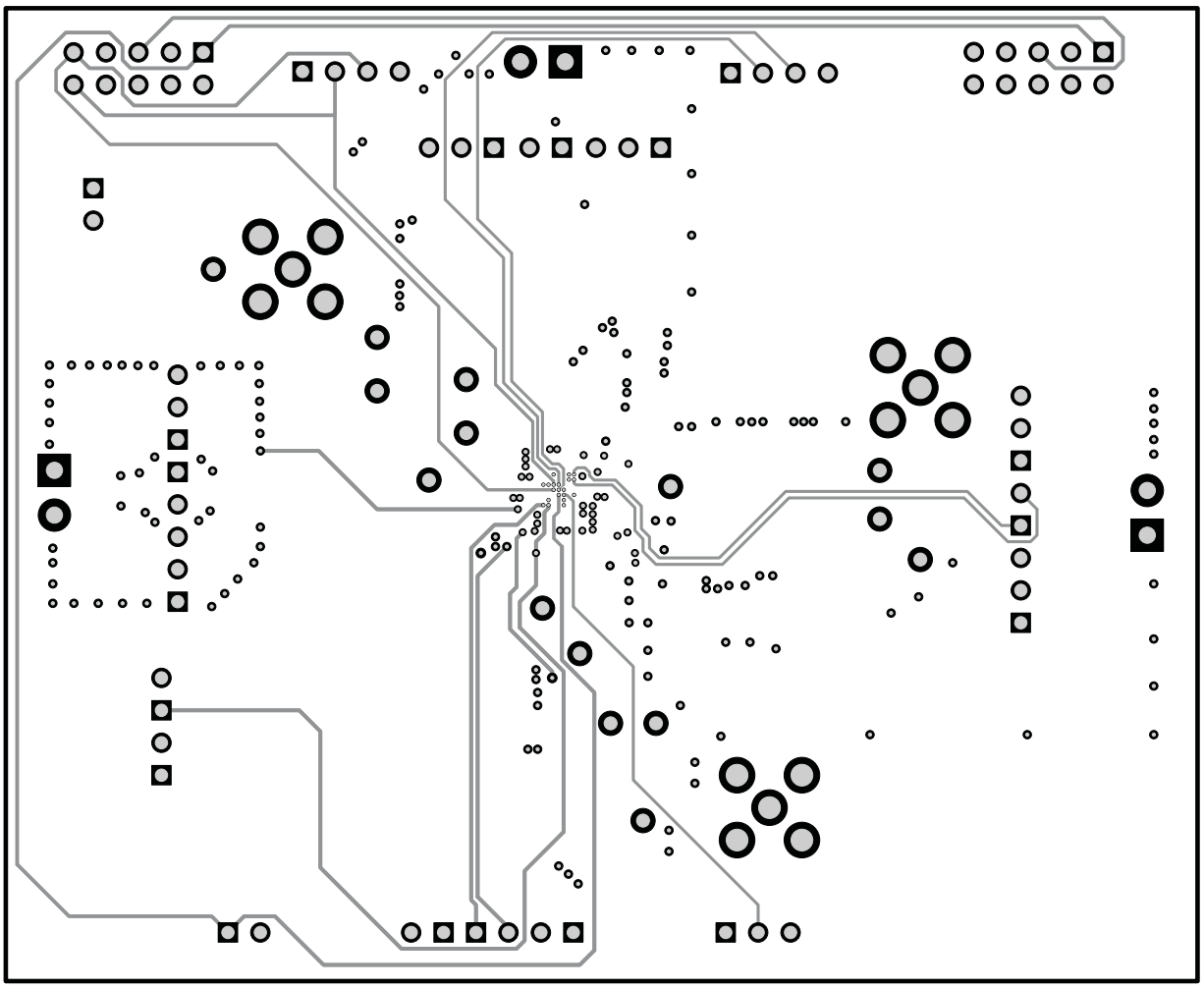


Figure 21. Bottom Layer

6 Schematic and Bill of Materials

This section provides the TPS650380EVM-054 schematic and bill of materials. The bill of materials is provided in two tables. Table 3 are the components required to build the TPS650380 solution. Table 4 are the components used only to evaluate the TPS650380EVM-054 solution.

6.1 Bill of Materials

Table 3. TPS650380 Solution Required Components[(1)]

Count -001	RefDes	Value	Description	Size	Part Number	MFR
2	C3, C4	0.1uF	Capacitor, Ceramic, X5R, 10V, 20%	0402	STD	STD
4	C6, C7, C8, C10	10uF	Capacitor, Ceramic, X5R, 6.3V, 20%	0603	STD	STD
6	C11, C12, C13, C14, C15, C16	4.7uF	Capacitor, Ceramic, X5R, 6.3V, 20%	0402	STD	STD
6	L1, L2, L3, L4, L5, L6	0.47uH	Inductor, Shielded Power, 6.6A, 7.6 mOhm, 20%	4 mm x 4 mm	XFL4015-471ME	Coilcraft
1	U1	TPS650380	IC, miniPMU for Processor Power	3.25 mm x 3.25 mm	TPS650380YFF	TI

(1) The TPS650380EVM-054 is populated with TPS650380 (U1) devices that do not contain the correct top side markings on the top of the device itself. These devices are still fully tested TPS650380 devices.

Table 4. TPS650380EVM-054 Evaluation Components

Count -001	RefDes	Value	Description	Size	Part Number	MFR
0	C1, C2, C25	Open	Capacitor, Ceramic, X5R, 6.3V, 20%	0805	STD	STD
1	C5	100uF	Capacitor, Ceramic, X5R, 6.3V, 20%	1210	STD	STD
0	C9	Open	Capacitor, Ceramic, X5R, 6.3V, 20%	0603	STD	STD
0	C17, C18, C19	Open	Capacitor, Ceramic, X5R, 6.3V, 20%	1210	STD	STD
3	C20, C23, C26	4.7uF	Capacitor, Ceramic, X5R, 6.3V, 20%	0402	STD	STD
3	C21, C24, C27	10uF	Capacitor, Ceramic, X5R, 6.3V, 20%	0603	STD	STD
1	C22	22uF	Capacitor, Ceramic, X5R, 6.3V, 20%	0805	STD	STD
0	J22, J23, J24	901-144-8RFX	Connector, SMA , Straight, PC mount	0.210 sq inch	901-144-8RFX	AMP
3	Q1, Q2, Q3	IRLR3715	MOSFET, N-ch, 20V, 49A, 11 milliohm	DPAK	IRLR3715ZPbF	IR
5	R1, R2, R3, R4, R9	0	Resistor, Chip, 1/16W	0603	STD	STD
0	R5, R6, R7, R8	Open	Resistor, Chip, 1/16W, 1%	0603	STD	STD
4	R10, R12, R15, R22	10.0K	Resistor, Chip, 1/16W, 1%	0603	STD	STD
3	R11, R13, R17	100	Resistor, Chip, 1/16W, 1%	0603	STD	STD
3	R14, R16, R18	0.1	Resistor, Chip, 1W, 1%	2512	STD	STD
0	R19, R20, R21	Open	Resistor, Chip, 1W, 1%	2512	STD	STD

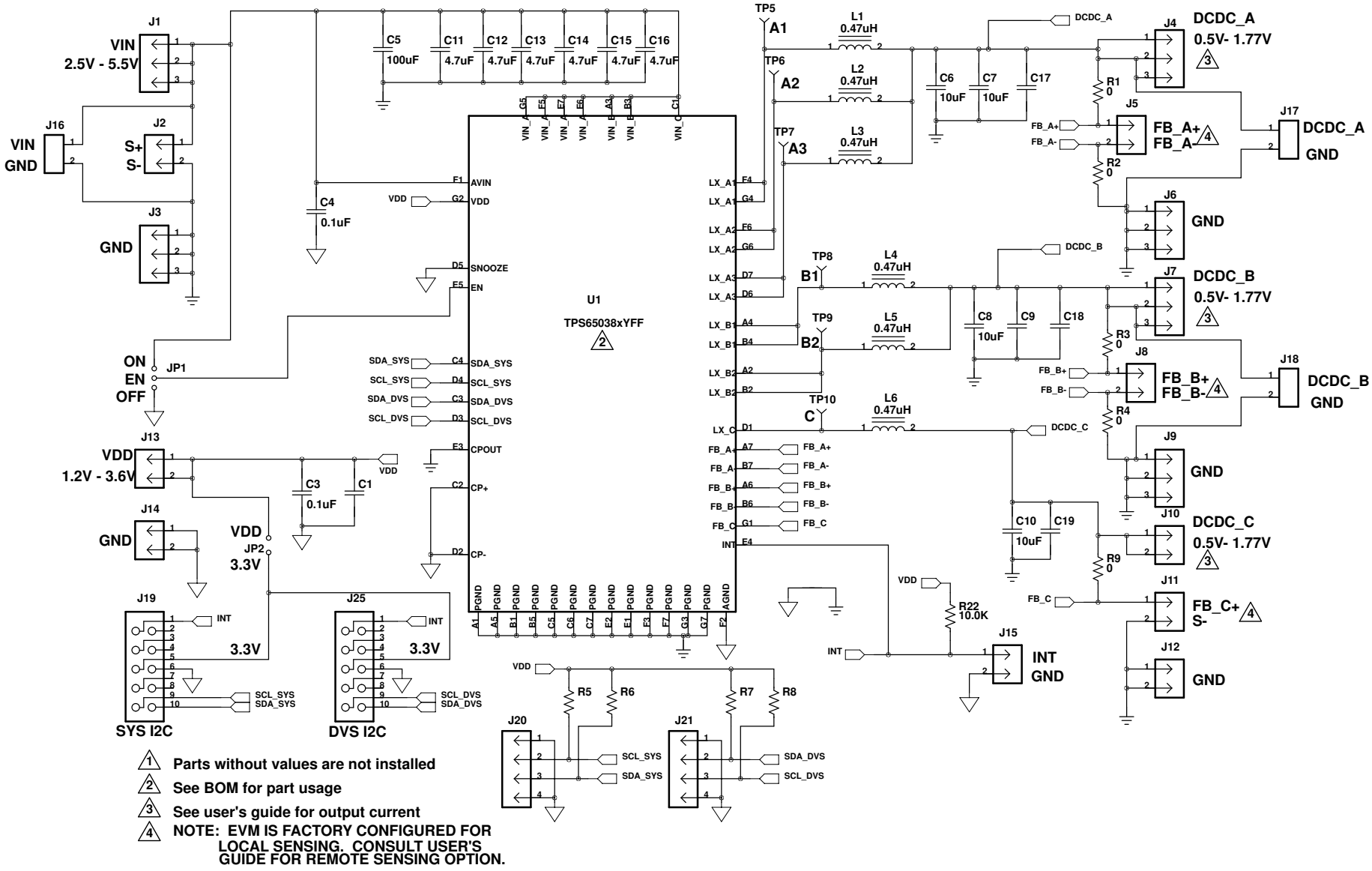
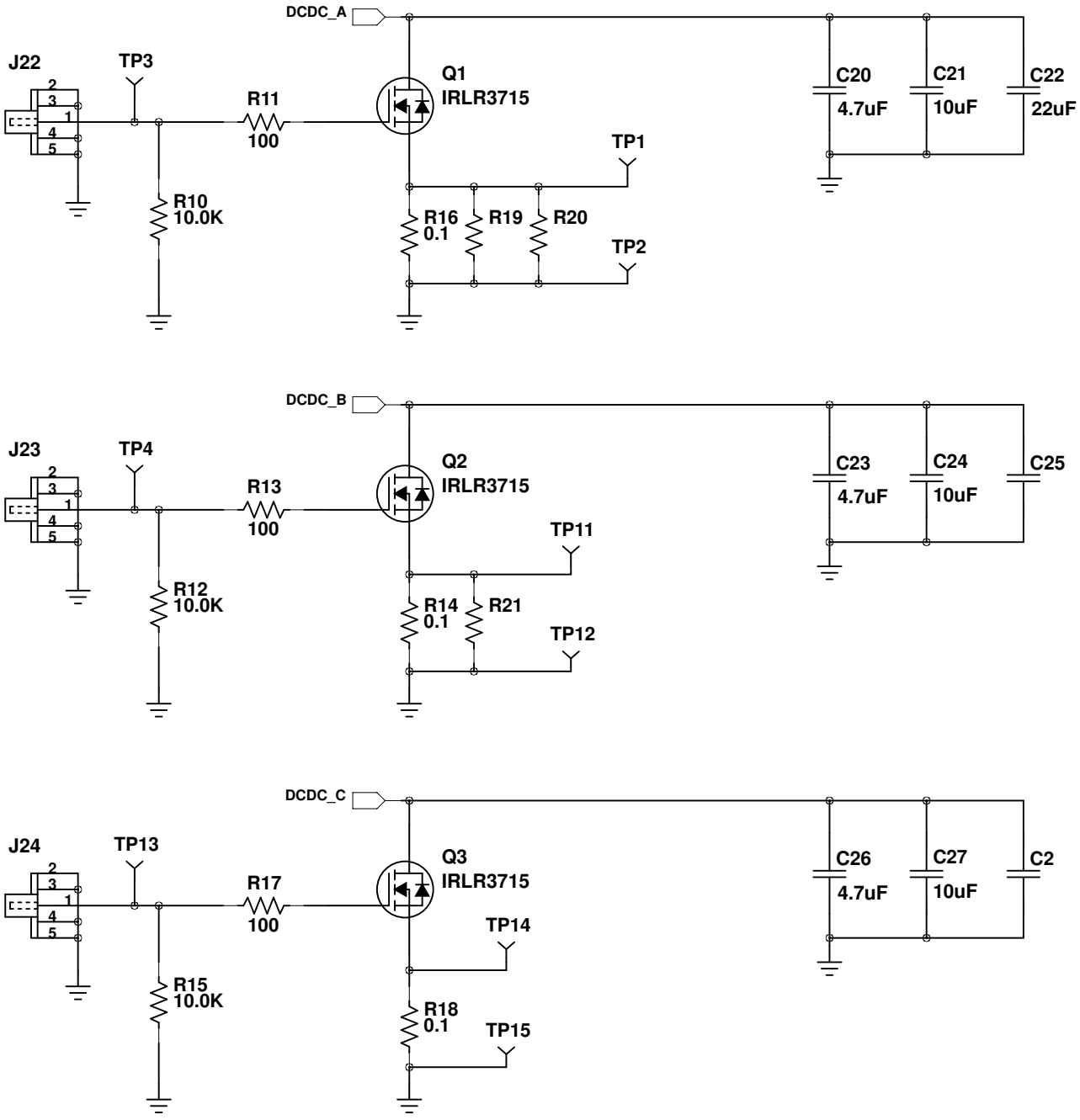


Figure 22. Schematic, Page 1



1 **Parts without values are not installed**

Figure 23. Schematic, Page 2

6.2 Related Documentation From Texas Instruments

miniPMU with 3 DC/DC Converters for Application Processors data sheet (SLVSBL5)

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For EVMs **not** subject to the above rules, this evaluation board/kit/module is intended for use for ENGINEERING DEVELOPMENT, DEMONSTRATION OR EVALUATION PURPOSES ONLY and is not considered by TI to be a finished end product fit for general consumer use. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or ICES-003 rules, which are designed to provide reasonable protection against radio frequency interference. Operation of the equipment may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: This radio is intended for development/professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability of this EVM and its development application(s) must comply with local laws governing radio spectrum allocation and power limits for this evaluation module. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by Texas Instruments unless user has obtained appropriate experimental/development licenses from local regulatory authorities, which is responsibility of user including its acceptable authorization.

For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

For EVMs annotated as IC – INDUSTRY CANADA Compliant

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs including radio transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs including detachable antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada.

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

【Important Notice for Users of this Product in Japan】

This development kit is NOT certified as Confirming to Technical Regulations of Radio Law of Japan

If you use this product in Japan, you are required by Radio Law of Japan to follow the instructions below with respect to this product:

1. Use this product in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use this product only after you obtained the license of Test Radio Station as provided in Radio Law of Japan with respect to this product, or
3. Use of this product only after you obtained the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to this product. Also, please do not transfer this product, unless you give the same notice above to the transferee. Please note that if you could not follow the instructions above, you will be subject to penalties of Radio Law of Japan.

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