User's Guide

LM3475 Buck Controller Evaluation Module User's Guide

ABSTRACT

The TPS51225EVM-133 evaluation module (EVM) uses the TPS51225. The TPS51225 is a D-CAP™ mode, dual synchronous step-down controller with 5-V and 3.3-V low-dropout regulators (LDO). The EVM provides fixed 5-V and 3.3-V outputs at up to 10 A each, from a 12-V input bus.

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Trademarks

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1 Description

The TPS51225EVM-133 is designed to use a regulated 12-V bus to produce regulated 5-V and 3.3-V outputs at up to 10 A each of load current. The EVM demonstrates the TPS51225 as a computing-system power supply. It also provides 5-V and 3.3-V LDOs and 14-V voltage-current protection (VCP) for charge pump applications.

1.1 Typical Applications

- Notebook computers, netbooks, tablet computers
- Servers, telecom motherboards, embedded computers

1.2 Features

The TPS51225EVM-133 features:

- 10-A DC steady-state output current for 5-V and 3.3-V outputs
- Supports pre-bias output voltage start-up
- S1 for Enable/Disable output1
- S2 for Enable/Disable output2
- Convenient test points for probing critical waveforms

2 Electrical Performance Specifications

Table 2-1. TPS51225EVM-133 Electrical Performance Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Voltage range	V_{IN}	8	12	20	V
Maximum input current	V_{IN} = 8 V, 5 V_{OUT}, 1/10 A, 3.3 V_{OUT}, 2/10 A		7.3		A
No load input current	V_{IN} = 20 V, 5 V_{OUT}, 1/0 A, 3.3 V_{OUT}, 2/0 A with auto-skip mode		1.5		mA
OUTPUT CHARACTERISTICS					
Output voltage V_{OUT}1			5		V
Output voltage regulation	Line regulation (V_{IN} = 8 V–20 V)		0.1%		
	Load regulation (V_{IN} = 12 V, VOUT1/0 A–10 A with auto-skip mode), Voutput2: off		0.5%		
Output voltage ripple	V_{IN} = 12 V, VOUT1/ 10 A , Voutput2: off		32		mVpp
Output load current	V_{IN} = 8 V–20 V	0	8	10	A
Output over current	V_{IN} = 12 V		12.9		A
Switching frequency	V_{IN} = 12 V, Voutput1/10 A		300		kHz
Efficiency	V_{IN} = 12 V, Vout1/10 A, Vout2: off		95.69%		
Output voltage Vout2			3.3		V
Output voltage regulation	Line regulation (V_{IN} = 8 V–20 V)		0.1%		
	Load regulation (V_{IN} = 12 V, VOUT 2/0 A–10 A with auto-skip mode), Voutput1: off		0.5%		
Output voltage ripple	V_{IN} = 12 V, Vout2/10 A , Voutput1: off		30		mVpp
Output load current	V_{IN} = 8 V–20 V	0	8	10	A
Output over current	V_{IN} = 12 V		12.9		A
Switching Frequency	V_{IN} = 12 V, Voutput2/10 A		355		kHz
Efficiency	V_{IN} = 12 V, Vout2 at 10 A, Vout1: off		94.33%		
Operating temperature			25		°C

3 Schematic

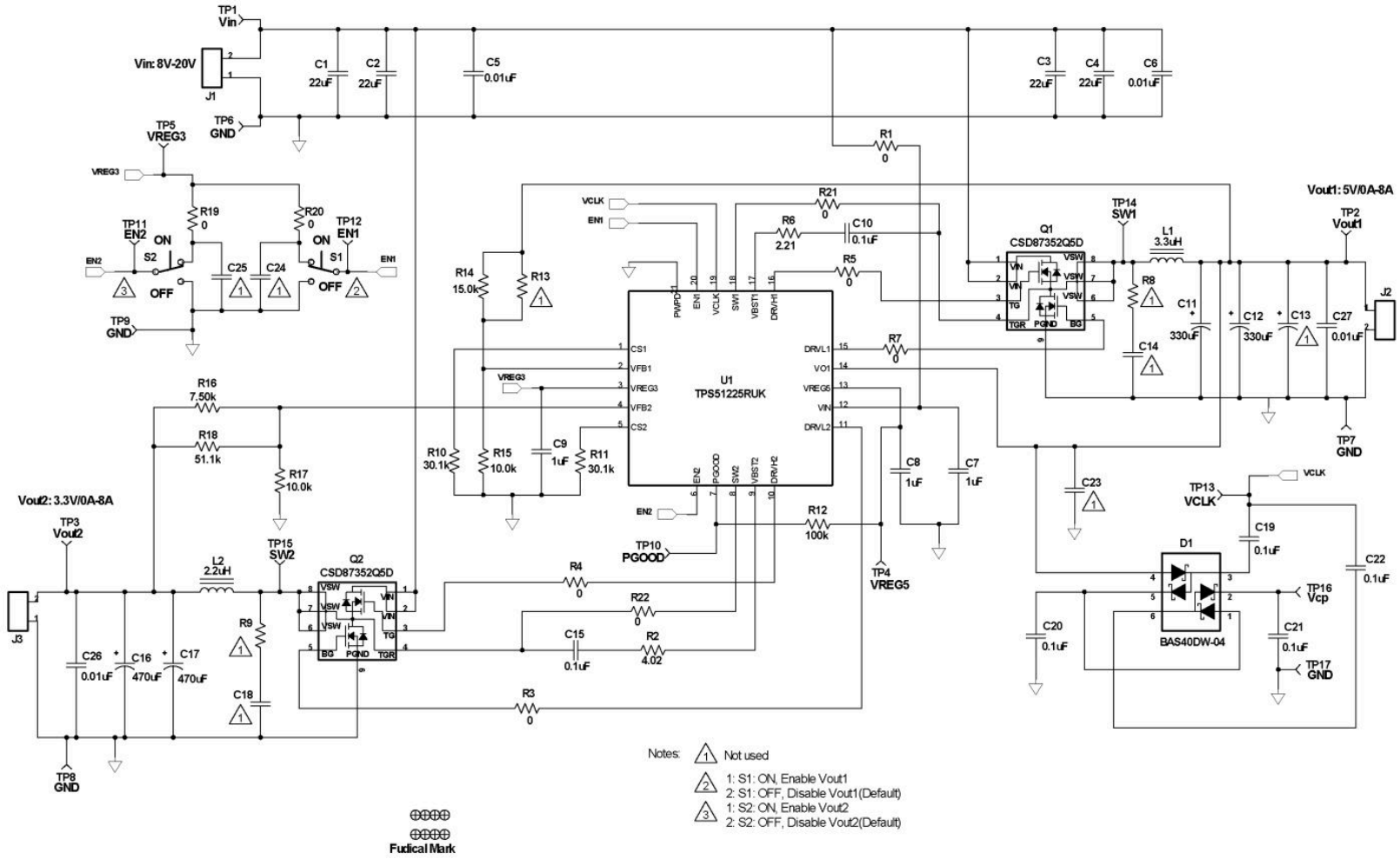

Figure 3-1. TPS51225EVM-133 Schematic

4 Test Setup

4.1 Test Equipment

Voltage Source: The input voltage, V_{IN}, should be a 0-V to 20-V variable DC source capable of supplying 10 A_{DC}. Connect VIN to J1 as shown in Figure 4-2.

Multimeters:

- V1: V_{IN} at TP1 (VIN) and TP6 (GND)
- V2: Vout1 at TP2 (Vout1) and TP7 (GND)
- V3: Vout2 at TP3 (Vout2) and TP8 (GND)
- A1: V_{IN} input current

Output Load: The output load should be an electronic constant resistance mode load capable of 0 A_{DC} to 15 A_{DC}.

Oscilloscope: A digital or analog oscilloscope can measure the output ripple. Set the oscilloscope for the following:

- 1-MΩ impedance
- 20-MHz bandwidth
- AC coupling
- 4-µs/division horizontal resolution
- 50-mV/division vertical resolution

Use test points TP2 (Vout1), TP3 (Vout2), TP7 (GND), and TP8 (GND) for measuring the output ripple voltage by placing the oscilloscope probe tip through TP2/TP3 and holding the ground barrel on TP7/TP8 as shown in Figure 4-1. Using a leaded ground connection can induce additional noise due to the large ground loop.

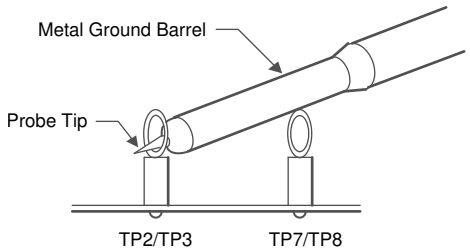

Figure 4-1. Tip and Barrel Measurement for V_{OUT} Ripple

Fan: Some of the components in this EVM can approach temperatures of 60°C during operation. A small fan capable of 200–400 linear feet per minute (LFM) is recommended to reduce component temperatures while the EVM is operating. Do not probe the EVM while the fan is not running.

Recommended Wire Gauge:

1. VIN to J1(12-V input):
   The recommended wire size is 1× American wire gauge (AWG) #14 per input connection, with the total length of wire less than four feet (2-feet input, 2-feet return).
2. J2, J3 to Load1, Load2:
   The minimum recommended wire size is AWG #14, with the total length of wire less than four feet (2-feet output, 2-feet return).

4.2 Recommended Test Setup

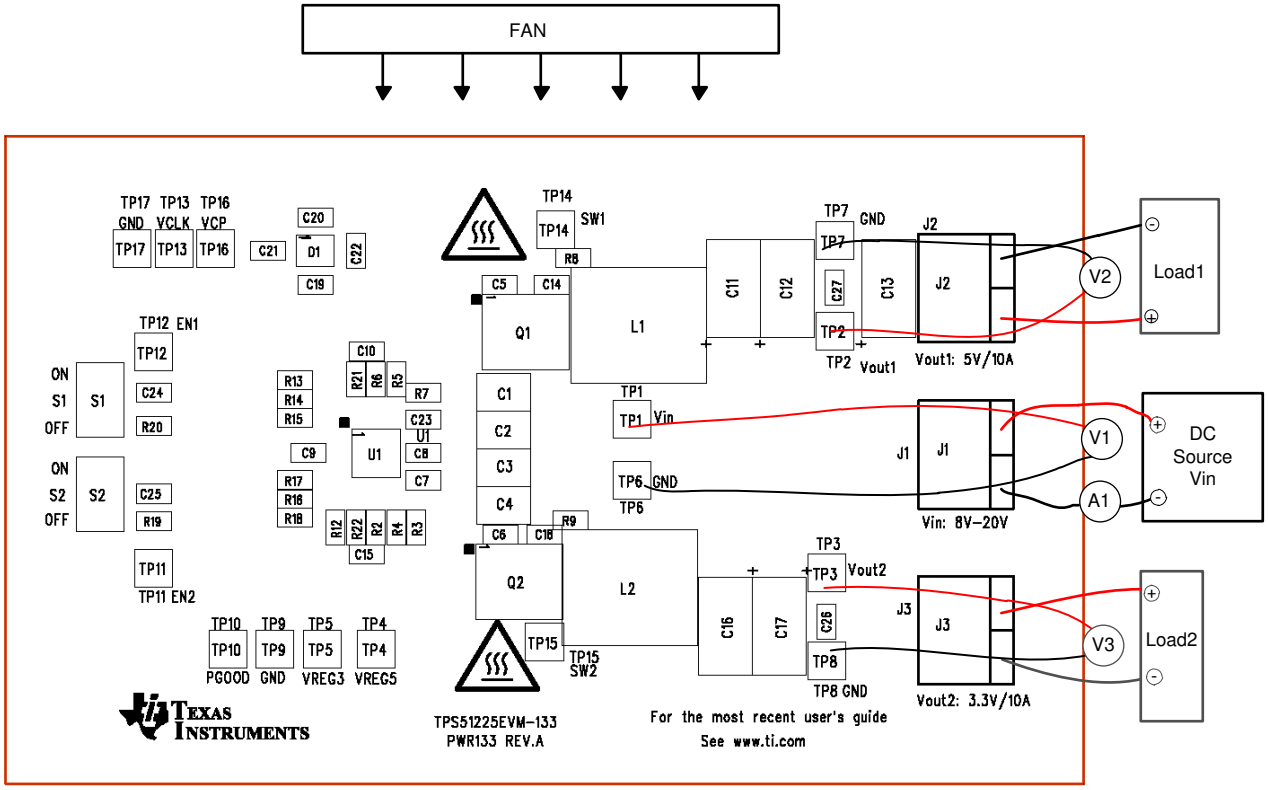

Figure 4-2. TPS51225EVM-133 Recommended Test Setup

Figure 4-2 is the recommended test setup for evaluating the EVM. Working at an ESD workstation, make sure that any wrist straps, bootstraps, or mats are connected referencing the user to earth ground before power is applied to the EVM.

Input Connections:

1. Prior to connecting the DC input source, V_{IN}, it is advisable to limit the source current from V_{IN} to 10-A maximum. Make sure VIN is initially set to 0 V and connected as shown in Figure 4-2.
2. Connect a voltmeter, V1, at TP1 (VIN) and TP6 (GND) to measure the input voltage.
3. Connect a current meter, A1, to measure the input current.

Output Connections:

1. Connect Load1 to J2 and set Load to constant resistance mode to sink 0 A_{DC} before VIN is applied
2. Connect a voltmeter, V2, at TP2 (Vout1) and TP7 (GND) to measure the output1 voltage.
3. Connect Load2 to J3 and set Load to constant resistance mode to sink 0 A_{DC} before VIN is applied.
4. Connect a voltmeter, V3, at TP3 (Vout2) and TP8 (GND) to measure the output2 voltage.

Other Connections:
Place a fan as shown in Figure 4-2 and turn it on, making sure air is flowing across the EVM.

5 Configurations

Make all switcher selections before applying power to the EVM. Configure this EVM per the following:

Enable1 Selection

The EN1 pin can be set by S1.
Default setting: S1 to OFF to disable the Output1

Table 5-1. EN1 Selection

Switcher set to	SKIPSEL Selection
ON	Enable the Output1
OFF	**Disable the Output1**

Enable2 Selection

Default setting: S2 to OFF to disable the Output2

Table 5-2. EN2 Selection

Switcher set to	Enable Selection
ON	Enable the Output2
OFF	**Disable the Output2**

6 Test Procedure

6.1 Line/Load Regulation and Efficiency Measurement Procedure

1. Set up the EVM as described in Section 4 and Figure 4-2.
2. Ensure Load1 and Load2 are set to constant resistance mode and to sink 0 A_{DC}.
3. Ensure the configuration settings per Section 5.
4. Ensure S1 and S2 are in the OFF position before V_{IN} is applied.
5. Increase V_{IN} from 0 V to 12 V. Use V1 to measure input voltage.
6. Switch S1 to the ON position to enable the Output1.
7. Use V2 to measure Vout1 voltage.
8. Vary Load1 from 0–10 A_{DC}. Vout1 should remain in load regulation.
9. Vary V_{IN} from 8 V to 20 V. Vout1 should remain in line regulation.
10. Switch S1 to the OFF position to disable the Output1.
11. Switch S2 to the ON position to enable the Output2.
12. Use V3 to measure Vout2 voltage.
13. Vary Load2 from 0–10 A_{DC}. Vout2 should remain in load regulation.
14. Vary V_{IN} from 8 V to 20 V. Vout2 should remain in line regulation.
15. Switch S2 to the OFF position to disable the Output2.
16. Decrease Load1 and Load2 to 0 A.
17. Decrease V_{IN} to 0 V.

6.2 List of Test Points

Table 6-1. The Functions of Each Test Points

Test Points	Name	Description
TP1	Vin	12-V input
TP2	Vout1	5-V output
TP3	Vout2	3.3-V output
TP4	VREG5	5-V LDO output
TP5	VREG3	3.3-V LDO output
TP6	GND	Ground
TP7	GND	Ground
TP8	GND	Ground
TP9	GND	Ground
TP10	PGOOD	Power Good
TP11	EN2	Enable2
TP12	EN1	Enable1
TP13	VCLK	Clock output for charge pump
TP14	SW1	Switching node of Output1
TP15	SW2	Switching node of Output2
TP16	VCP	14-V charge bump voltage
TP17	GND	Ground

6.3 Equipment Shutdown

1. Shut down Load1 and Load2.
2. Shut down VIN.
3. Shut down the fan.

7 Performance Data and Typical Characteristic Curves

Figure 7-1 through Figure 7-17 present typical performance curves for the TPS51225EVM-133.

7.1 5-V Efficiency

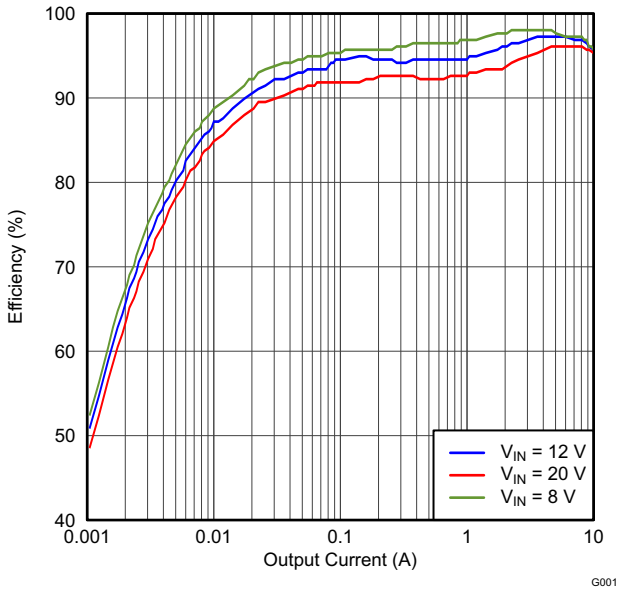

Figure 7-1. 5-V Efficiency

7.2 5-V Load Regulation

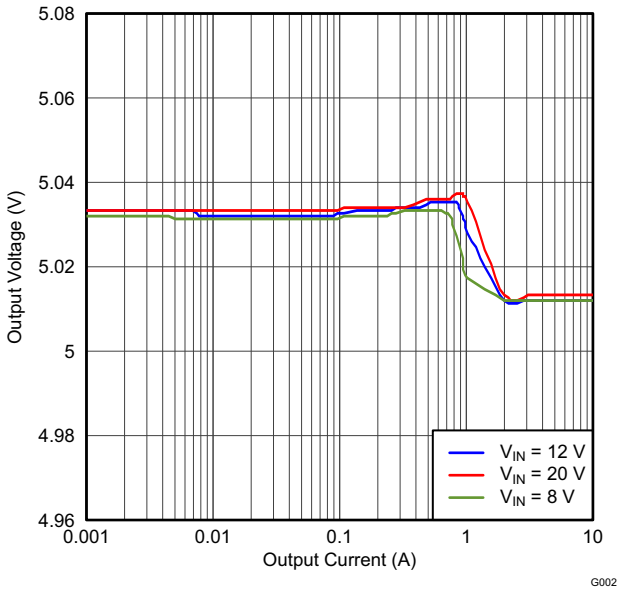

Figure 7-2. 5-V Load Regulation

7.3 3.3-V Efficiency

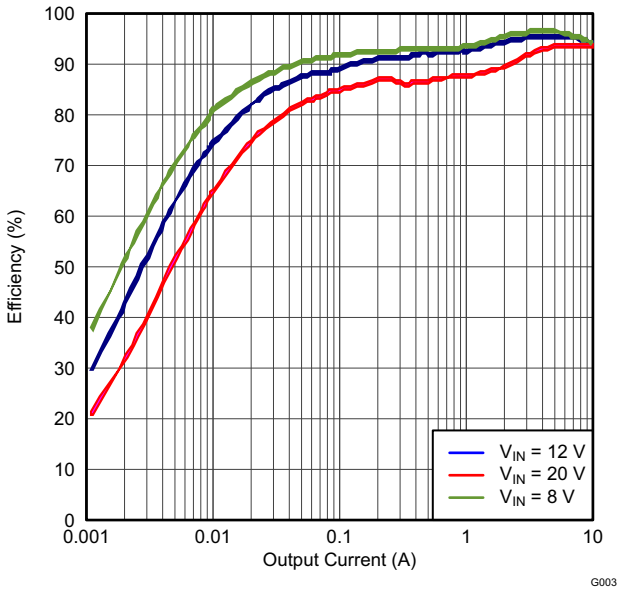

Figure 7-3. 3.3-V Efficiency

7.4 3.3-V Load Regulation

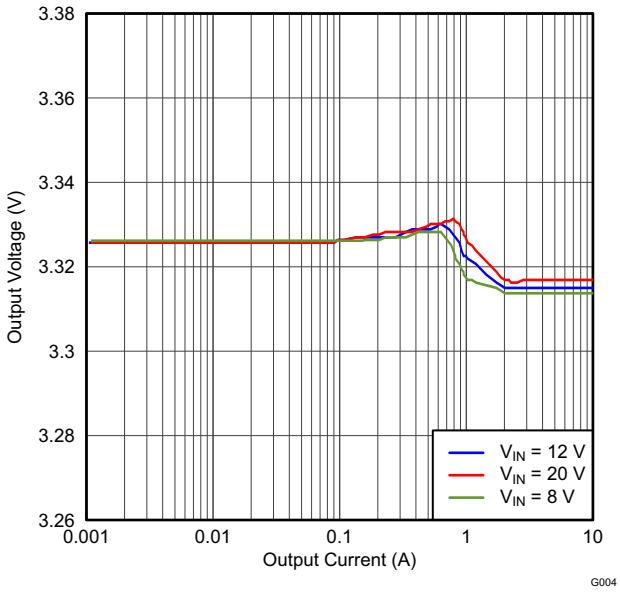

Figure 7-4. 3.3-V Load Regulation

7.5 Enable Turn-On/Turn-Off

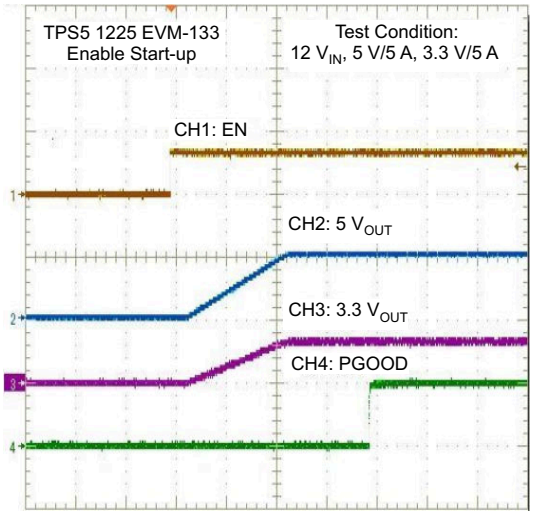

Figure 7-5. EN1 and EN2 Turn-On

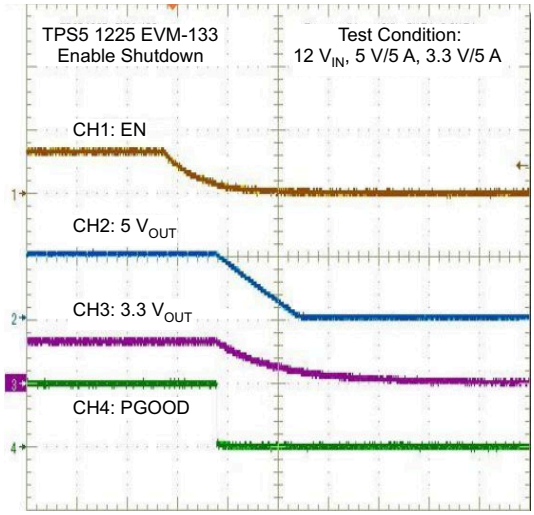

Figure 7-6. EN1 and EN2 Turn-Off

7.6 Output Ripple

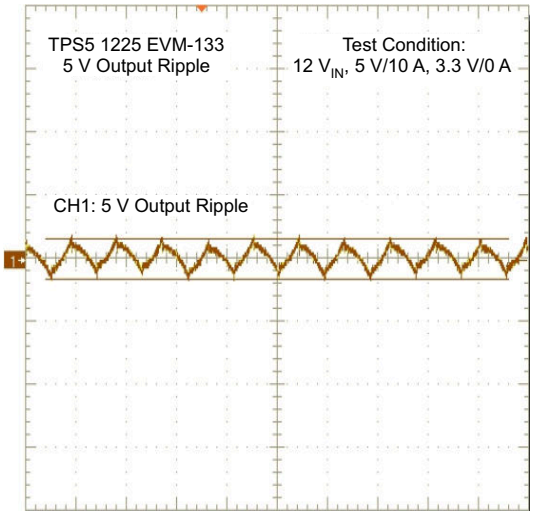

Figure 7-7. 5-V Output Ripple

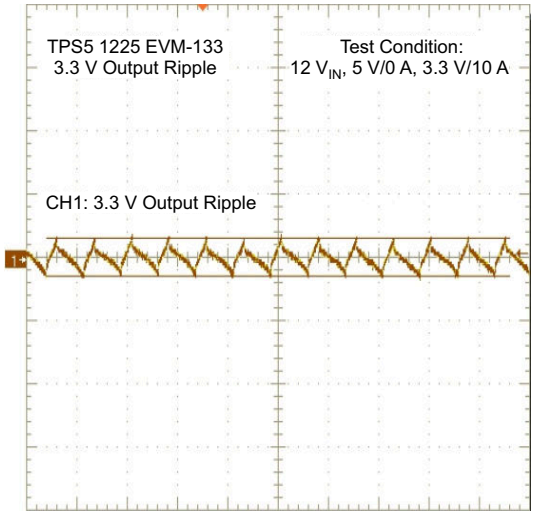

Figure 7-8. 3.3-V Output Ripple

7.7 Switching Node

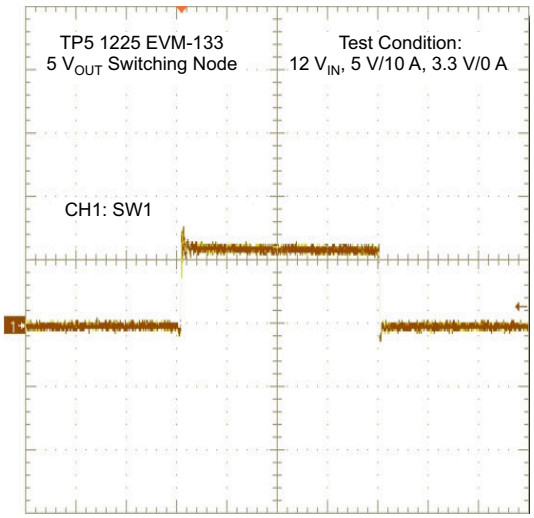

Figure 7-9. 5-V Switching Node

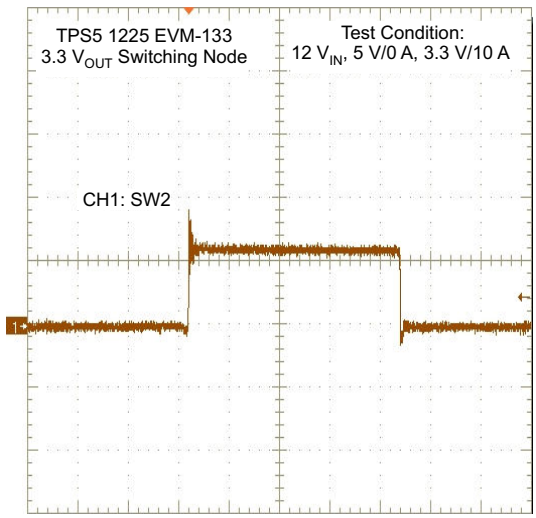

Figure 7-10. 3.3-V Switching Node

7.8 5-V Output Transient with Auto-skip Mode

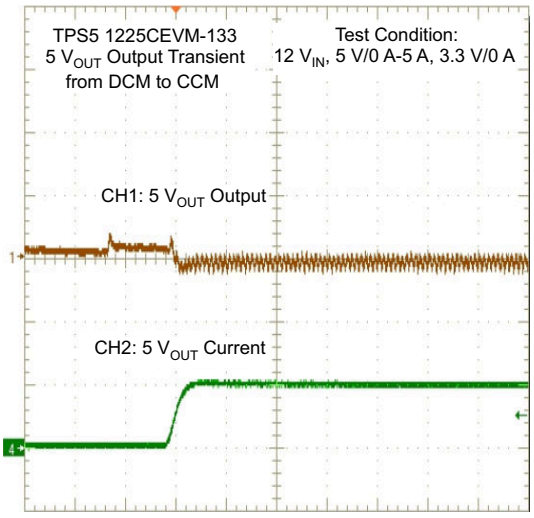

Figure 7-11. 5-V Output Transient from DCM to CCM

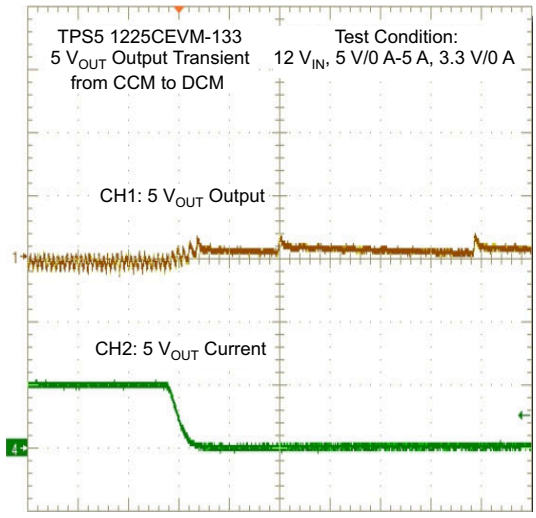

Figure 7-12. 5-V Output Transient from CCM to DCM

7.9 3.3-V Output Transient with Auto-skip Mode

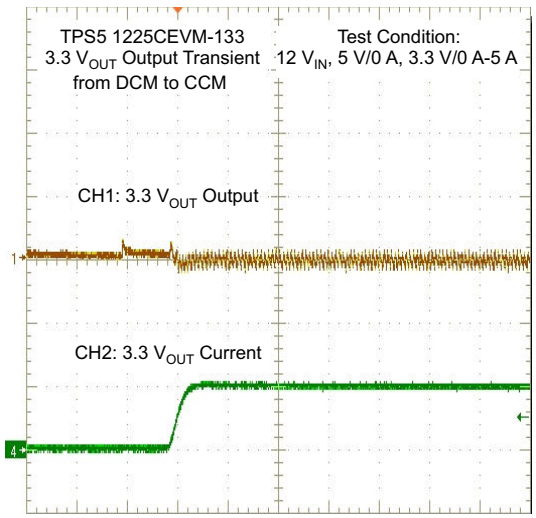

Figure 7-13. 3.3-V Output Transient from DCM to CCM

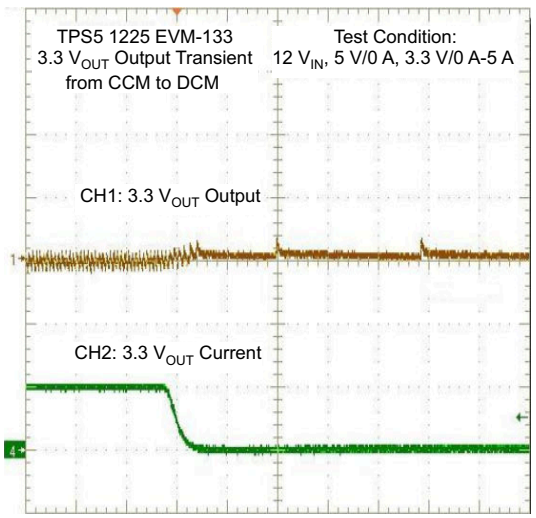

Figure 7-14. 3.3-V Output Transient from CCM to DCM

7.10 Output Prebias Turn-On

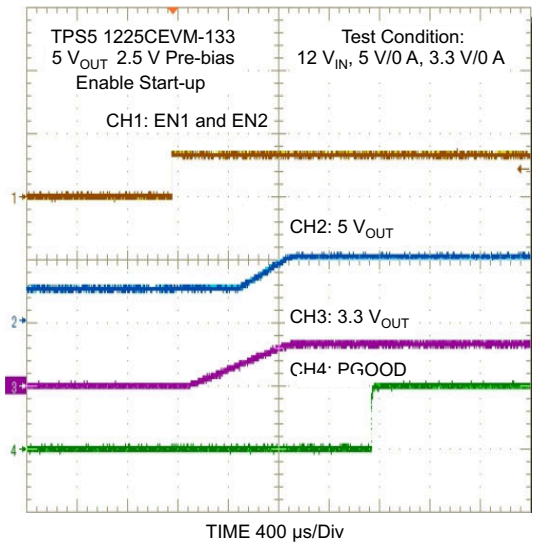

Figure 7-15. 5-V Output, 2.5-V Prebias Start-Up

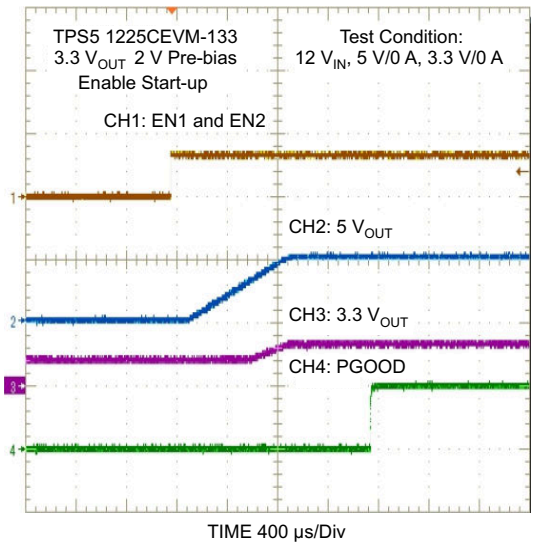

Figure 7-16. 3.3-V Output, 2-V Prebias Start-Up

7.11 Thermal Image

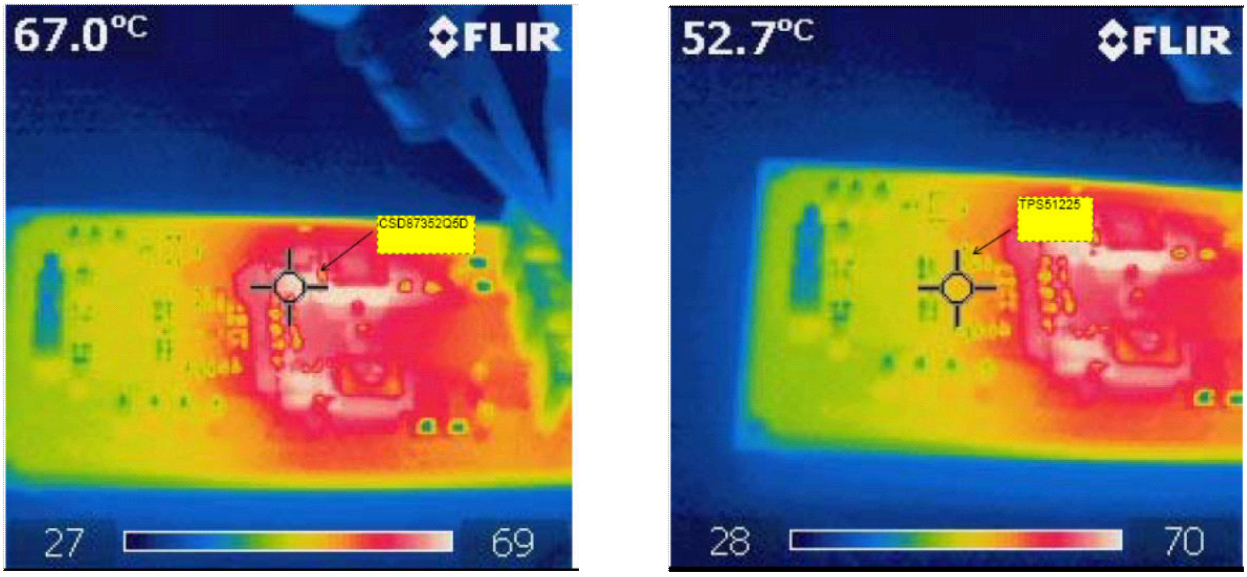

Figure 7-17. Top Board at 12 V_{IN}, 5 V/10 A, 3.3 V/10 A, 25°C Ambient Without Airflow

8 EVM Assembly Drawing and PCB Layout

The following figures (Figure 8-1 through Figure 8-6) show the design of the TPS51225EVM-133 printed circuit board. The EVM has been designed using four layers, 2-oz copper circuit board.

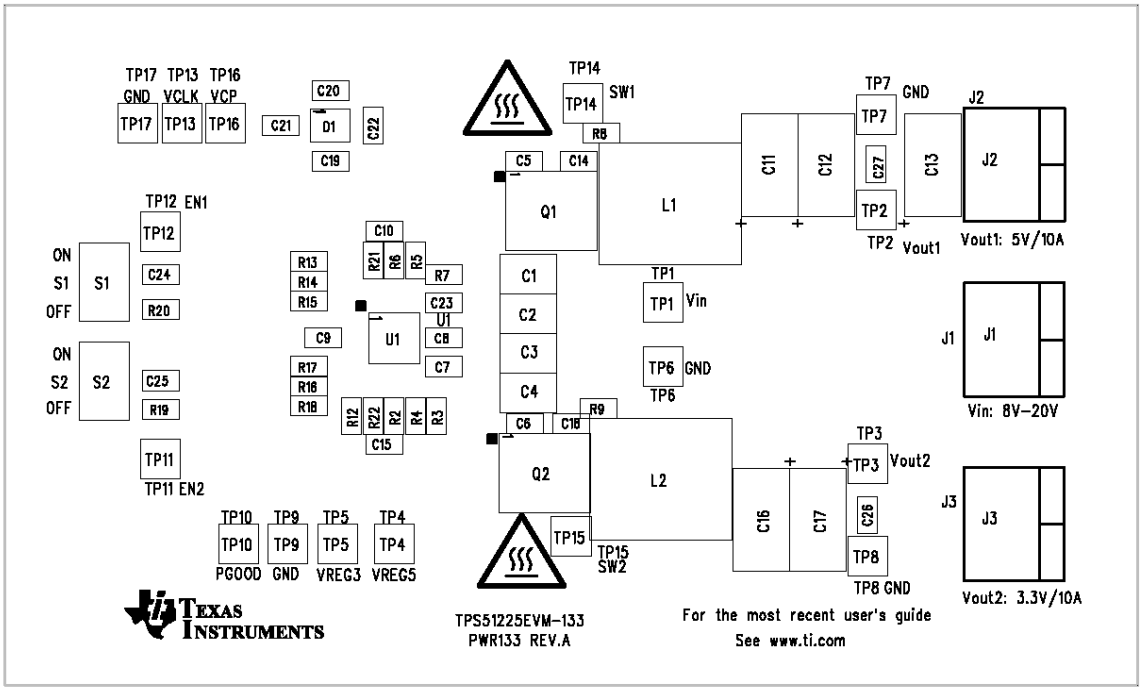

Figure 8-1. TPS51225EVM-133 Top Layer Assembly Drawing

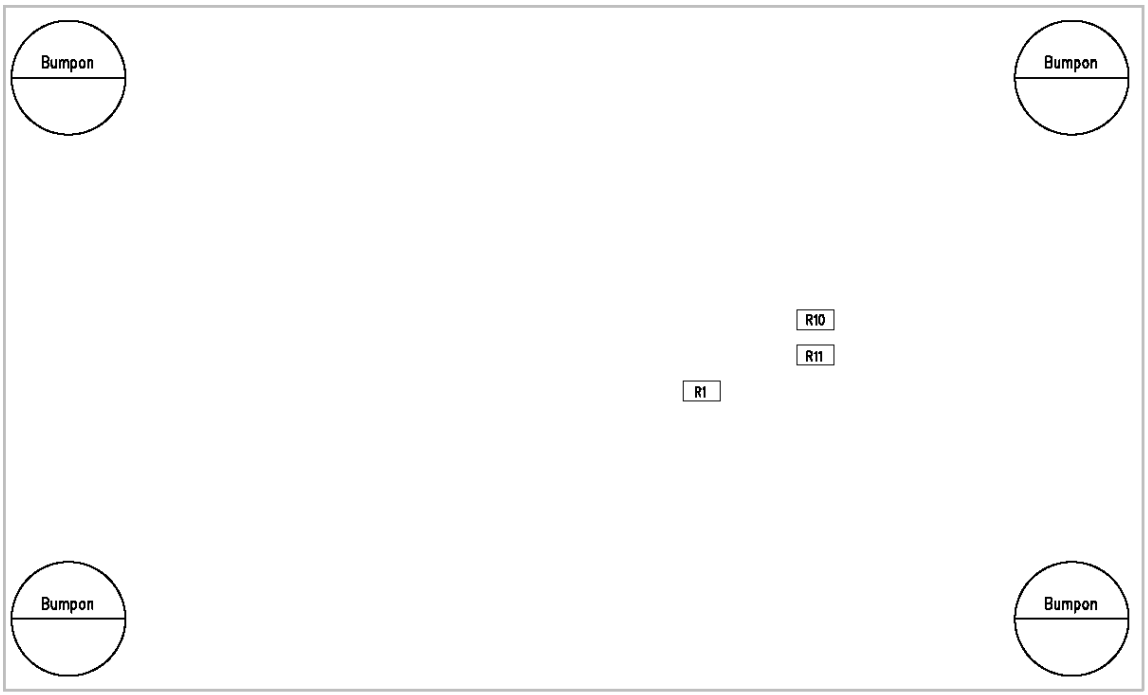

Figure 8-2. TPS51225EVM-133 Bottom Assembly Drawing

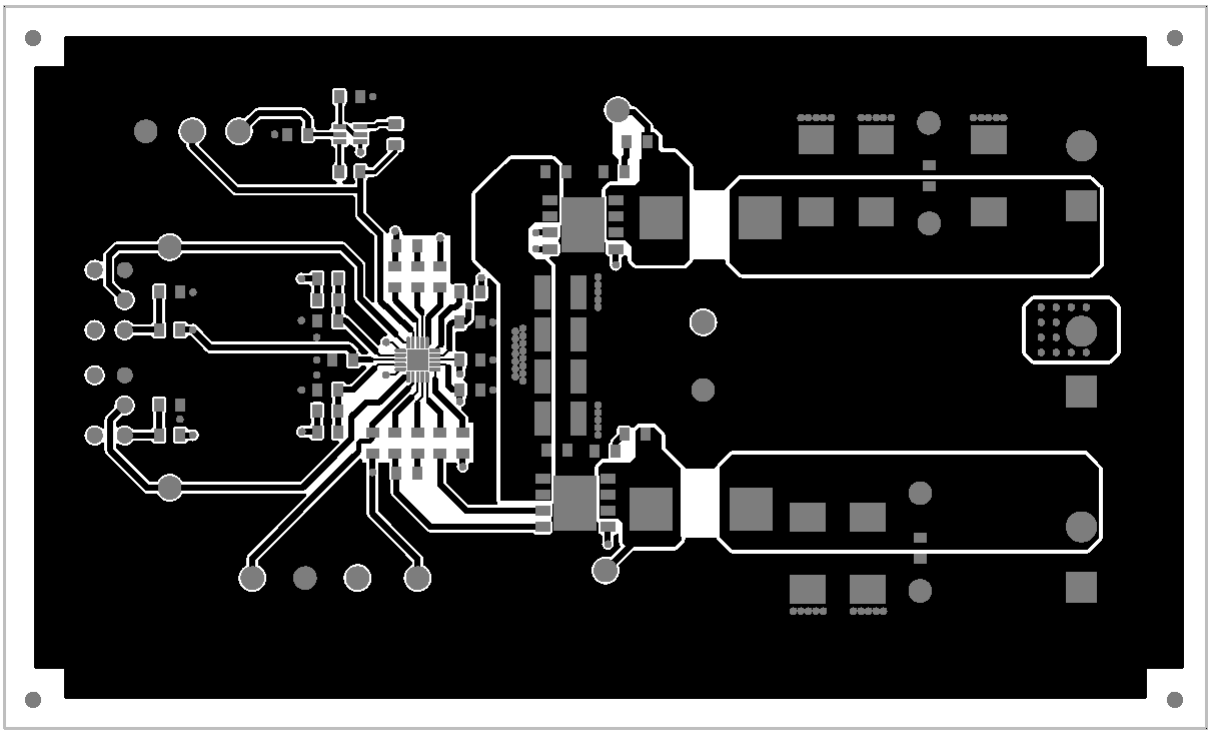

Figure 8-3. TPS51225EVM-133 Top Copper

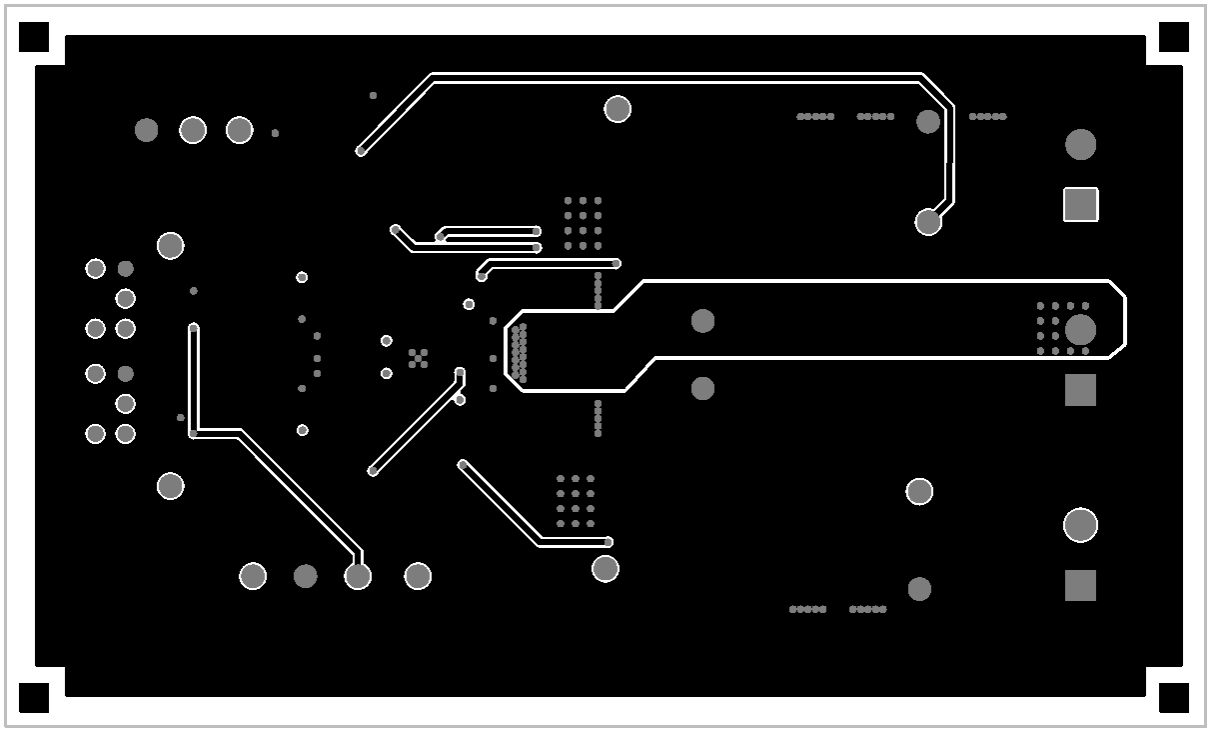

Figure 8-4. TPS51225EVM-133 Layer 2 Copper

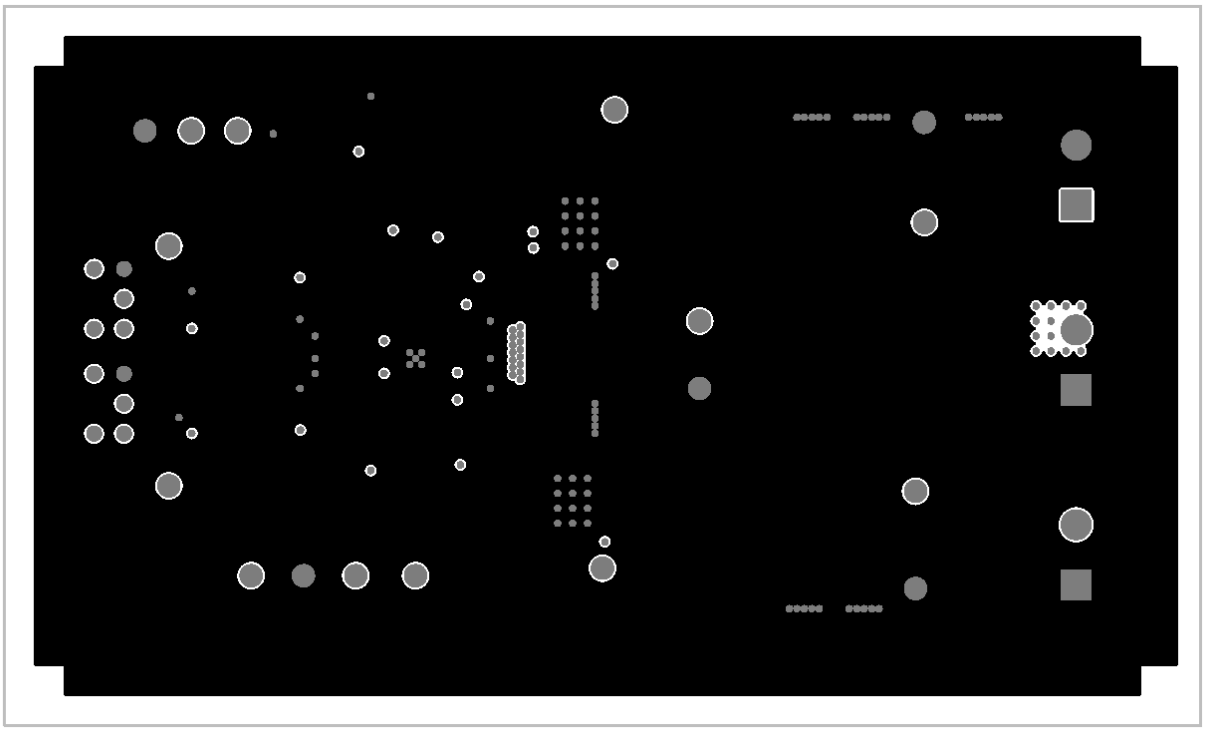

Figure 8-5. TPS51225EVM-133 Layer 3 Copper

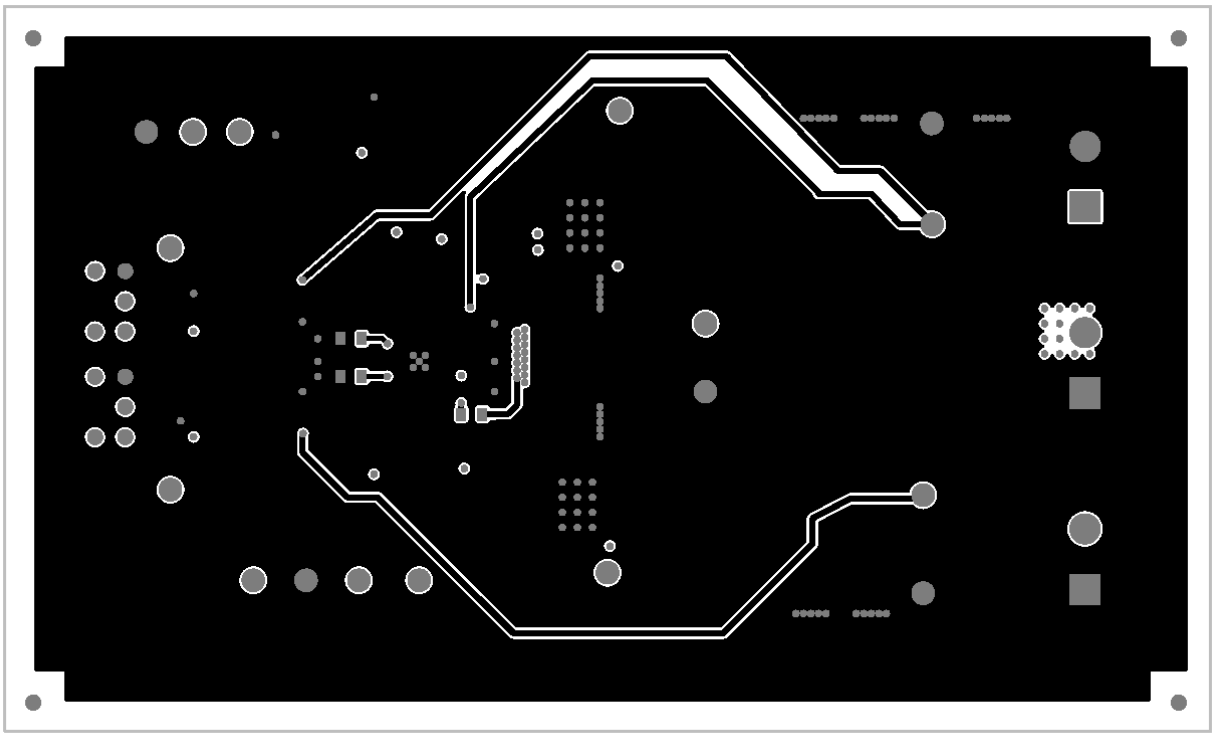

Figure 8-6. TPS51225EVM-133 Layer 4 Copper

9 Bill of Materials

This is the EVM components list according to the schematic shown in Figure 3-1.

Table 9-1. EVM Components List

Qty	RefDes	Description	MFR	Part Number
4	C1, C2, C3, C4	Capacitor, ceramic, 22 µF, 25 V, X5R, 20%, 1210	Murata	GRM32ER61C226KE20L
6	C10, C15, C19, C20, C21, C22	Capacitor, ceramic, 0.1 µF, 50 V, X7R, 10%, 0603	STD	STD
4	C5, C6, C26, C27	Capacitor, ceramic, 0.01 µF, 50 V, X7R, 10%, 0603	STD	STD
3	C7, C8, C9	Capacitor, ceramic, 1 µF, 10 V, X7R, 10%, 0603	STD	STD
2	C11, C12	Capacitor, POS, 330 µF, 6.3 VDC, 18 mΩ, 20%, 7343	Sanyo	6TPE330MIL
2	C16, C17	Capacitor, POS, 470 µF, 4 VDC, 18 mΩ, 20%, 7343	Sanyo	4TPE470MIL
1	D1	Diode, Schottky barrier array, 70 mA, 40 V, SOT363	BAS40DW-04	Diodes
1	L1	Inductor, SMT, 3.3 µH, 12.3 A, 9.2 mΩ, 11.2 mm × 10.0 mm	Toko	FDVE1040-H-3R3M
1	L2	Inductor, SMT, 2.2 µH, 14.2 A, 6.1 mΩ, 11.2 mm × 10.0 mm	Toko	FDVE1040-H-2R2M
2	Q1, Q2	MOSFET, Dual N-Chan, 30 V, 25 A, QFN-8 POWER	TI	CSD87352Q5D
9	R1, R3, R4, R5, R7, R19, R20, R21, R22	Resistor, chip, 0 Ω, 1/16W, 1%, 0603	STD	STD
2	R10, R11	Resistor, chip, 30.1 kΩ, 1/16W, 1%, 0603	STD	STD
1	R18	Resistor, chip, 51.1 kΩ, 1/16W, 1%, 0603	STD	STD
1	R12	Resistor, chip, 100 kΩ, 1/16W, 1%, 0603	STD	STD
1	R14	Resistor, chip, 15.0 kΩ, 1/16W, 1%, 0603	STD	STD
2	R15, R17	Resistor, chip, 10.0 kΩ, 1/16W, 1%, 0603	STD	STD
1	R16	Resistor, chip, 7.50 kΩ, 1/16W, 1%, 0603	STD	STD
1	R6	Resistor, chip, 2.21 Ω, 1/16W, 1%, 0603	STD	STD
1	R2	Resistor, chip, 4.02 Ω, 1/16W, 1%, 0603	STD	STD
1	U1	IC, Dual Synchronous Step-Down Controller with 5-V/3.3-V LDOs for Notebook System Power DFN-20	TI	TPS51225RUK

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (June 2012) to Revision A (February 2022) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document. 3
- Updated the user's guide title..... 3

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