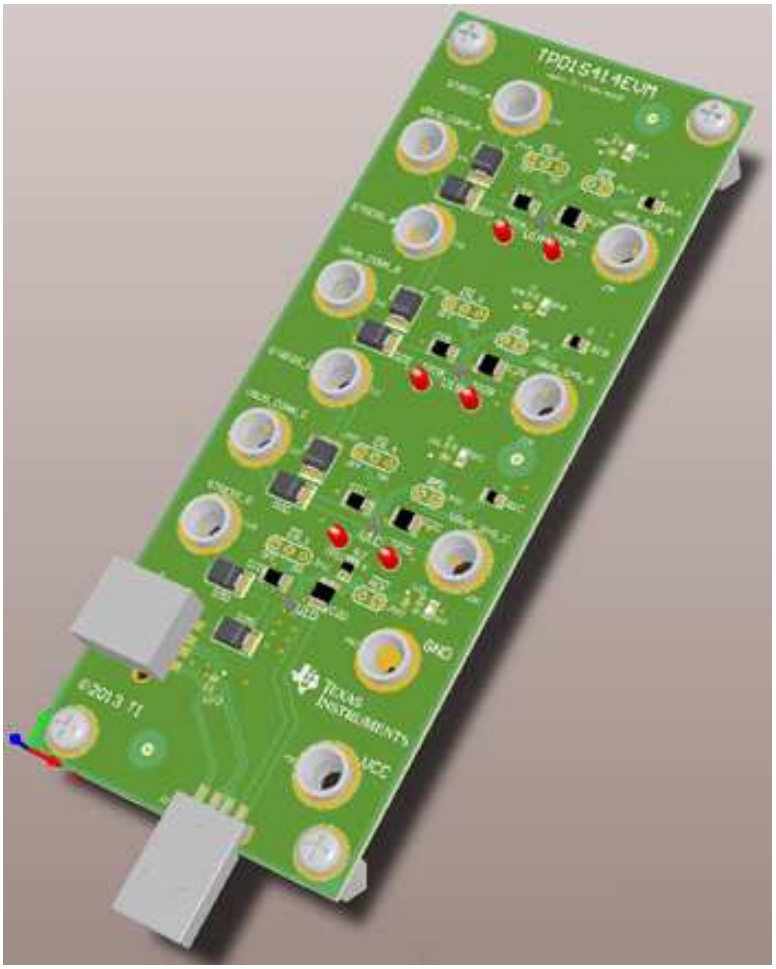
TPD1S414EVM

This user's guide describes the characteristics, operation, and use of the TPD1S414EVM evaluation module (EVM). This EVM includes 4 TPD1S414's in various configurations for testing. Three TPD1S414's are configured for IEC61000-4-5 compliance testing; one TPD1S414 is configured for throughput on USB 2.0 Type A connectors for throughput analysis. This user's guide includes setup instructions, schematic diagrams, a bill of materials, and printed-circuit board layout drawings for the EVM.



1 Introduction

Texas Instrument's TPD1S414 evaluation module helps designers evaluate the operation and performance of the TPD1S414 device. The TPD1S414 is a single-chip solution for USB connector's VBUS line protection. The bi-directional nFET switch ensures safe current flow in both charging and host mode while protecting the internal system circuits from any over-voltage conditions at the V_{BUS_CON} pin. On the V_{BUS_CON} pin, this device can handle over-voltage protection up to 30 V. After the $\overline{EN}$ pin toggles low, the TPD1S414 waits 15 ms before turning ON the nFET through a soft start delay. $\overline{ACK}$ pin indicates the FET is completely turned ON.

Table 1. EVM Configuration

Reference Designator	TI Part Number	Configuration
U1A-U1C	TPD1S414	Surge
U1D and U3	TPD1S414 and TPD3E001	Surge and ESD

2 Board Setup

This section describes the intended use of the TPD1S414EVM. A generalized outline of the procedure given in IEC-61000-4-5 is described here. IEC-61000-4-5 should be referred to for a more specific testing outline.

2.1 U1A – U1C

Three separate and identical test setups for TPD1S414 (U1A – U1C) are pinned out to allow evaluating device performance during normal operating conditions as well as during surge events. V_{BUS_CON} is J1A – J1C and V_{BUS_SYS} is J3A – J3C. Surge can be injected onto V_{BUS_CON} using J2A – J2C. A Schottky Barrier Diode (D2A – D2C) protects equipment attached to J1x from any surge (up to 90 V DC) injected on J2x. Another Schottky Barrier Diode (D3A – D3C) prevents V_{BUS_CON} from back driving voltage into the surge tester, which can cause the surge tester problems with outputting an IEC61000-4-5 compliant signal.

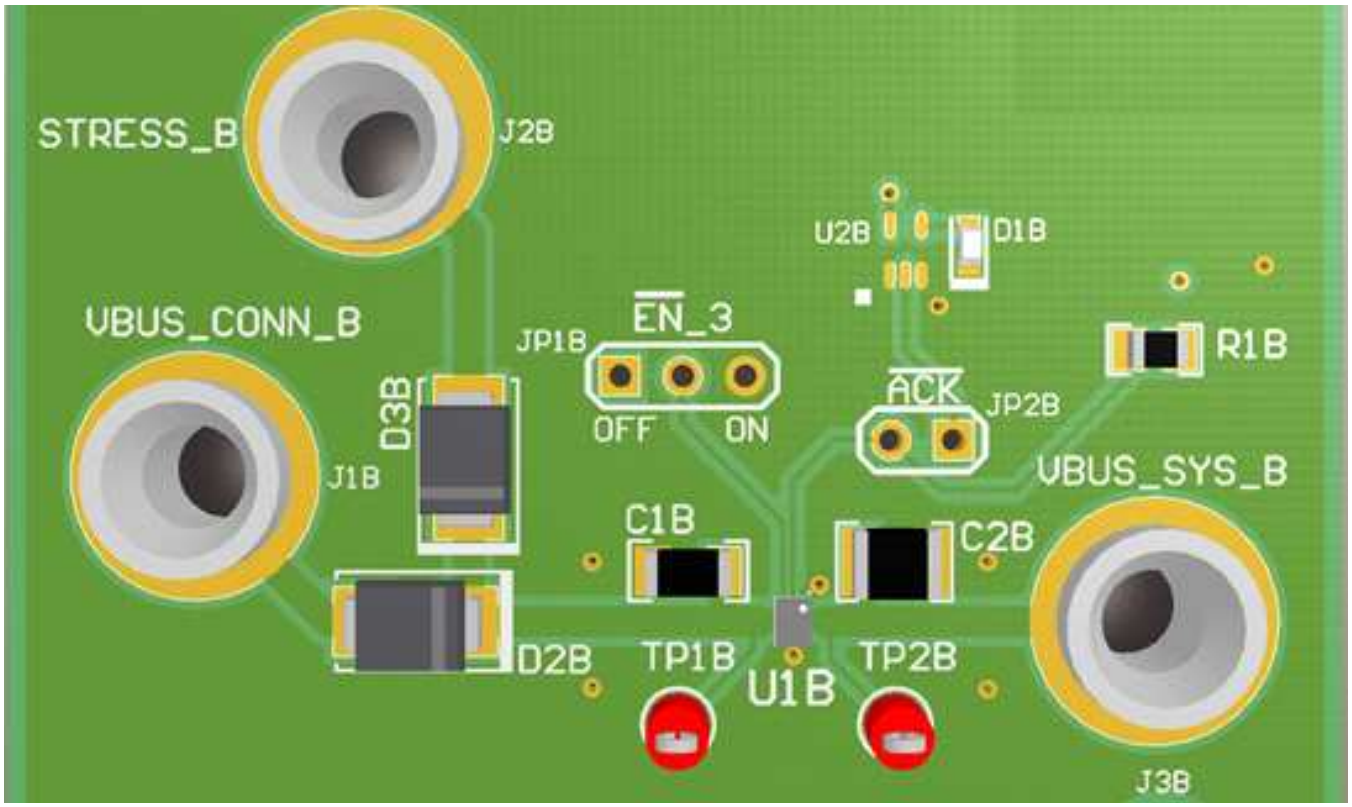


Figure 1. TPD1S414 Board Configuration for U1A – U1C

Test points (TP1A – TP1C and TP2A – TP2C) provide Kelvin connections for monitoring the voltage drop across U1A – U1C during surge events as well as for measuring R_{DYN} while current is flowing through TPD1S414. A 3-pin header (JP1A – JP1C) allows shunting the $\overline{EN}$ pin (JP1A – JP1C) on or off. A 2-pin header (JP2A – JP2C) allows monitoring $\overline{ACK}$ by observing an LED (D1A – D1C) with a shunt installed, or by measuring the voltage by clipping to the TPD1S414 side of JP2x. All testing requires +5V applied to VCC (PS1) and ground to GND (PS2).

2.2 U1D

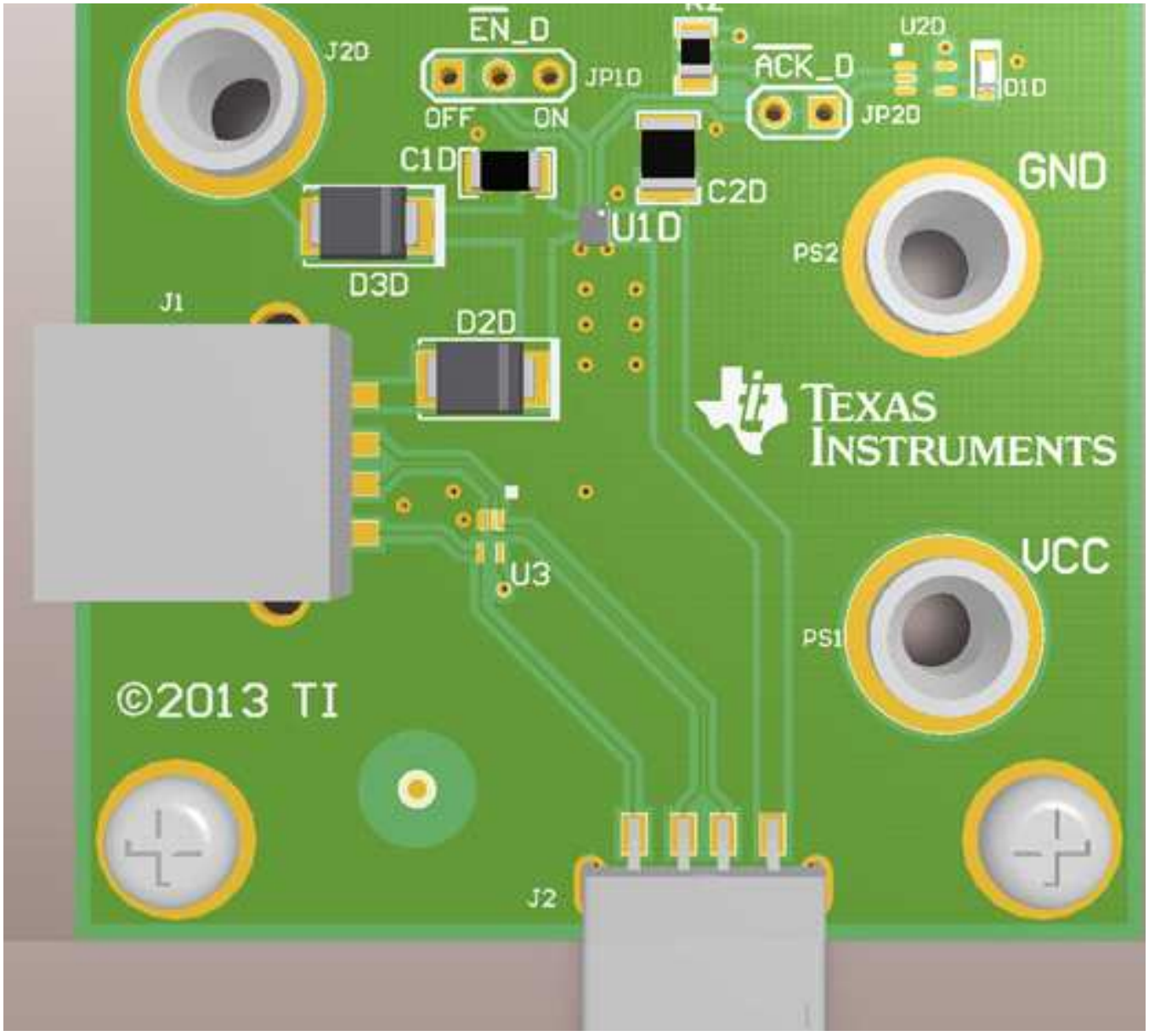


Figure 2. TPD1S414 Board Configuration for U1D

A pass through USB2.0 port is included for system level testing. The female USB connector (J1) is the "Connector" side of TPD1S414 and a male USB connector (J2) is the "System" side. ESD protection has been added to the Hi-Speed data lines and ID pin in the form of TPD3E001DRL to complete the port protection example scheme.

Surge can be injected onto V_{BUS_CON} using J2D. A Schottky Barrier Diode (D2D) protects equipment attached to J1 from any surge (up to 90 V DC) injected on J2D. Another Schottky Barrier Diode (D3D) prevents V_{BUS_CON} from back driving voltage into the surge tester, which can cause the surge tester problems with outputting an IEC61000-4-5 compliant signal.

A 3-pin header (JP1D) allows shunting the $\overline{EN}$ pin (JP1D) on or off. A 2-pin header (JP2D) allows monitoring $\overline{ACK}$ by observing an LED (D1D) with a shunt installed, or by measuring the voltage by clipping to the TPD1S414 side of JP2D. All testing requires +5V applied to VCC (PS1) and ground to GND (PS2).

3 Bill of Materials

Table 2. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
C1A, C1B, C1C, C1D	4	1uF	CAP, CERM, 1uF, 25V, +/-10%, X7R, 1206	1206	12063C105KAT2A	AVX
C2A, C2B, C2C, C2D	4	2.2uF	CAP, CERM, 2.2uF, 100V, +/-10%, X7R, 1210	1210	GRM32ER72A225KA35L	MuRata
D1A, D1B, D1C, D1D	4	Red	LED, Green, SMD	1.6 x 0.8 x 0.8 mm	LTST-C190GKT	Lite-On
D2A, D2B, D2C, D2D, D3A, D3B, D3C, D3D	8	90V	Diode, Schottky, 90 V, 2 A, SMB	SMB	B290-13-F	Diodes Inc.
H1, H2, H3, H4	4		Machine Screw, Round, #4-40 x 1/4, Nylon, Philips pan head	Screw	NY PMS 440 0025 PH	B & F Fastener Supply
H5, H6, H7, H8	4		Standoff, Hex, 0.5"L #4-40 Nylon	Standoff	1902C	Keystone
J1	1		Connector, Receptacle, USB TYPE A, 4POS SMD	USB TYPE A CONNECTOR RECEPTACLE 4 POS SMD	896-43-004-00-000000	Mill-Max
J1A, J1B, J1C, J2A, J2B, J2C, J2D, J3A, J3B, J3C, PS1, PS2	12		Standard Banana Jack, Un-insulated, 5.5 mm	Keystone_575-4	575-4	Keystone
J2	1		Connector, USB Type A, 4POS R/A, SMD	USB Type A right angle	48037-1000	Molex
JP1A, JP1B, JP1C, JP1D	4	PEC03SAAN	Header, Male 3-pin, 100 mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
JP2A, JP2B, JP2C, JP2D	4	PEC02SAAN	Header, Male 2-pin, 100 mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
R1A, R1B, R1C, R2	4	4.3k	RES, 4.3 kΩ, 5%, 0.125W, 0805	0805	CRCW08054K30JNEA	Vishay-Dale
TP1A, TP1B, TP1C, TP2A, TP2B, TP2C	6	Red	Test Point, Miniature, Red, TH	Red Miniature Test point	5000	Keystone
U1A, U1B, U1C, U1D	4		USB CHARGER OVP SWITCH WITH ESD FOR VBUS_CON PIN, YFF0012ALAR	YFF0012ALAR	TPD1S414YFF	Texas Instruments
U2A, U2B, U2C, U2D	4	SN74LVC1G125DCK	IC, Single Bus Buffer Gate With 3-States Outputs, OE Active Low	DCK	SN74LVC1G125DCK	Texas Instruments
U3	1	TPD3E001DRLR	IC, LOW-CAPACITANCE 3-CHANNEL ±15-kV ESD-PROTECTION ARRAY FOR HIGH-SPEED DATA INTERFACES	SOP-5 (DRL)	TPD3E001DRLR	Texas Instruments

4 Schematics

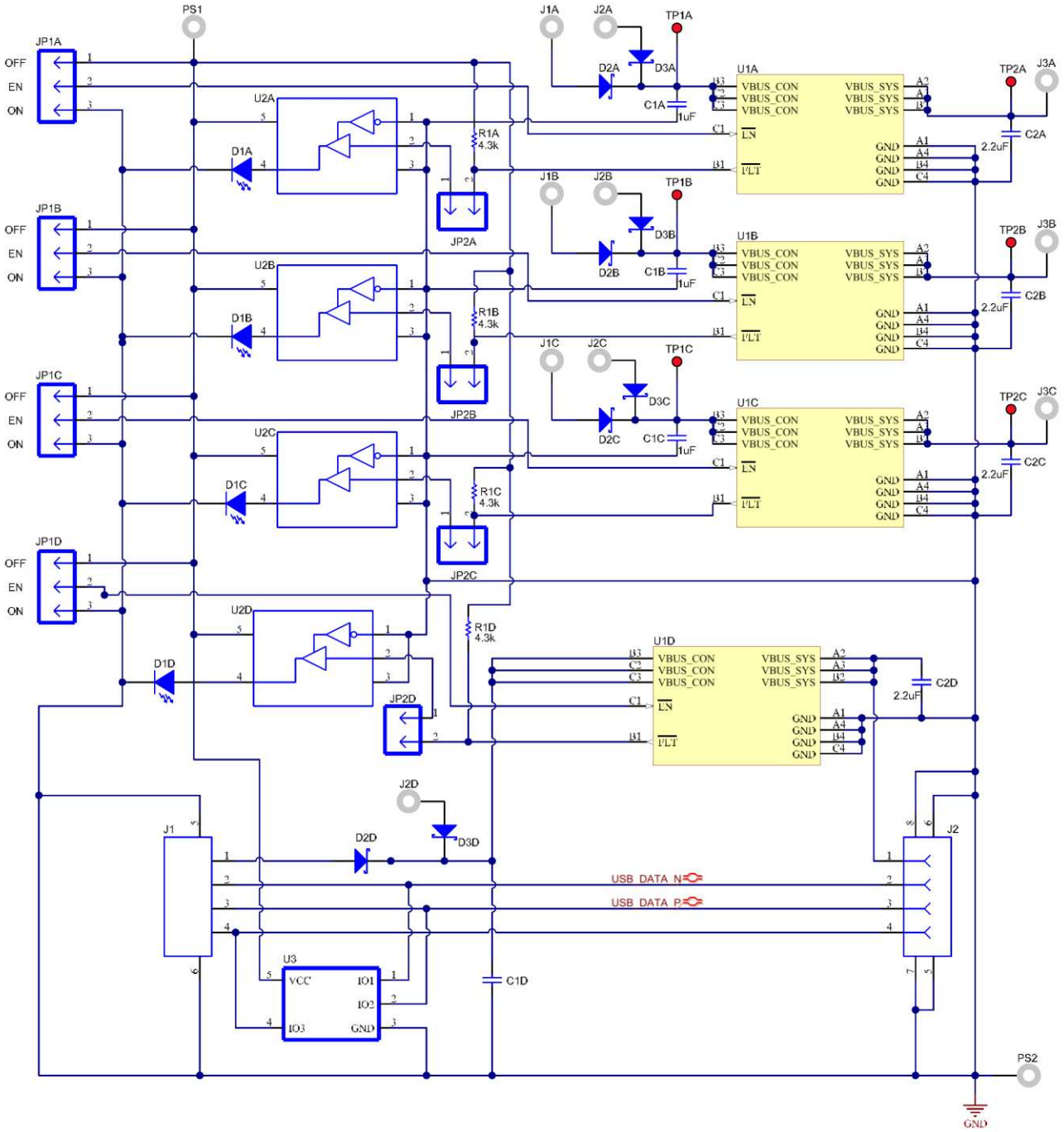


Figure 3. TPD1S414EVM Schematic

5 Board Layout

This section provides the TPD1S414EVM board layout. TPD1S414EVM is a 4-layer board of FR-4 at 0.062" thickness.

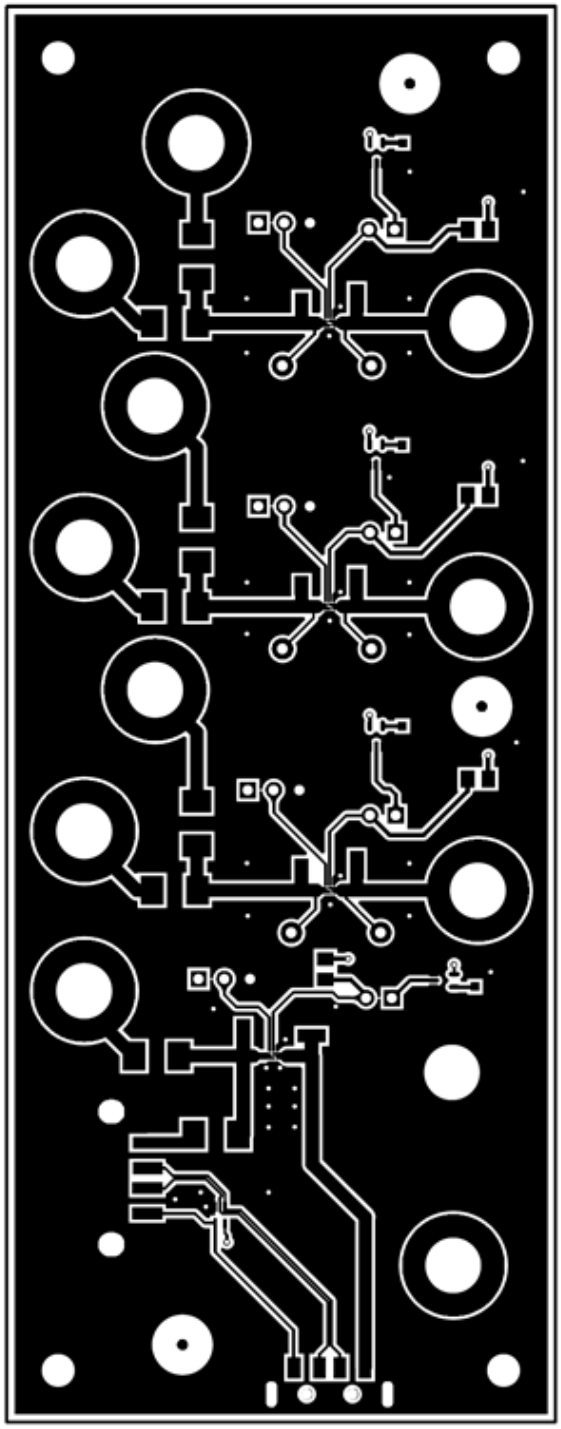


Figure 4. Top Layer Copper

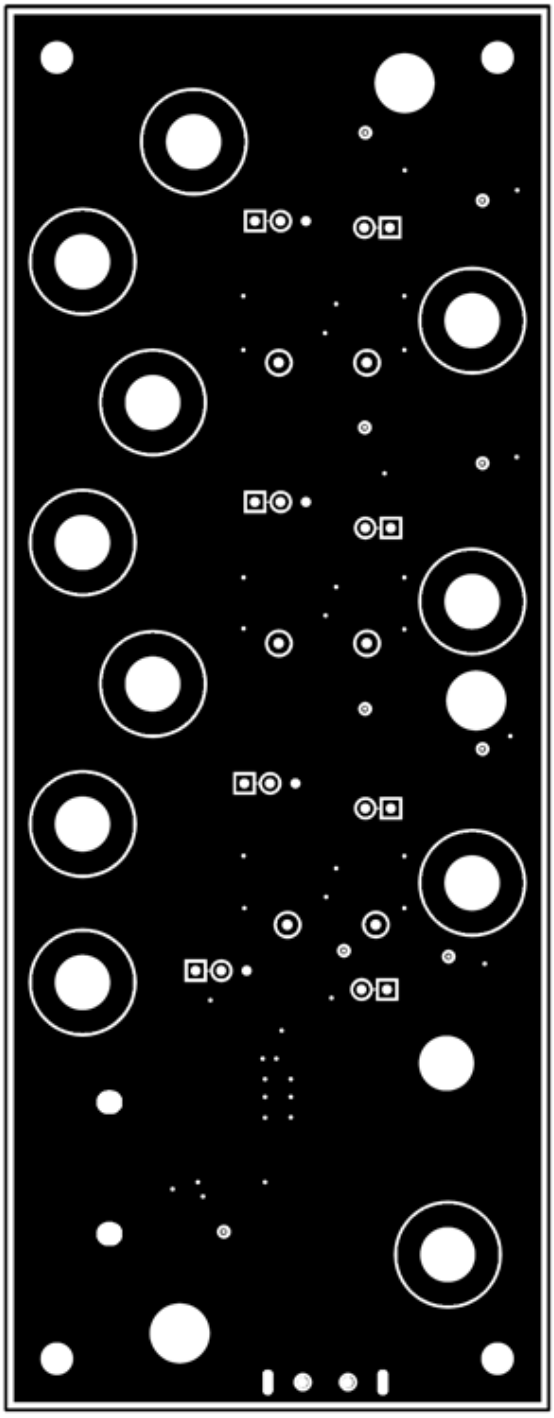


Figure 5. Bottom Layer Copper

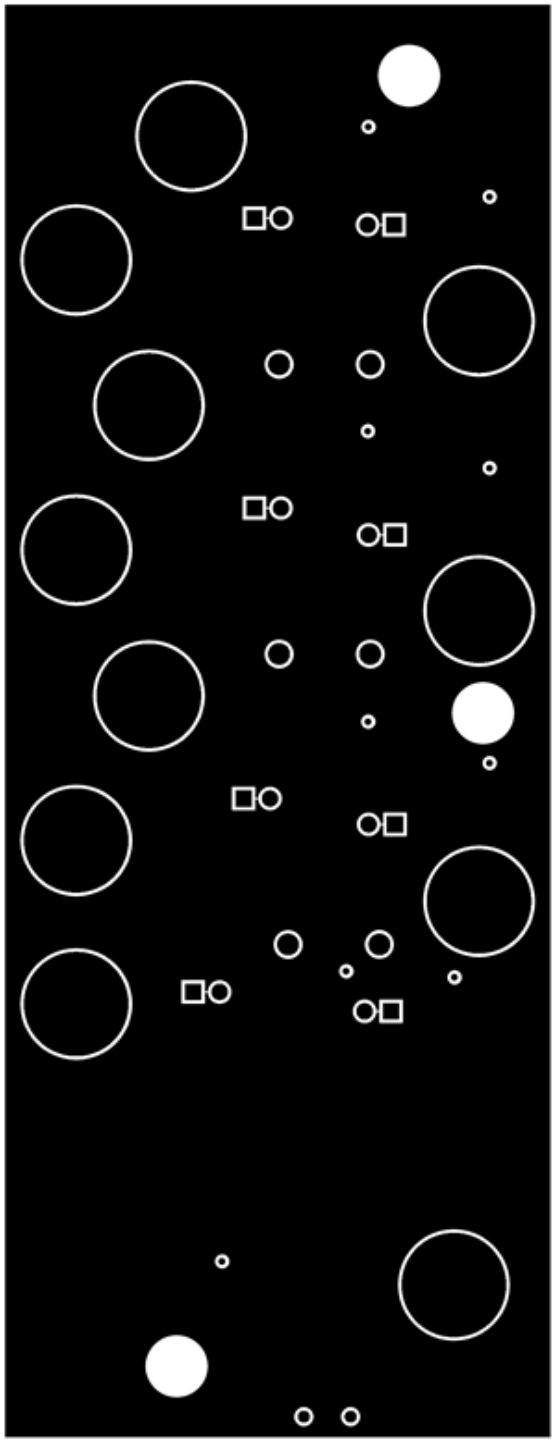


Figure 6. Layer 2 Copper

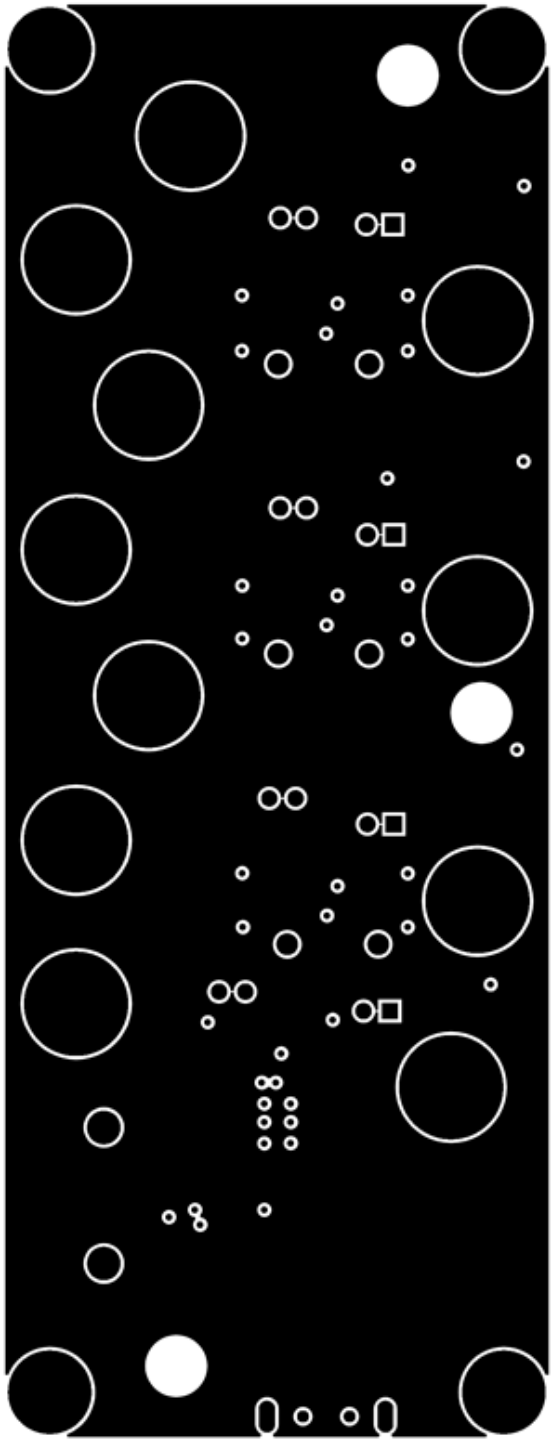


Figure 7. Layer 3 Copper

Revision History

Changes from Original (May 2015) to A Revision	Page
• Updated section order.	1
• Added Schematics section.	5

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