User's Guide

TPS65581 Buck Converter Evaluation Module User's Guide

ABSTRACT

This user's guide contains information for the TPS65581 as well as support documentation for the TPS65581EVM-575 evaluation module. Included are the performance specifications, board layouts, schematic, and the bill of materials of the TPS65581EVM-575.

Table of Contents

Trademarks

D-CAP2™ is a trademark of Texas Instruments.
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1 Introduction

The TPS65581 is a triple output, advanced D-CAP2™-mode, synchronous buck converter requiring a very low external component count. The advanced D-CAP2 control circuit is optimized for low-ESR output capacitors such as POSCAP, SP-CAP, or ceramic types and features fast transient response with no external compensation. The switching frequency is internally set at a nominal 700 kHz. The high-side and low-side switching MOSFETs are incorporated inside the TPS65580 package along with the gate-drive circuitry. The low drain-to-source on resistance of the MOSFETs allows the TPS65580 to achieve high efficiencies and helps keep the junction temperature low at high output currents. The TPS65580 dc/dc synchronous converter is designed to provide up to 1.5-A, 2.5-A and 1.5-A output for each of 3 channels from an input voltage source of 4.5 V to 18 V. The output voltage range is from 0.76 V to 6.5 V. Rated input voltage, output voltage and output current ranges for the evaluation module are given in Table 1-1. This user's guide describes the TPS65581EVM-575 performance.

Table 1-1. Input Voltage and Output Current Summary

EVM	Input Voltage Range	Channel	Output Voltage	Output Current Range
TPS65581EVM-575	V_{IN} = 4.5 V to 18 V	CH1	3.3 V	0-A to 1.5-A
		CH2	1.2 V	0-A to 2.5-A
		CH3	1.5 V	0-A to 1.5-A

2 Performance Specification Summary

A summary of the TPS65581EVM-575 performance specifications is provided in Table 2-1. Specifications are given for an input voltage of V_{IN} = 12 V and T_a = 25°C unless otherwise noted.

Table 2-1. TPS65581EVM-575 Performance Specifications Summary

Specifications		Test Conditions	Min	Typ	Max	Unit
Input voltage range (V_{IN})			4.5	12	18	V
Operating frequency				700		kHz
CH1	Output voltage			3.3		V
	Output current range		0		1.5	A
	Over current limit	V_{IN} = 12 V, L_O = 3.3 µH		2.0		A
	Output ripple voltage	V_{IN} = 12 V, I_O = 1.5 A		10		mV_{PP}
CH1	Output voltage			1.2		V
	Output current range		0		2.5	A
	Over current limit	V_{IN} = 12 V, L_O = 2.2 µH		3.5		A
	Output ripple voltage	V_{IN} = 12 V, I_O = 2.5 A		10		mV_{PP}
CH1	Output voltage			1.5		V
	Output current range		0		1.5	A
	Over current limit	V_{IN} = 12 V, L_O = 2.2 µH		2.0		A
	Output ripple voltage	V_{IN} = 12 V, I_O = 1.5 A		10		mV_{PP}

3 Modifications

These evaluation modules are designed to provide access to the features of the TPS65581. Some modifications can be made to this module.

3.1 Output Voltage Setpoint

To change the output voltage of the EVMs, it is necessary to change the value of the top resistor in the voltage set point divider network (R9, R13, and R17). Changing the value of R_{TOP} can change the output voltage above 0.765 V. The value of R_{TOP} for a specific output voltage can be calculated using Equation 1.

$$R_{TOP} = R_{BOT} \times \left(\frac{V_{OUT}}{0.764V} - 1 \right) \quad (1)$$

Table 3-1 lists the R_{TOP} values for some common output voltages. For higher output voltages of 1.8 V or above, a feed-forward capacitor (C_{FF}) may be required to improve phase margin. Pads for this component (C12, C18, and C24) are provided on the printed-circuit board. Note that the values given in Table 3-1 are standard values and not the exact value calculated using Equation 1.

Table 3-1. Output Voltages

Output Voltage (V)	R_{TOP} (kΩ)	R_{BOT} (kΩ)	C_{FF} (pF)	L_{OUT} (µH)			C_{OUT} (µF)
				Min	Typ	Max	
1.0	.681	2.21	220 - 680	1.5	2.2	3.3	22 - 68
1.05	.825	2.21	100 - 680	1.5	2.2	3.3	22 - 68
1.2	1.27	2.21	68 - 680	1.5	2.2	3.3	22 - 68
1.5	2.10	2.21	68 - 330	1.5	2.2	3.3	22 - 68
1.8	3.01	2.21	5 - 68	1.5	2.2	3.3	22 - 68
2.5	4.99	2.21	5 - 22	2.2	3.3	4.7	22 - 68
3.3	7.32	2.21	5 - 22	2.2	3.3	4.7	22 - 68
5.0	12.4	2.21	5 - 22	2.2	3.3	4.7	22 - 68
6.5	16.5	2.21	5 - 22	2.2	3.3	4.7	22 - 68

4 Test Setup and Results

This section describes how to properly connect, set up, and use the TPS65581EVM-575. The section also includes test results typical for the evaluation modules and efficiency, output load regulation, output line regulation, load transient response, output voltage ripple, input voltage ripple, start-up, and switching frequency.

4.1 Input/Output Connections

The TPS65581EVM-575 is provided with input/output connectors and test points as shown in Table 4-1. A power supply capable of supplying 5 A must be connected to J1 through a pair of 20-AWG wires. The loads must be connected to J2, J3 and J4 through pairs of 20-AWG wires. The maximum load current capability is for each channel is shown in Table 1-1. Wire lengths must be minimized to reduce losses in the wires. Test point TP1 provides a place to monitor the V_{IN} input voltages with TP2 providing a convenient ground reference. Test points TP11, TP15 and TP19 are used to monitor the output voltage for each of the three channels. Test points TP12, TP18 and TP20 are used as the ground reference for each of the three channels.

Table 4-1. Connections and Test Points

Reference Designator	Function
J1	V_{IN} (see Table 1-1 for V_{IN} range)
J2	CH1 V_{OUT}, 3.3 V at 1.5-A maximum
J3	CH2 V_{OUT}, 1.2 V at 2.5-A maximum
J4	CH3 V_{OUT}, 1.5 V at 1.5-A maximum
JP1	CH1 EN control. Jumper JP1-2 to JP1-3 to disable, jumper JP1-2 to JP1-1 to enable.
JP2	CH2 EN control. Jumper JP2-2 to JP2-3 to disable, jumper JP2-2 to JP2-1 to enable.
JP3	CH3 EN control. Jumper JP3-2 to JP3-3 to disable, jumper JP3-2 to JP3-1 to enable.
TP1	V_{IN} test point at V_{IN} connector
TP2	GND test point at V_{IN}
TP3	CH1 EN test point
TP4	CH2 EN test point
TP5	CH3 EN test point
TP6	Power good test point
TP7	Power ground test point
TP8	Analog ground test point
TP9	CH1 switch node test point
TP10	CH1 loop response test point
TP11	CH1 output voltage test point
TP12	CH1 ground test point at output connector
TP13	CH2 switch node test point
TP14	CH2 loop response test point
TP15	CH2 output voltage test point
TP16	CH2 ground test point at output connector
TP17	CH3 switch node test point
TP18	CH3 loop response test point
TP19	CH3 output voltage test point
TP20	CH3 ground test point at output connector

4.2 Start-Up Procedure

1. Ensure that the jumpers at JP1 (CH1 Enable control), JP2 (CH2 Enable control) and JP3 (CH3 Enable control) is set from ON to OFF
2. Apply appropriate V_{IN} voltage to VIN and GND terminals at J1
3. Set the jumpers at JP1 (CH1 Enable control), JP2 (CH2 Enable control) and JP3 (CH3 Enable control) to ON. The EVM enables the output voltages for each of the three channels.

4.3 Efficiency

Figure 4-1 shows the efficiency for the TPS65581EVM-575 CH1.

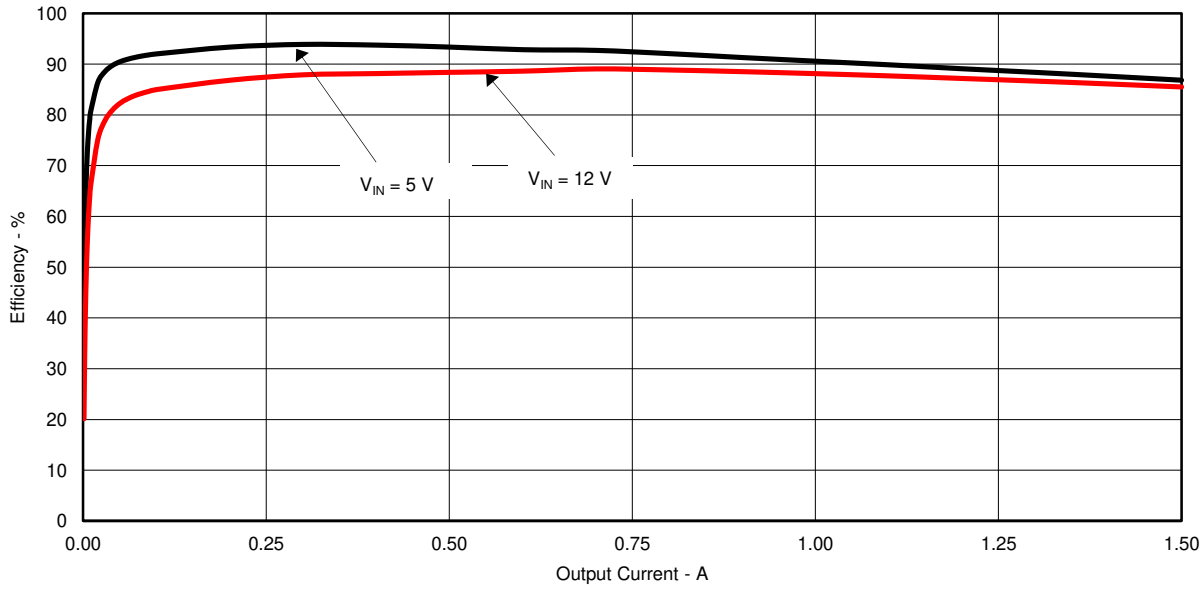

Figure 4-1. TPS65581EVM-575 CH1 Efficiency

Figure 4-2 shows the efficiency at light loads for the TPS65581EVM-575 CH1.

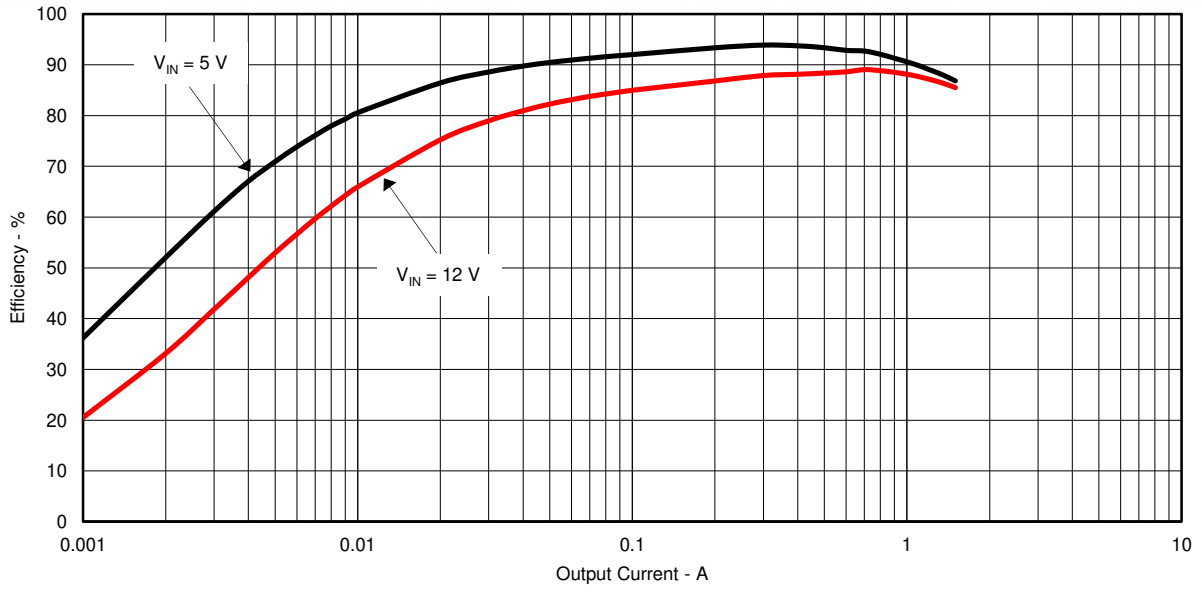

Figure 4-2. TPS65581EVM-575 Light CH1 Load Efficiency

Figure 4-3 shows the efficiency for the TPS65581EVM-575 CH2.

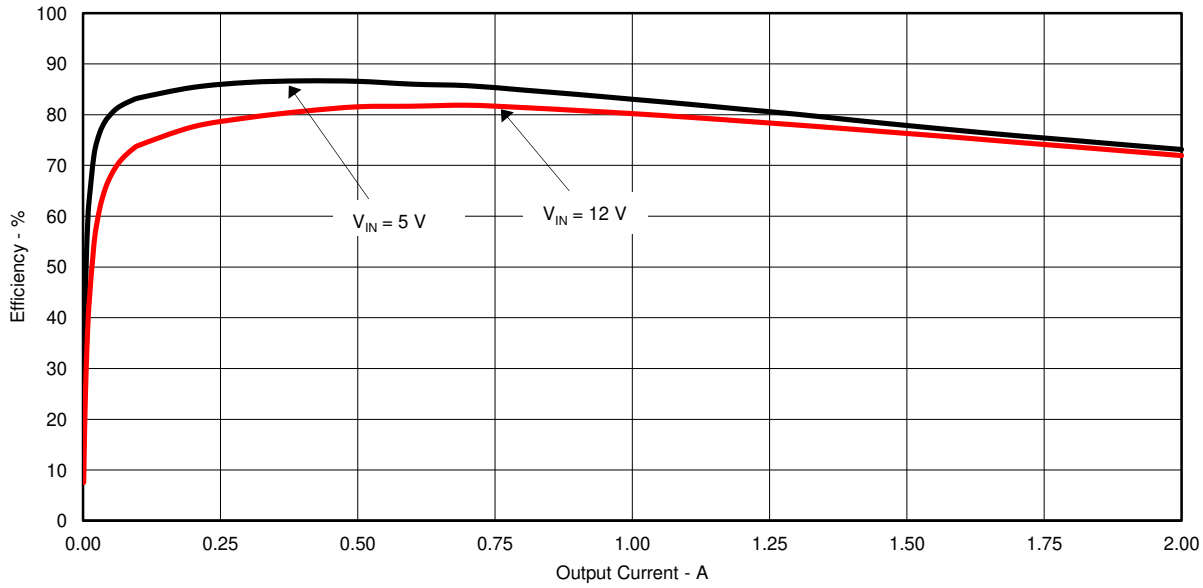

Figure 4-3. TPS65581EVM-575 CH2 Efficiency

Figure 4-4 shows the efficiency at light loads for the TPS65581EVM-575 CH2.

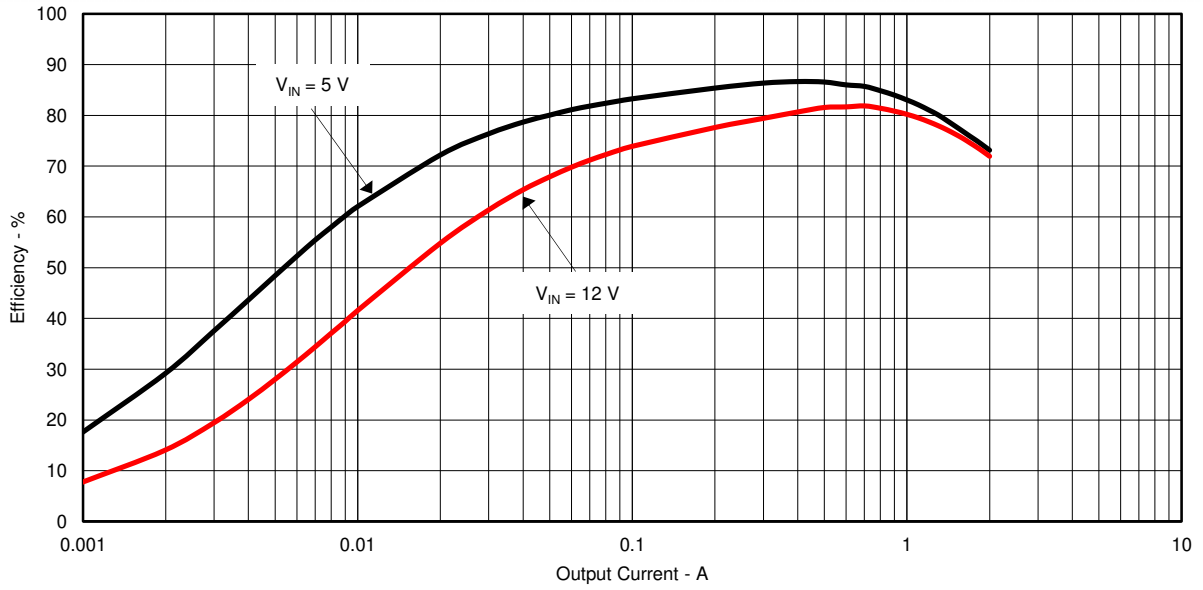

Figure 4-4. TPS65581EVM-575 Light CH2 Load Efficiency

Figure 4-5 shows the efficiency for the TPS65581EVM-575 CH3.

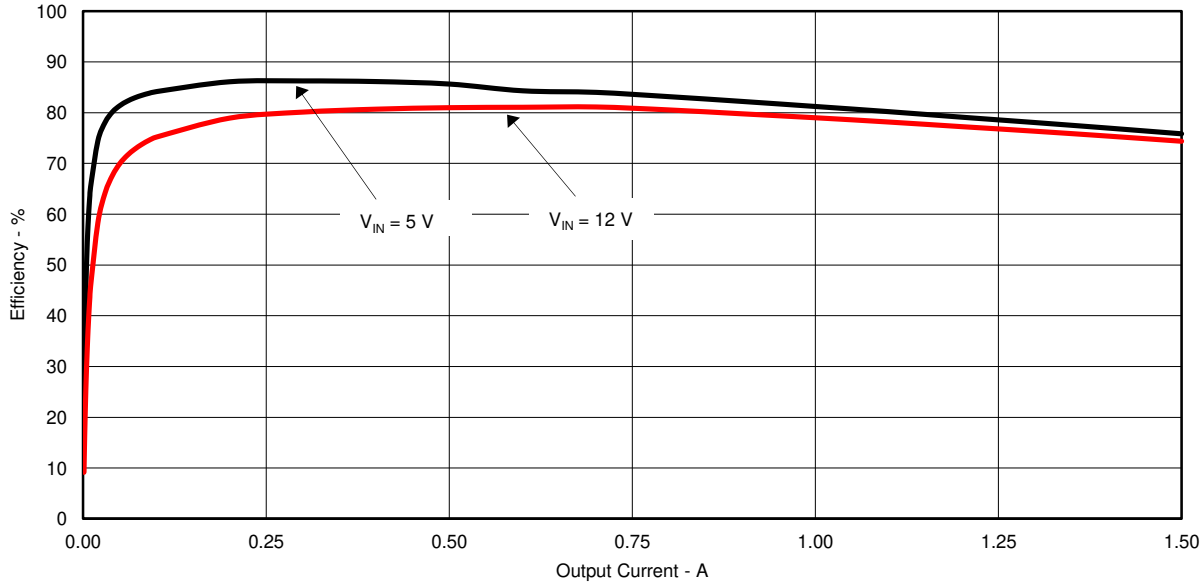

Figure 4-5. TPS65581EVM-575 CH3 Efficiency

Figure 4-6 shows the efficiency at light loads for the TPS65581EVM-575 CH3.

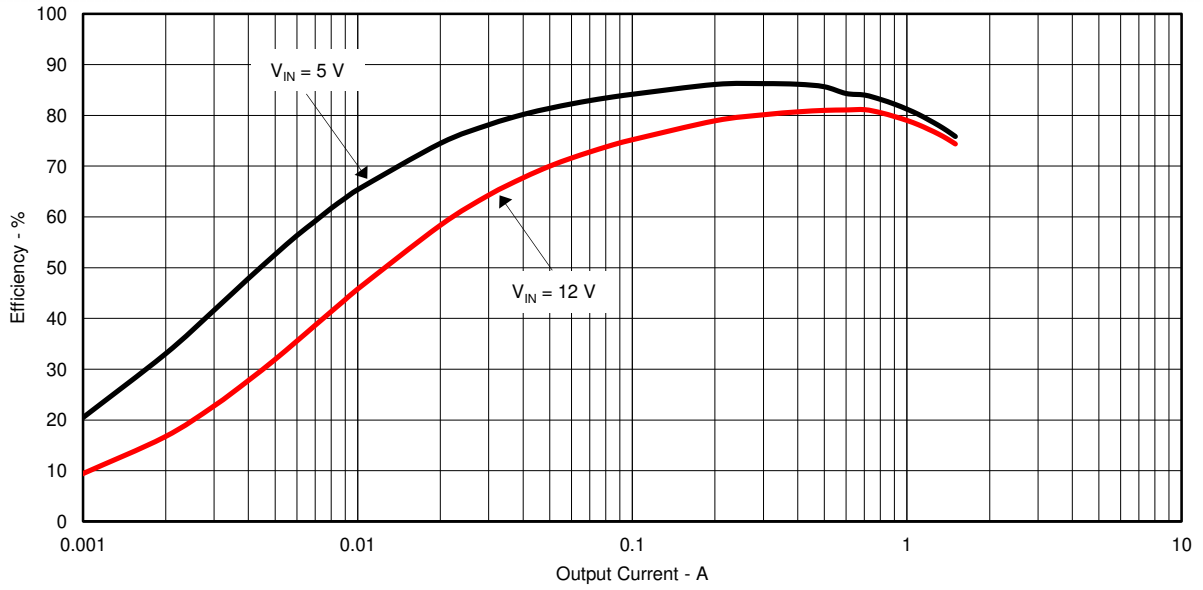

Figure 4-6. TPS65581EVM-575 Light CH3 Load Efficiency

4.4 Load Regulation

The load regulation for the TPS65581EVM-575 CH1 is shown in Figure 4-7. The load regulation for CH2 and CH3 is similar and is not shown.

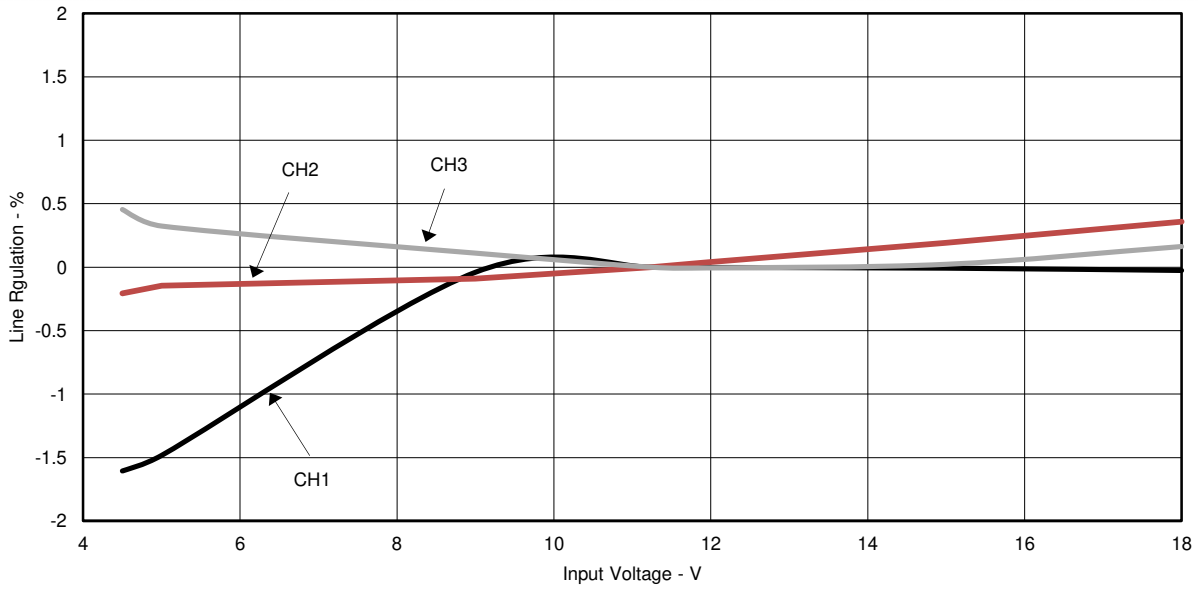

Figure 4-7. TPS65581EVM-575 CH1 Load Regulation

4.5 Line Regulation

The line regulation for the TPS65581EVM-575 CH1, CH2, and CH3 is shown in Figure 4-8. Note that the CH1 output voltage is 3.3 V and the line regulation is lessened as V_{IN} approaches V_{OUT}.

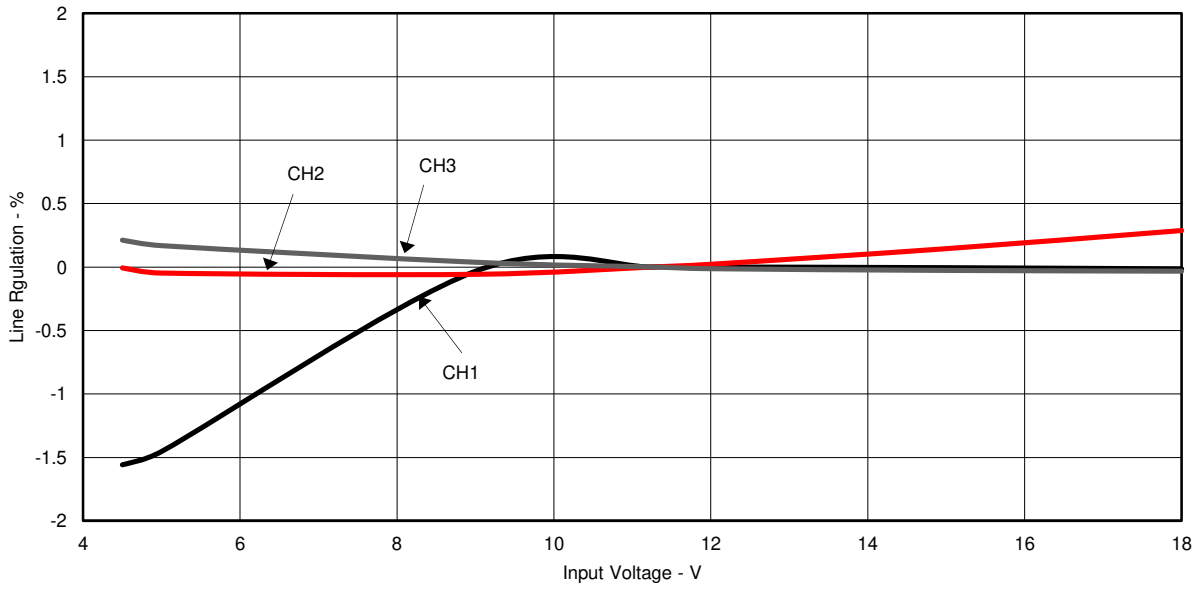

Figure 4-8. TPS65581EVM-575 Line Regulation

4.6 Load Transient Response

The TPS65581EVM-575 CH1 response to load transients is shown in Figure 4-9. The current steps and slew rates are indicated in the figures. Total peak-to-peak voltage variation is as shown. The transient response for CH2 and CH3 is similar and is not shown.

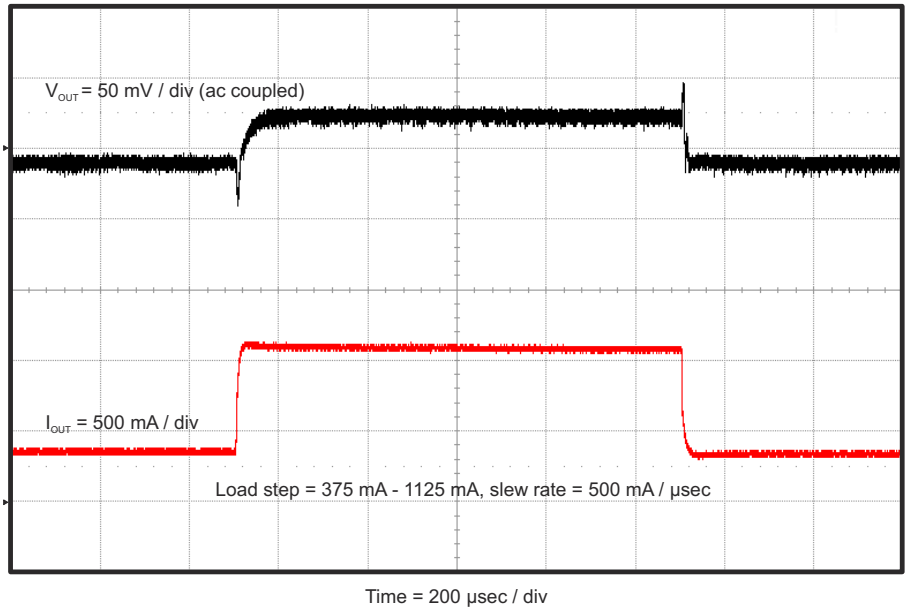

Figure 4-9. TPS65581EVM-575 CH1 Load Transient Response, 25% to 75% Load Step

4.7 Input Voltage Ripple

The TPS65581EVM-575 input voltage ripple is shown in Figure 4-10. The output current for each channel is the full rated load of 1.5-A, 2.5-A and 1.5-A. Note that the switching waveforms for each channel are out of phase to reduce input ripple.

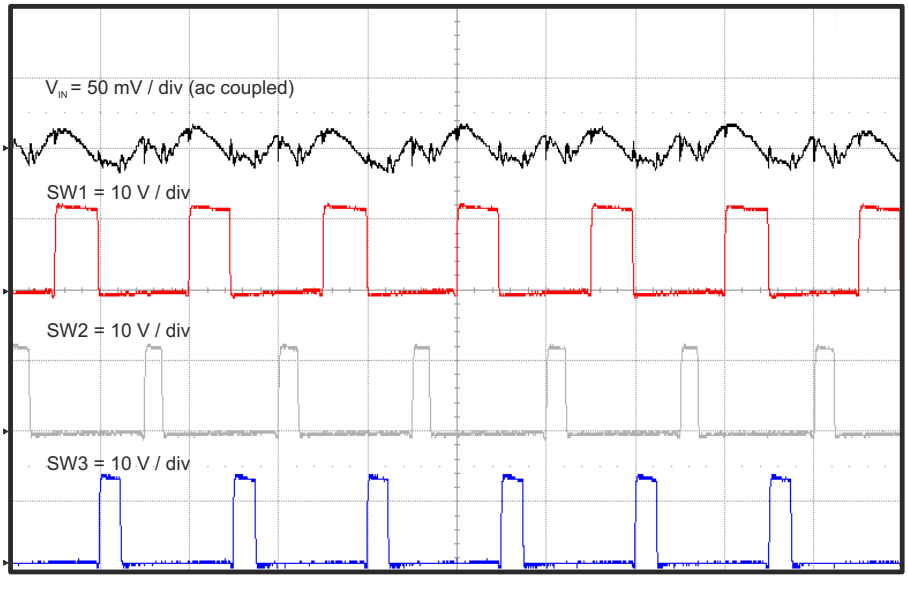

Figure 4-10. TPS65581EVM-575 Input Voltage Ripple

4.8 Start-Up

The TPS65581EVM-575 start-up waveform for CH1 relative to V_{IN} is shown in Figure 4-11. Load = 4 Ω resistive. The start up waveforms for CH2 and CH3 are similar and not shown.

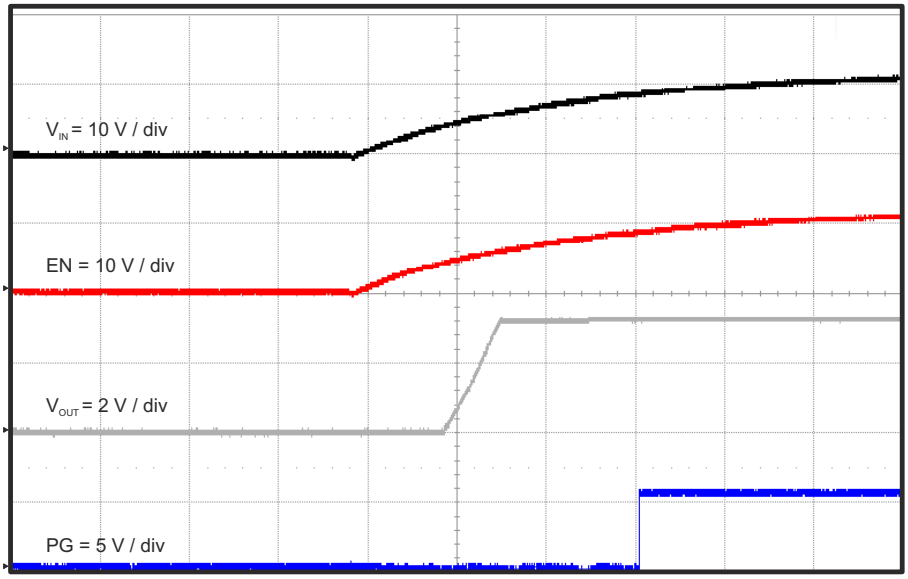

Figure 4-11. TPS65581EVM-575 CH1 Start-Up Relative to V_{IN}

The TPS65581EVM-575 start-up waveform for CH1 relative to enable (EN) is shown in Figure 4-12. Load = 4 Ω resistive. The start up waveforms for CH2 and CH3 are similar and not shown.

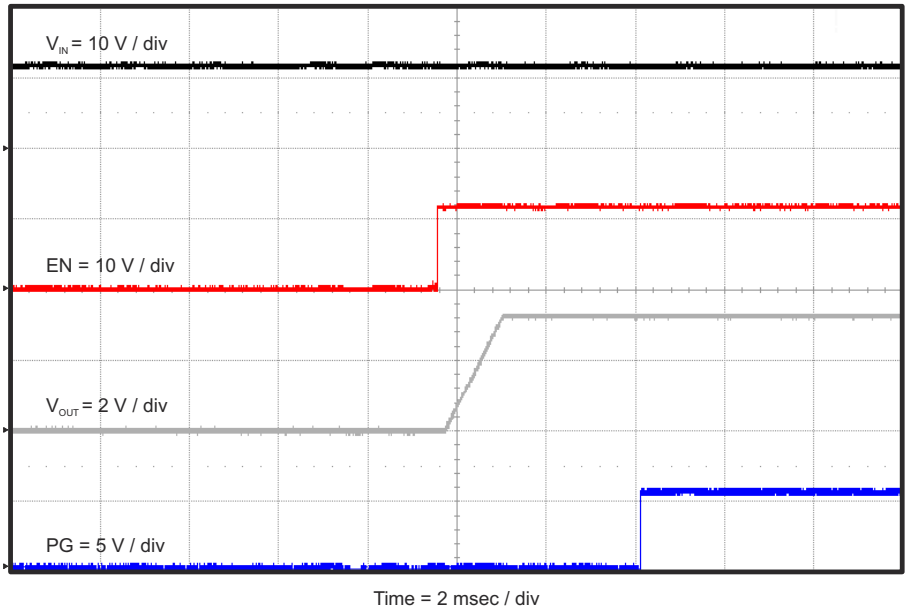

Figure 4-12. TPS65581EVM-575 CH1 Start-Up Relative to EN

5 Board Layout

This section provides a description of the TPS65581EVM-575, board layout, and layer illustrations.

5.1 Layout

The board layout for the TPS65581EVM-575 is shown in Figure 5-1 through Figure 5-5.

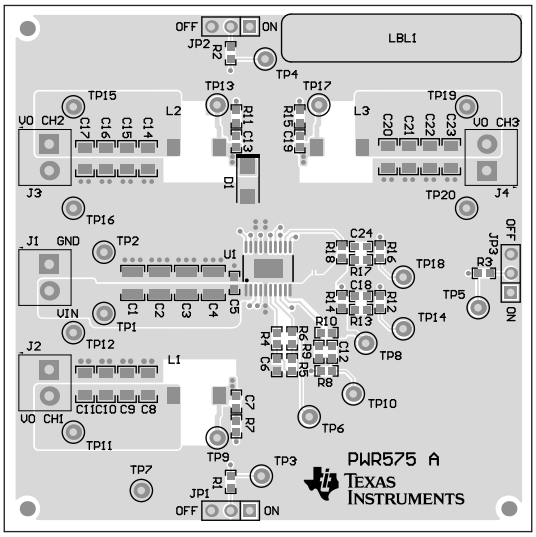

Figure 5-1. Top Assembly

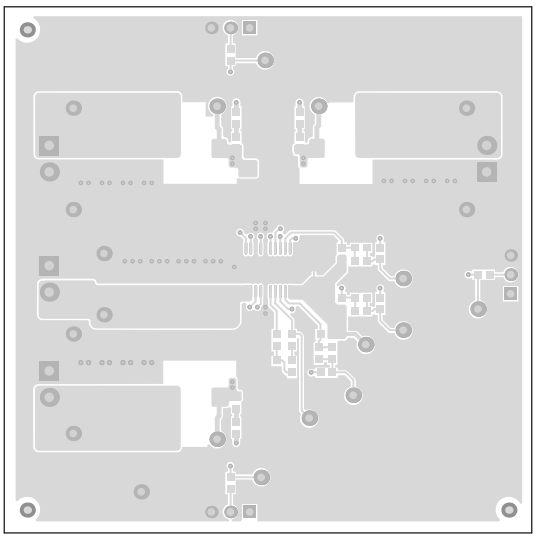

Figure 5-2. Top Layer

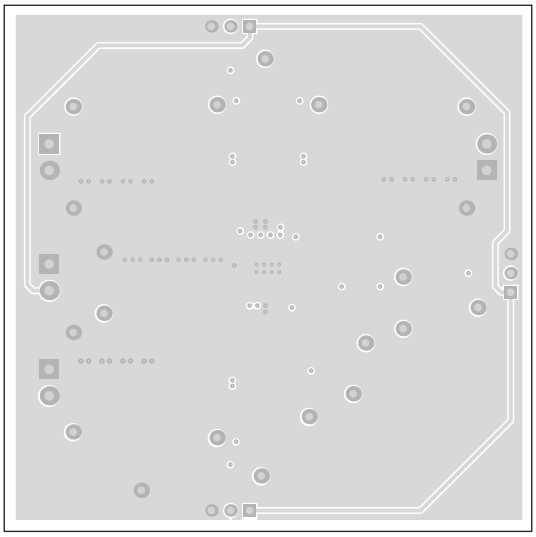

Figure 5-3. Internal Layer 1

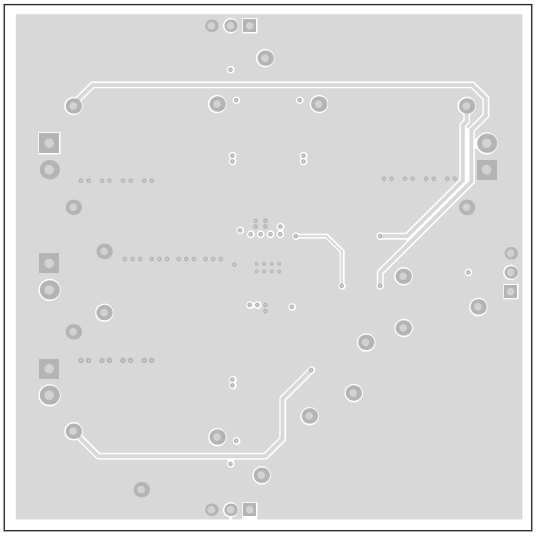

Figure 5-4. Internal Layer 2

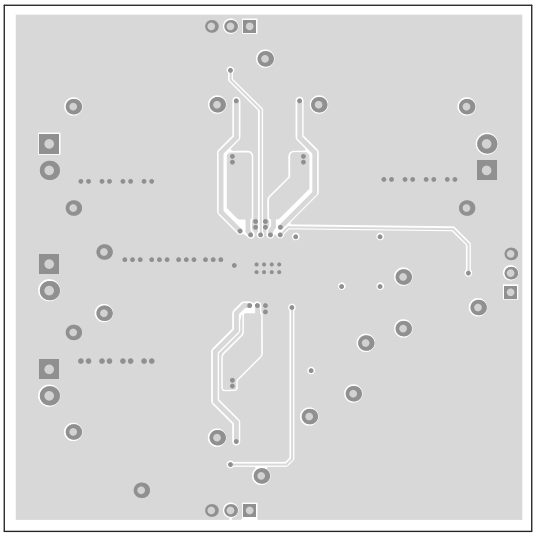

Figure 5-5. Bottom Layer

6 Schematic, Bill of Materials, and Reference

6.1 Schematic

Figure 6-1 is the schematic for the TPS65581EVM-575.

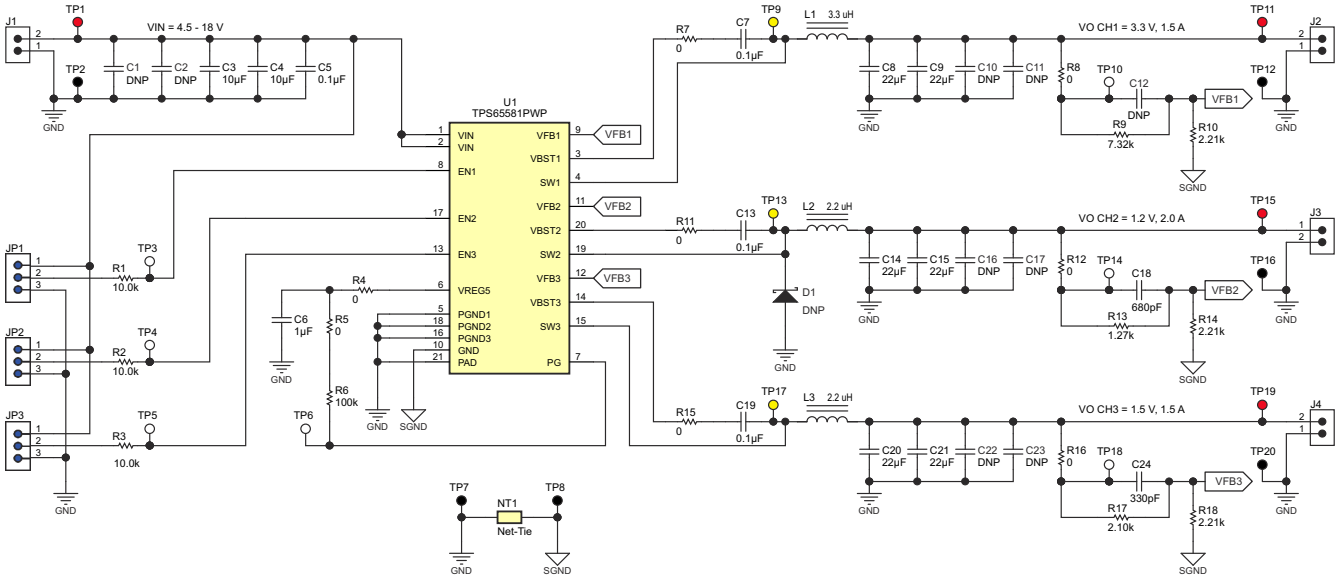

Figure 6-1. TPS65581EVM-575 Schematic Diagram

6.2 Bill of Materials

Table 6-1. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
PCB1	1		Printed Circuit Board		PWR575	Any
C3, C4	2	10 µF	CAP, CERM, 10uF, 25V, +/-10%, X5R, 1210	1210	GRM32DR61E106KA12L	MuRata
C5, C7, C13, C19	4	0.1 µF	CAP, CERM, 0.1uF, 25V, +/-10%, X5R, 0603	0603	GRM188R61E104KA01D	MuRata
C6	1	1 µF	CAP, CERM, 1uF, 10V, +/-10%, X5R, 0603	0603	GRM185R61A105KE36D	MuRata
C8, C9, C14, C15, C20, C21	6	22 µF	CAP, CERM, 22uF, 10V, +/-10%, X5R, 1206	1206	GRM31CR61A226KE19L	MuRata
C18	1	680 pF	CAP, CERM, 680pF, 50V, +/-10%, X7R, 0603	0603	GRM188R71H681KA01D	MuRata
C24	1	330 pF	CAP, CERM, 330pF, 50V, +/-10%, X7R, 0603	0603	GRM188R71H331KA01D	MuRata
J1, J2, J3, J4	4		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	7.0x8.2x6.5mm	ED555/2DS	On-Shore Technology, Inc.
JP1, JP2, JP3	3	1x3	Header, TH, 100mil, 1x3, Gold plated, 230 mil above insulator	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions
L1	1	3.3 µH	Inductor, Power Line, Magnetic Shielded, ±30%	6.9x7.2 mm	CLF7045T-3R3N	TDK
L2, L3	2	2.2 µH	Inductor, Power Line, Magnetic Shielded, ±30%	6.9x7.2 mm	CLF7045T-2R2N	TDK
R1, R2, R3	3	10.0k	RES, 10.0k ohm, 1%, 0.1W, 0603	0603	CRCW060310K0FKEA	Vishay-Dale
R4, R5, R7, R8, R11, R12, R15, R16	8	0	RES, 0 ohm, 5%, 0.1W, 0603	0603	CRCW06030000Z0EA	Vishay-Dale
R6	1	100k	RES, 100k ohm, 1%, 0.1W, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
R9	1	7.32k	RES, 7.32k ohm, 1%, 0.1W, 0603	0603	CRCW06037K32FKEA	Vishay-Dale
R10, R14, R18	3	2.21k	RES, 2.21k ohm, 1%, 0.1W, 0603	0603	CRCW06032K21FKEA	Vishay-Dale
R13	1	1.27k	RES, 1.27k ohm, 1%, 0.1W, 0603	0603	CRCW06031K27FKEA	Vishay-Dale
R17	1	2.10k	RES, 2.10k ohm, 1%, 0.1W, 0603	0603	CRCW06032K10FKEA	Vishay-Dale
SH-JP1, SH-JP2, SH-JP3	3	1x2	Shunt, 100mil, Gold plated, Black	Shunt	969102-0000-DA	3M
TP1, TP11, TP15, TP19	4	Red	Test Point, Miniature, Red, TH	Red Miniature Testpoint	5000	Keystone
TP2, TP7, TP8, TP12, TP16, TP20	6	Black	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone
TP3, TP4, TP5, TP6, TP10, TP14, TP18	7	White	Test Point, Miniature, White, TH	White Miniature Testpoint	5002	Keystone
TP9, TP13, TP17	3	Yellow	Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone
U1	1		4.5V to 18V Input 1.5A/2A/1.5A Triple Synchronous Step-Down SWIFT Converter, PWP0020B	PWP0020B	TPS65581PWP	Texas Instruments
C1, C2	0	10uF	CAP, CERM, 10uF, 25V, +/-10%, X5R, 1210	1210	GRM32DR61E106KA12L	MuRata
C10, C11, C16, C17, C22, C23	0	22uF	CAP, CERM, 22uF, 10V, +/-10%, X5R, 1206	1206	GRM31CR61A226KE19L	MuRata
C12	0		CAP, CERM,		Used in BOM report	Used in BOM report
D1	0	30V	Diode, Schottky, 30V, 3A, SMA	SMA	B330A-13-F	Diodes Inc.

6.3 Reference

TPS65581: *4.5V to 18V Input 1.5A, 2.5A, 1.5A Triple Synchronous Step-Down Converter* data sheet (SLVSC38)

7 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (October 2013) to Revision A (May 2021)	Page
• Updated user's guide title	2
• Updated the numbering format for tables, figures, and cross-references throughout the document	2

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