UCD90240EVM-704 24-Rail Sequencer Development Board

The UCD90240 is a 24-rail PMBus power sequencer and system manager. This UCD90240EVM-704 user's guide describes features, typical applications, electrical specifications, and an overview of the EVM board. Also included are test setup and procedures, software setup, printed-circuit board layouts, a bill of materials (BOM), and the EVM schematics.

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1 Introduction

This user's guide describes the UCD90240 Sequencer Development Board (UCD90240EVM-704). The UCD90240 is a 24-rail PMBus power sequencer and system manager. The UCD90240 can sequence, monitor and margin 24 voltage rails, monitor and respond to user-defined faults such as OV, UV, OC, UC, temperature, time-out, and GPI-triggered faults; provide flexible configurations such as sequence-on/off dependencies, delay time, and Boolean logic; store fault logs into nonvolatile memory; and integrate value-added features such as watchdog, system reset, cascading and sync clock.

2 Description

The UCD90240EVM-704 contains a UCD90240 sequencer device and a step-down power stage using the TPS54678 synchronous step-down switcher with integrated FET (SWIFT™). Access to all of the I/O pins is provided via strip connectors for integration into complex systems using clip-type jumper wires. The UCD90240EVM provides a PMBus (power management bus) communication port. Microsoft® Windows® based host computers can monitor, control and configure the UCD90240 device using a USB interface adapter EVM (HPA172) and TI fusion digital power designer graphical user interface (GUI). The power stage using the TPS54678 synchronous step-down switcher (5-V input, 1.2-V output) is provided to assist evaluation of the UCD90240's margining function.

2.1 Typical Applications

- Industrial / ATE
- Telecom / Networking equipment
- Servers and storage systems
- Any system requiring sequencing and monitoring of multiple power rails

2.2 Features

- Powered by single 5-V supply
- Status LEDs on all digital I/O pins
- Strip connector I/O access
- Headers with pullup/pulldown configurability
- PMBus interface for configuration and monitoring

3 Electrical Performance Specifications

Table 1. UCD90240EVM-704 Electrical Performance Specifications

Parameter	Test Conditions	MIN	TYP	MAX	UNIT
Input Power					
Input voltage range		4.5	5	5.5	V
Input current	All LEDs on, no external load current on I/O pins or step-down converter		135		mA
Step-Down Converter					
Output voltage	Normal operation, not in margin mode		1.2		V
Output current				6	A
Analog Input					
Analog input voltage range	Use internal reference	0	–	3.3	V
Analog input voltage range	Use external reference	0	–	3	V
Digital Inputs and Outputs					
I/O high-level input voltage(1)		2.15	–	5.5	V
I/O low-level input voltage		0	–	1.15	V
I/O input hysteresis		0.2	–	–	V
I/O high-level output voltage	Load current (source) = –4 mA	2.4	–	–	V
I/O low-level output voltage	Load current (sink) = 4 mA	–	–	0.4	V

(1) Maximum input voltage for PMBUS_CNTRL, PMBALERT#, MARGIN19 and MARGIN20 pins are V33D +0.3 V

4 Board Overview

Figure 1 illustrates the UCD90240EVM-704 board.

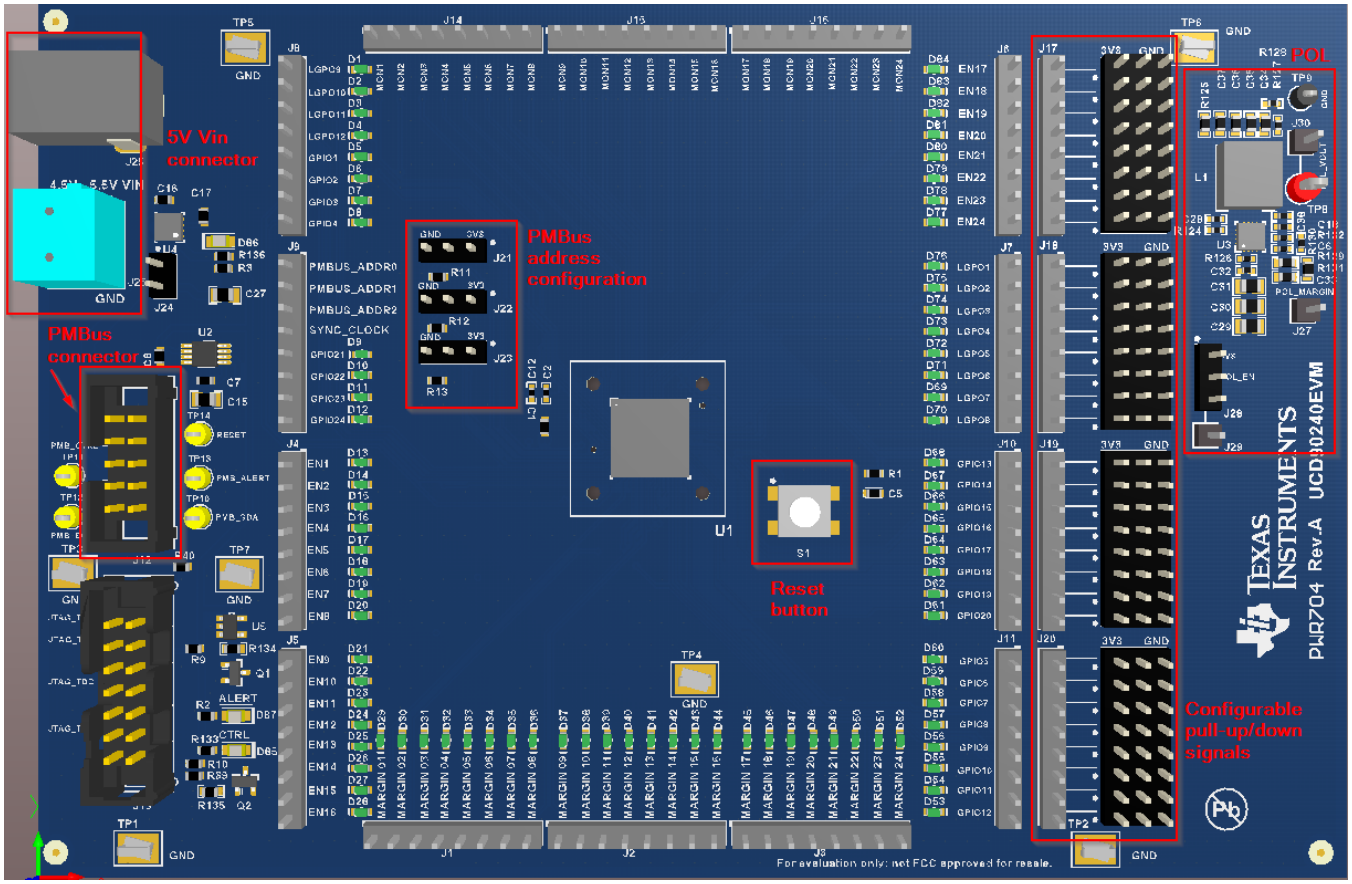


Figure 1. UCD90240EVM-704 Board Overview

5 Test Setup

5.1 Test Equipment

Voltage Source: One 5-volt power supply with at least 0.5-A sourcing capability. (Optional) One DC power supply with adjustable voltage from 0 V to 3.3 V.

Multimeters: One voltmeter

Output Load: Optional

Oscilloscope: Optional

Fan: None

Recommended Wire Gauge:AWG 24, or thicker

To Test Configuration, Monitoring and Control Functionality

Recommended PC platform: Windows 7, 64-bit with 8-GB RAM

USB Interface Adapter EVM (USB-to-GPIO): HPA172

The latest version Fusion Digital Power Designer software can be downloaded at the following link to the Texas Instruments website:
http://focus.ti.com/docs/toolsw/folders/print/fusion_digital_power_designer.html

5.2 Recommended Test Setup

Figure 2 illustrates the recommended test setup.

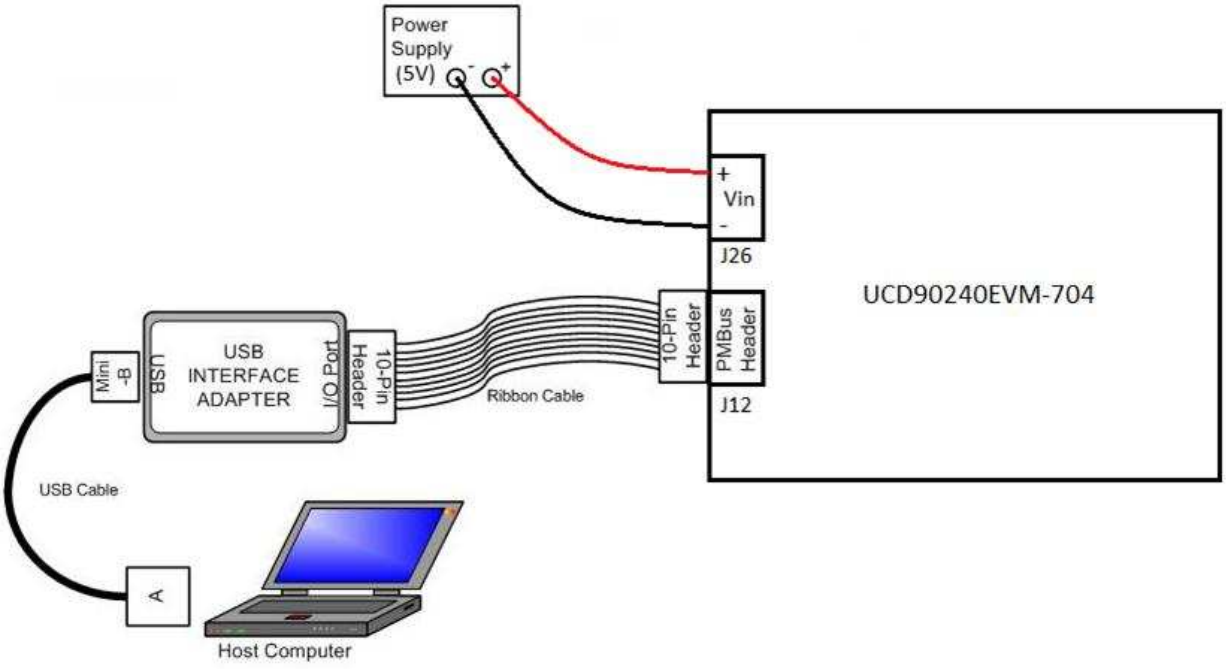


Figure 2. UCD90240EVM-704 Recommended Test Setup

5.3 List of Connectors and Functions

Table 2 lists the EVM connectors and functions.

Table 2. Connector Definition

Connectors	Pins	Name	Description
J1	1	MARGIN1	Margin PWM output
	2	MARGIN2	Margin PWM output
	3	MARGIN3	Margin PWM output
	4	MARGIN4	Margin PWM output
	5	MARGIN5	Margin PWM output
	6	MARGIN6	Margin PWM output
	7	MARGIN7	Margin PWM output
	8	MARGIN8	Margin PWM output
J2	1	MARGIN9	Margin PWM output
	2	MARGIN10	Margin PWM output
	3	MARGIN11	Margin PWM output
	4	MARGIN12	Margin PWM output
	5	MARGIN13	Margin PWM output
	6	MARGIN14	Margin PWM output
	7	MARGIN15	Margin PWM output
	8	MARGIN16	Margin PWM output
J3	1	MARGIN17	Margin PWM output
	2	MARGIN18	Margin PWM output
	3	MARGIN19	Margin PWM output
	4	MARGIN20	Margin PWM output
	5	MARGIN21	Margin PWM output
	6	MARGIN22	Margin PWM output
	7	MARGIN23	Margin PWM output
	8	MARGIN24	Margin PWM output
J4	1	EN1	Rail enable output
	2	EN2	Rail enable output
	3	EN3	Rail enable output
	4	EN4	Rail enable output
	5	EN5	Rail enable output
	6	EN6	Rail enable output
	7	EN7	Rail enable output
	8	EN8	Rail enable output
J5	1	EN9	Rail enable output
	2	EN10	Rail enable output
	3	EN11	Rail enable output
	4	EN12	Rail enable output
	5	EN13	Rail enable output
	6	EN14	Rail enable output
	7	EN15	Rail enable output
	8	EN16	Rail enable output

Table 2. Connector Definition (continued)

Connectors	Pins	Name	Description
J6	1	EN17	Rail enable output
	2	EN18	Rail enable output
	3	EN19	Rail enable output
	4	EN20	Rail enable output
	5	EN21	Rail enable output
	6	EN22	Rail enable output
	7	EN23	Rail enable output
	8	EN24	Rail enable output
J7	1	LGPO1	Logic GPO output
	2	LGPO2	Logic GPO output
	3	LGPO3	Logic GPO output
	4	LGPO4	Logic GPO output
	5	LGPO5	Logic GPO output
	6	LGPO6	Logic GPO output
	7	LGPO7	Logic GPO output
	8	LGPO8	Logic GPO output
J8	1	LGPO9	Logic GPO output
	2	LGPO10	Logic GPO output
	3	LGPO11	Logic GPO output
	4	LGPO12	Logic GPO output
	5	GPIO1	General Purpose I/O
	6	GPIO2	General Purpose I/O
	7	GPIO3	General Purpose I/O
	8	GPIO4	General Purpose I/O
J9	1	PMBUS_ADDR0	PMBus address pin
	2	PMBUS_ADDR1	PMBus address pin
	3	PMBUS_ADDR2	PMBus address pin
	4	SYNC_CLOCK	Sync Clock pin
	5	GPIO21	General Purpose I/O
	6	GPIO22	General Purpose I/O
	7	GPIO23	General Purpose I/O
	8	GPIO24	General Purpose I/O
J10	1	GPIO13	General Purpose I/O
	2	GPIO14	General Purpose I/O
	3	GPIO15	General Purpose I/O
	4	GPIO16	General Purpose I/O
	5	GPIO17	General Purpose I/O
	6	GPIO18	General Purpose I/O
	7	GPIO19	General Purpose I/O
	8	GPIO20	General Purpose I/O

Table 2. Connector Definition (continued)

Connectors	Pins	Name	Description
J11	1	GPIO5	General Purpose I/O
	2	GPIO6	General Purpose I/O
	3	GPIO7	General Purpose I/O
	4	GPIO8	General Purpose I/O
	5	GPIO9	General Purpose I/O
	6	GPIO10	General Purpose I/O
	7	GPIO11	General Purpose I/O
	8	GPIO12	General Purpose I/O
J12	1		No connection
	2		No connection
	3		No connection
	4		No connection
	5	+3V3_USB	3.3-V power provided by USB Interface Adapter EVM
	6	GND	PMBus GND
	7	PMB_CTRL	PMBus CONTROL line
	8	PMB_ALERT	PMBus ALERT# line
	9	PMB_SCL	PMBus Clock
	10	PMB_SDA	PMBus Data
J13	1	JTAG_TMS	JTAG TMS
	2		JTAG nTRST (unused)
	3	JTAG_TDI	JTAG TDI
	4		JTAG TDIS (unused)
	5		JTAG VTRef (unused)
	6		JTAG KEY
	7	JTAG_TDO	JTAG TDO
	8	GND	JTAG GND
	9		JTAG RTCK (unused)
	10	GND	JTAG GND
	11	JTAG_TCK	JTAG TCK
	12	GND	JTAG GND
	13		JTAG EMU0 (unused)
	14		JTAG EMU1 (unused)
J14	1	MON1	Analog monitor input
	2	MON2	Analog monitor input
	3	MON3	Analog monitor input
	4	MON4	Analog monitor input
	5	MON5	Analog monitor input
	6	MON6	Analog monitor input
	7	MON7	Analog monitor input
	8	MON8	Analog monitor input

Table 2. Connector Definition (continued)

Connectors	Pins	Name	Description
J15	1	MON9	Analog monitor input
	2	MON10	Analog monitor input
	3	MON11	Analog monitor input
	4	MON12	Analog monitor input
	5	MON13	Analog monitor input
	6	MON14	Analog monitor input
	7	MON15	Analog monitor input
	8	MON16	Analog monitor input
J16	1	MON17	Analog monitor input
	2	MON18	Analog monitor input
	3	MON19	Analog monitor input
	4	MON20	Analog monitor input
	5	MON21	Analog monitor input
	6	MON22	Analog monitor input
	7	MON23	Analog monitor input
	8	MON24	Analog monitor input
J17	1		Pullup/pulldown signal (can be used as GPI input)
	2		Pullup/pulldown signal (can be used as GPI input)
	3		Pullup/pulldown signal (can be used as GPI input)
	4		Pullup/pulldown signal (can be used as GPI input)
	5		Pullup/pulldown signal (can be used as GPI input)
	6		Pullup/pulldown signal (can be used as GPI input)
	7		Pullup/pulldown signal (can be used as GPI input)
	8		Pullup/pulldown signal (can be used as GPI input)
J18	1		Pullup/pulldown signal (can be used as GPI input)
	2		Pullup/pulldown signal (can be used as GPI input)
	3		Pullup/pulldown signal (can be used as GPI input)
	4		Pullup/pulldown signal (can be used as GPI input)
	5		Pullup/pulldown signal (can be used as GPI input)
	6		Pullup/pulldown signal (can be used as GPI input)
	7		Pullup/pulldown signal (can be used as GPI input)
	8		Pullup/pulldown signal (can be used as GPI input)
J19	1		Pullup/pulldown signal (can be used as GPI input)
	2		Pullup/pulldown signal (can be used as GPI input)
	3		Pullup/pulldown signal (can be used as GPI input)
	4		Pullup/pulldown signal (can be used as GPI input)
	5		Pullup/pulldown signal (can be used as GPI input)
	6		Pullup/pulldown signal (can be used as GPI input)
	7		Pullup/pulldown signal (can be used as GPI input)
	8		Pullup/pulldown signal (can be used as GPI input)

Table 2. Connector Definition (continued)

Connectors	Pins	Name	Description
J20	1		Pullup/pulldown signal (can be used as GPI input)
	2		Pullup/pulldown signal (can be used as GPI input)
	3		Pullup/pulldown signal (can be used as GPI input)
	4		Pullup/pulldown signal (can be used as GPI input)
	5		Pullup/pulldown signal (can be used as GPI input)
	6		Pullup/pulldown signal (can be used as GPI input)
	7		Pullup/pulldown signal (can be used as GPI input)
	8		Pullup/pulldown signal (can be used as GPI input)
J21	1	VDD	VDD (connect to Pin2 to pullup)
	2		Floating pin connected to PMBUS_ADDR0 through 1-kΩ resistor
	3	GND	GND (connect to Pin2 to pulldown)
J22	1	VDD	VDD (connect to Pin2 to pullup)
	2		Floating pin connected to PMBUS_ADDR1 through 1-kΩ resistor
	3	GND	GND (connect to Pin2 to pulldown)
J23	1	VDD	VDD (connect to Pin2 to pullup)
	2		Floating pin connected to PMBUS_ADDR2 through 1-kΩ resistor
	3	GND	GND (connect to Pin2 to pulldown)
J24	1	+3V3_USB	3.3-V power provided by USB Interface Adapter EVM
	2	+3V3	3.3V rail to power VDD
J25	1	5V_VIN	5-V input power positive terminal
	2	GND	5-V input power negative terminal
J26	1	5V_VIN	5-V input power positive terminal
	2	GND	5-V input power negative terminal
J27	1	POL_Margin	Connect this pin to a MARGIN pin to test margining function.
J28	1	+3V3	+3V3 rail (connect to Pin2 to pullup)
	2	POL_EN	POL enable
	3		Input from J29 (connect to Pin2 to control POL enable)
J29	1		Connect this pin to an EN pin to test enable function.
J30	1	POL_VOUT	Connect this pin to a MON pin to test margining function.
J31	1	+3V3	Connect to Pin2 to pullup
	2	DIO_01	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J32	1	+3V3	Connect to Pin2 to pullup
	2	DIO_02	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J33	1	+3V3	Connect to Pin2 to pullup
	2	DIO_03	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J34	1	+3V3	Connect to Pin2 to pullup
	2	DIO_04	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J35	1	+3V3	Connect to Pin2 to pullup
	2	DIO_05	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown

Table 2. Connector Definition (continued)

Connectors	Pins	Name	Description
J36	1	+3V3	Connect to Pin2 to pullup
	2	DIO_06	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J37	1	+3V3	Connect to Pin2 to pullup
	2	DIO_07	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J38	1	+3V3	Connect to Pin2 to pullup
	2	DIO_08	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J39	1	+3V3	Connect to Pin2 to pullup
	2	DIO_09	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J40	1	+3V3	Connect to Pin2 to pullup
	2	DIO_10	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J41	1	+3V3	Connect to Pin2 to pullup
	2	DIO_11	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J42	1	+3V3	Connect to Pin2 to pullup
	2	DIO_12	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J43	1	+3V3	Connect to Pin2 to pullup
	2	DIO_13	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J44	1	+3V3	Connect to Pin2 to pullup
	2	DIO_14	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J45	1	+3V3	Connect to Pin2 to pullup
	2	DIO_15	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J46	1	+3V3	Connect to Pin2 to pullup
	2	DIO_16	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J47	1	+3V3	Connect to Pin2 to pullup
	2	DIO_17	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J48	1	+3V3	Connect to Pin2 to pullup
	2	DIO_18	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J49	1	+3V3	Connect to Pin2 to pullup
	2	DIO_19	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J50	1	+3V3	Connect to Pin2 to pullup
	2	DIO_20	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown

Table 2. Connector Definition (continued)

Connectors	Pins	Name	Description
J51	1	+3V3	Connect to Pin2 to pullup
	2	DIO_21	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J52	1	+3V3	Connect to Pin2 to pullup
	2	DIO_22	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J53	1	+3V3	Connect to Pin2 to pullup
	2	DIO_23	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J54	1	+3V3	Connect to Pin2 to pullup
	2	DIO_24	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J55	1	+3V3	Connect to Pin2 to pullup
	2	DIO_25	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J56	1	+3V3	Connect to Pin2 to pullup
	2	DIO_26	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J57	1	+3V3	Connect to Pin2 to pullup
	2	DIO_27	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J58	1	+3V3	Connect to Pin2 to pullup
	2	DIO_28	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J59	1	+3V3	Connect to Pin2 to pullup
	2	DIO_29	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J60	1	+3V3	Connect to Pin2 to pullup
	2	DIO_30	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J61	1	+3V3	Connect to Pin2 to pullup
	2	DIO_31	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown
J62	1	+3V3	Connect to Pin2 to pullup
	2	DIO_32	Floating pin to create a digital signal (high or low)
	3	GND	Connect to Pin2 to pulldown

5.4 Test Points

Table 3. Test Point Functions

Test Points	Name	Description
TP1	GND	Ground
TP2	GND	Ground
TP3	GND	Ground
TP4	GND	Ground
TP5	GND	Ground
TP6	GND	Ground
TP7	GND	Ground
TP8	POL_VOUT	POL output voltage
TP9	GND	Ground
TP10	PMB_SDA	PMBus Data
TP11	PMB_CTRL	PMBus CONTROL line
TP12	PMB_SCL	PMBus Clock
TP13	PMB_ALERT	PMBus ALERT# line
TP14	RESET	UCD90240 reset pin signal

6 Software Setup

Accessing the UCD90240EVM-704's configuration, control, and monitoring capabilities with the Fusion Digital Power Designer software tool requires a onetime software setup per host system.

6.1 Fusion Digital Power Designer Software (Fusion GUI) Installation

Place the Fusion Digital Power Designer Software (Fusion GUI) Installer executable file in a known location on the host computer to be used for EVM configuration/test.

Double click the *TI-Fusion-Digital-Power-Designer-2.0.xxx.exe* file and proceed through the installation by accepting the installer prompts and the license agreement. Use the Fusion GUI installer's suggested default installation locations to complete the install.

When the Fusion GUI installation reaches the finished window, uncheck the *Launch Application* check box and close the window.

7 Test Procedure

The *UCD90240EVM-704_Default_Configuration.xml* file is found in the SLVC613 zip file on the TI website and is provided to allow the user to return the EVM to its originally configured state.

Connect the EVM as shown in Figure 2: UCD90240 Recommended Test Setup. Apply the input voltage to the test setup. Open the Fusion Digital Power Designer GUI by navigating to the Start → Texas Instruments Fusion Digital Power Designer → Fusion Digital Power Designer (not the offline version which would have monitoring disabled). At the default Configuration Screen select the File → Import Project and the Project Open Wizard window will open. Open the default configuration file (UCD90240EVM-704_Default_Configuration.xml) and click Next. Follow the prompt to download the configuration file.

7.1 Voltage Monitoring Example

In the default configuration file, all MON pins are assigned to corresponding rails. Apply an external voltage within the specification in Table 1 to a MON pin. The voltage applied on the MON pin will be displayed in the Fusion GUI → Monitor page.

7.2 Rail Enable Example

In the default configuration file, all EN pins are assigned to corresponding rails, and all rails are controlled by CONTROL pin. The pin assignments are shown in Fusion GUI → Configure page→Pin Assignment tab. The CONTROL pin status can be controlled in Fusion GUI → Monitor page. Turn on the CONTROL Line in the Monitor page. Observe that all LEDs attached to EN pins are lit.

7.3 Fault Log Example (Including Blackbox Log)

Make sure the EN pin of a rail is asserted. Adjust the external voltage applied to the rail's MON pin such that the voltage is above Power Good On threshold and below OV Warn/Fault thresholds. In the Status page, click the Clear Faults button, Clear Logged Faults button, and Clear Blackbox Log button.

Adjust the external voltage applied to the MON pin such that the voltage is above OV fault threshold. In the Status page → Status Registers tab, observe that the Vout OV Fault of the corresponding rail is raised. In the Logged Faults tab, observe that the Vout OV Fault of the corresponding rail is also raised. In the Blackbox Info tab, click Refresh Blackbox Log button. Observe that the fault information and all the GPI/GPO/Rail statuses when the fault occurred were recorded in the Blackbox Log.

7.4 Command GPO Example

In the default configuration file, 12 GPIO pins are configured as command GPO. In the Configure page → Pin Assignment tab, change the Command GPO states and then click the Write to Hardware button. Observe the LED of the corresponding GPO pin changes state.

7.5 Configurable Pullup/Pulldown Signals

The UCD90240EVM-704 provides 32 configurable pullup/pulldown signals. The output pins of the pullup/pulldown signals are located in J17, J18, J19, and J20. Each pin is connected to 3.3 V or GND through a 680-Ω resistor. The state of each pin can be configured by a 3-pin header next to it. The pullup/pulldown signals can be used as GPI pin input signals and pull up for open-drain GPO pins.

7.6 GPI and Logic GPO Example

In the default configuration file, 12 GPIO pins are configured as GPI pin with GPI Fault feature enabled. Each of the 12 LGPO pins is configured to follow a corresponding GPI signal with a 960-ms time delay. The pin assignments are shown in the Configure page → Pin Assignment tab.

Connect a logic input signal to a GPI pin. Observe that the LED of the corresponding LGPO pin is lit after 960 ms. Also observe that the corresponding GPI Fault is logged in the Status page. Disconnect the logic input signal from the GPI pin. Observe that the LED of the corresponding LGPO pin is out after 960 ms.

7.7 Margin Example

In the default configuration file, all 24 rails are configured with the margining function. The pin assignments are shown in the Configure page→Pin Assignment tab. Connect the onboard POL output voltage (J30) to a rail's MON pin using a jumper wire. Then connect the rail's MARGIN pin to the onboard POL's margin input (J27) to close the margin loop. Connect the rail's EN pin to J29 which controls the onboard POL's enable signal. Connect J28's Pin 2 and Pin 3 using a shunt jumper. In the Fusion GUI → Monitor page, turn on the CONTROL line. Observe that the rail's EN pin LED is lit, and the onboard POL is enabled. The POL's output voltage is monitored in the Monitor page, which should be at 1.2 V.

In the Fusion GUI → Monitor page, click to change the margin status to Low. Observe that the POL output voltage is regulated at Margin Low level defined in the Configure page→ Vout Config tab. Click to change the margin status to High. Observe that the POL output voltage is regulated at Margin High level.

7.8 Cascading Example

7.8.1 Sync Clock

Sync Clock can synchronize multiple UCD90240 devices such that they respond to the same GPI event synchronously and the same GPI event has the same time stamp in all synchronized UCD90240 devices. The Sync Clock I/O pin is located in J9. Implementing the Sync Clock feature requires two or more UCD90240EVM-704 boards.

In the Fusion GUI → Configure page → Other Config tab, configure one EVM board as Sync Clock master, and all other boards as slaves. Connect the multiple EVM boards to the same ground. Connect all Sync Clock pins to the same node. Observe that the synchronized UCD90240 devices respond to the same GPI event synchronously.

When the Sync Clock pin is not used, configure the UCD90240 device as Sync Clock master.

7.8.2 Fault Pin

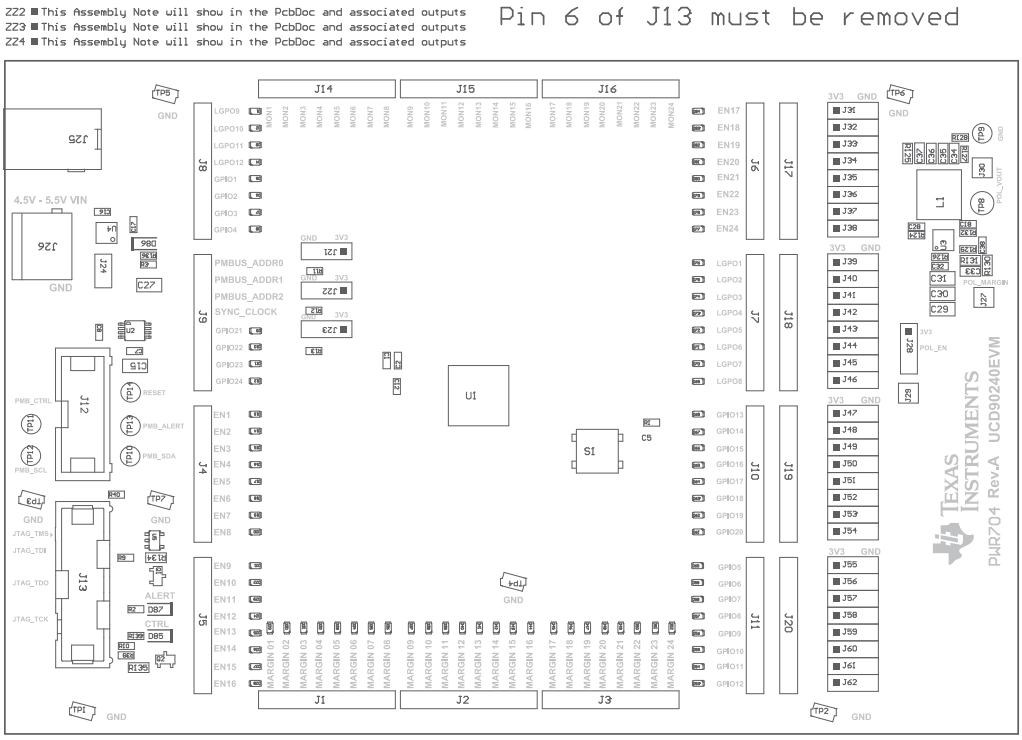
Multiple UCD90240 devices can be acknowledged on the same rail fault and react accordingly, even if the rail is monitored by only one UCD90240 device. This is achieved by the Fault Pin feature.

In each UCD90240 device, up to 4 GPI pins can be configured as Fault Pins. Each Fault Pin is connected to a Fault Bus. Each Fault Bus is pulled up to 3.3 V by a 10-kΩ resistor. When there is no fault on a Fault Bus, the Fault Pins are GPI pins and listen to the Fault Bus. When a rail fault is detected by a UCD90240 device, the corresponding Fault Pin is turned into active driven low state, pulling down the Fault Bus and informing all other UCD90240 devices of the corresponding fault. Refer to the UCD90240 datasheet for configuration and connection examples.

The Fault Pin feature and the Sync Clock feature can work together to achieve better synchronized fault-response performance.

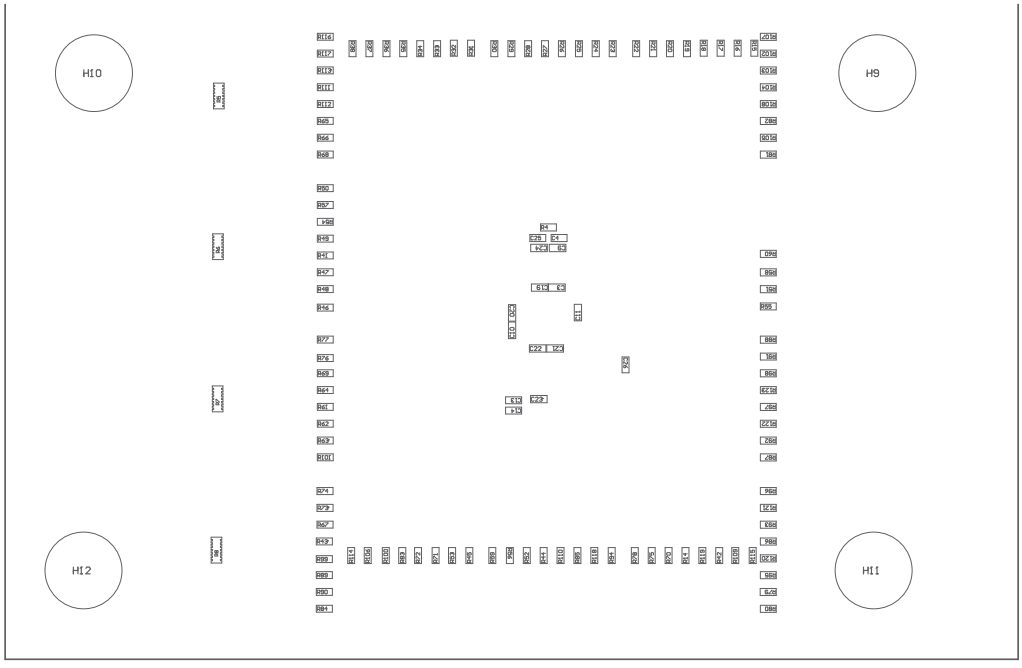
8 EVM Assembly Drawing and PCB Layout

Figure 3 and Figure 4 illustrate the EVM assembly drawings and PCB layouts.



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: 001

Figure 3. UCD90240EVM-704 Top Assembly Drawing



COMPONENTS MARKED 'DNP' SHOULD NOT BE POPULATED.
ASSEMBLY VARIANT: 001

Figure 4. UCD90240EVM-704 Bottom Assembly Drawing

Figure 5 illustrates the UCD90240EVM-704 fabrication drawing.

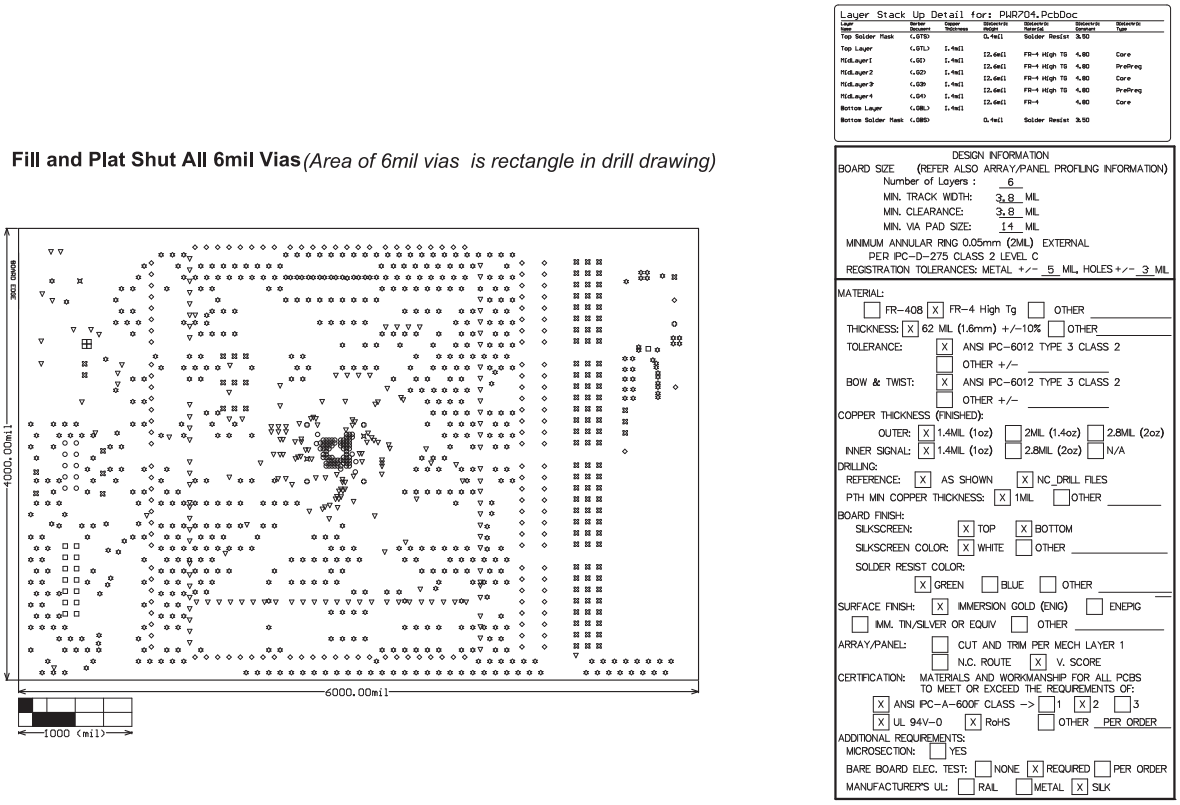


Figure 5. UCD90240EVM-704 Fabrication Drawing

Figure 6 through Figure 17 illustrate the UCD90240EVM-704 PCB drawings.

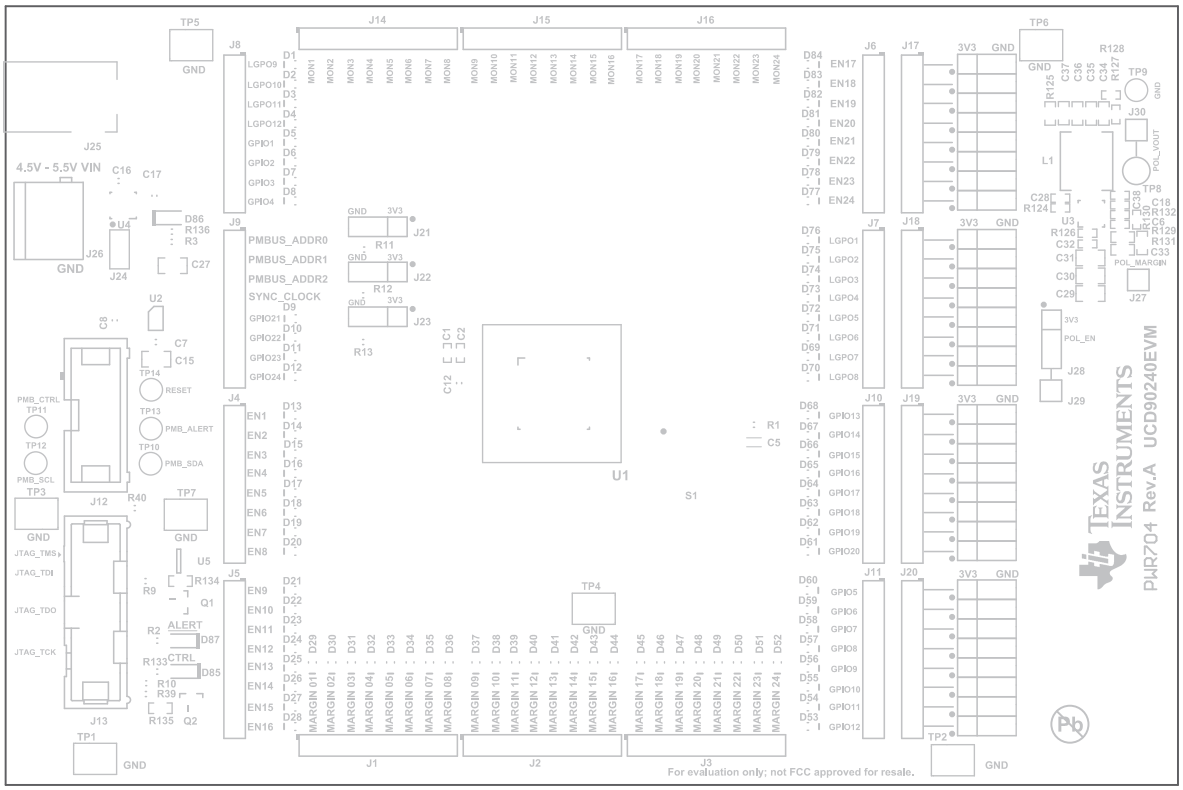


Figure 6. UCD90240EVM-704 Top Overlay

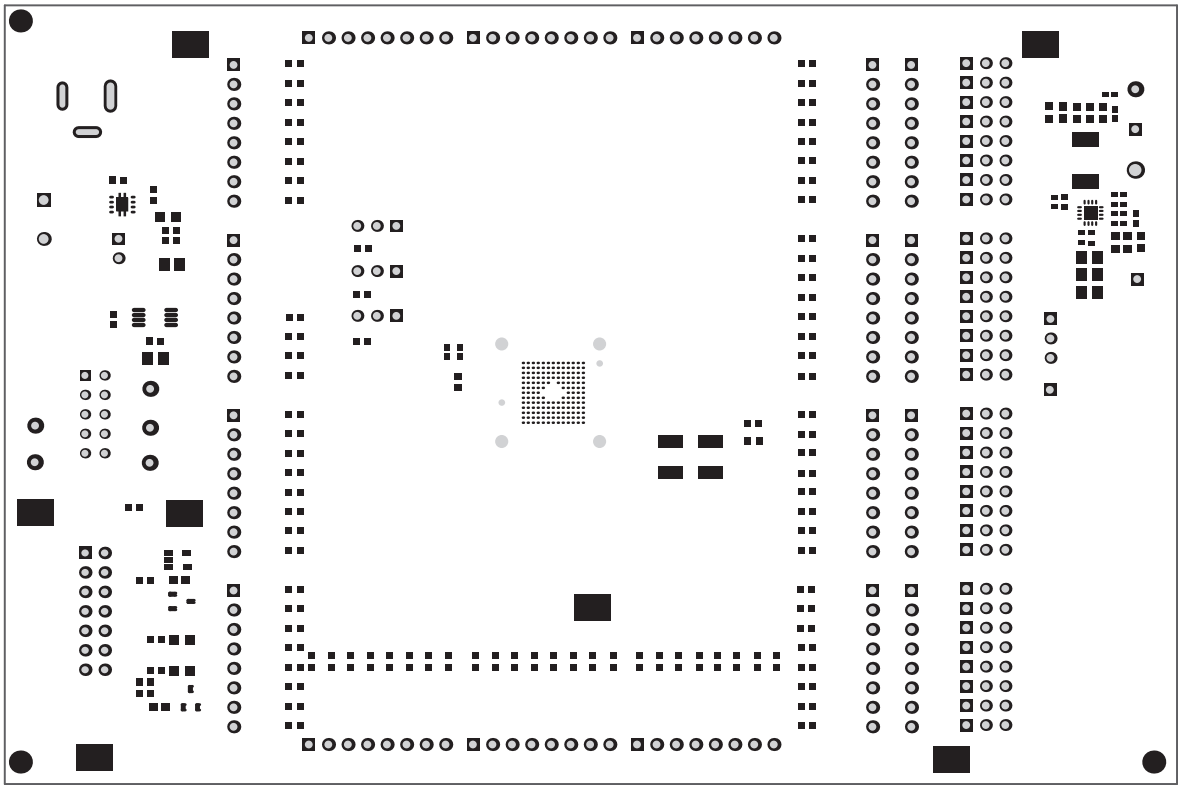


Figure 7. UCD90240EVM-704 Top Solder Mask

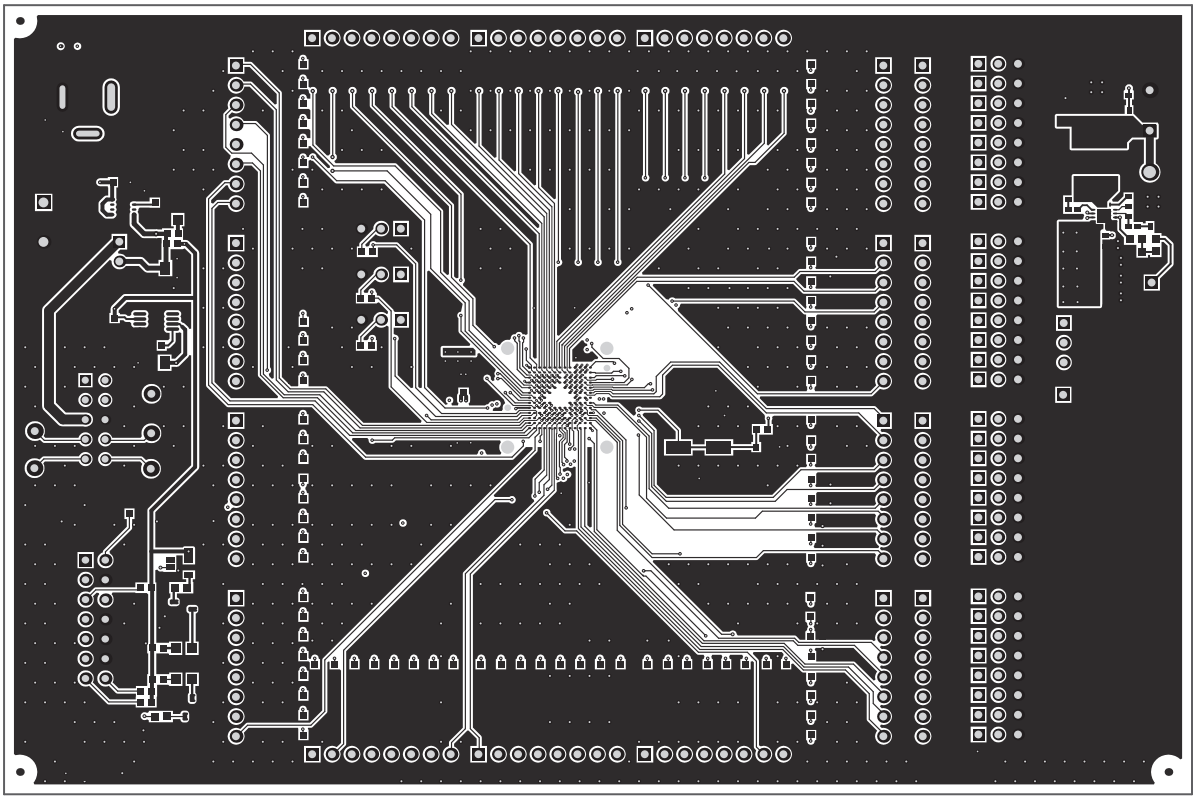


Figure 8. UCD90240EVM-704 Top Layer

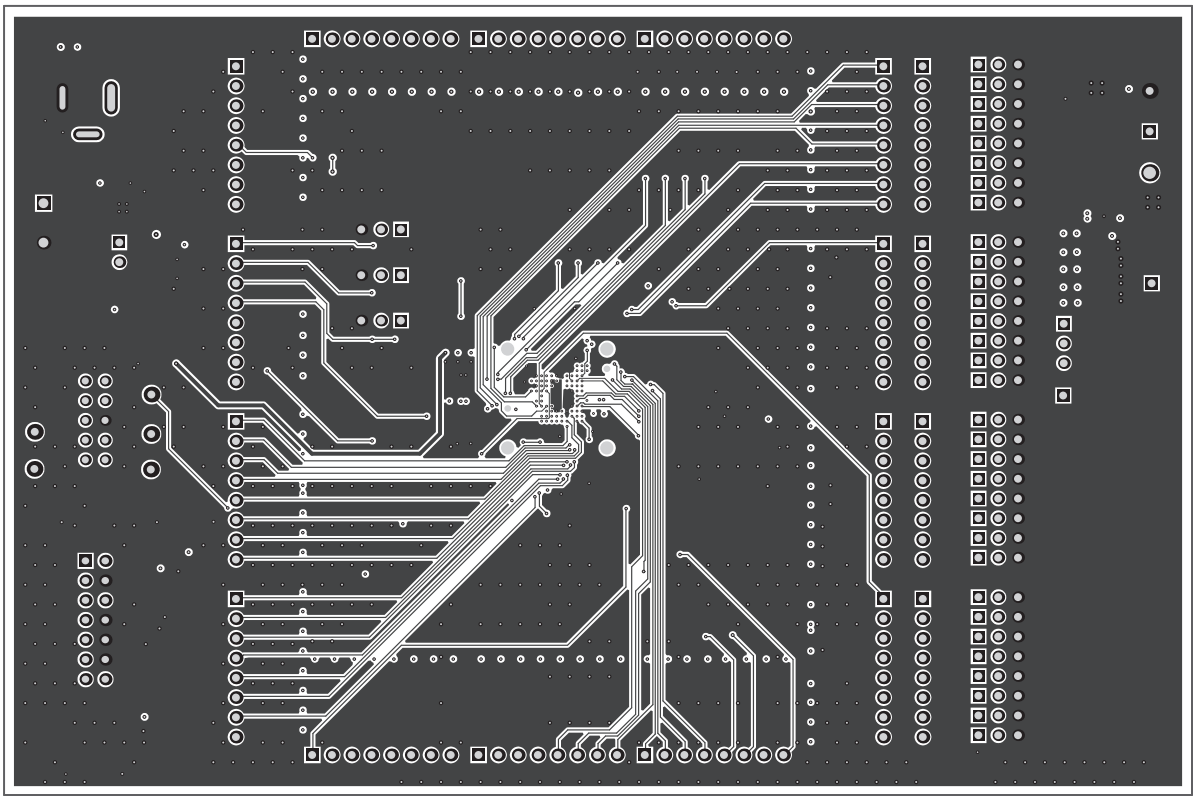


Figure 9. UCD90240EVM-704 Midlayer 1

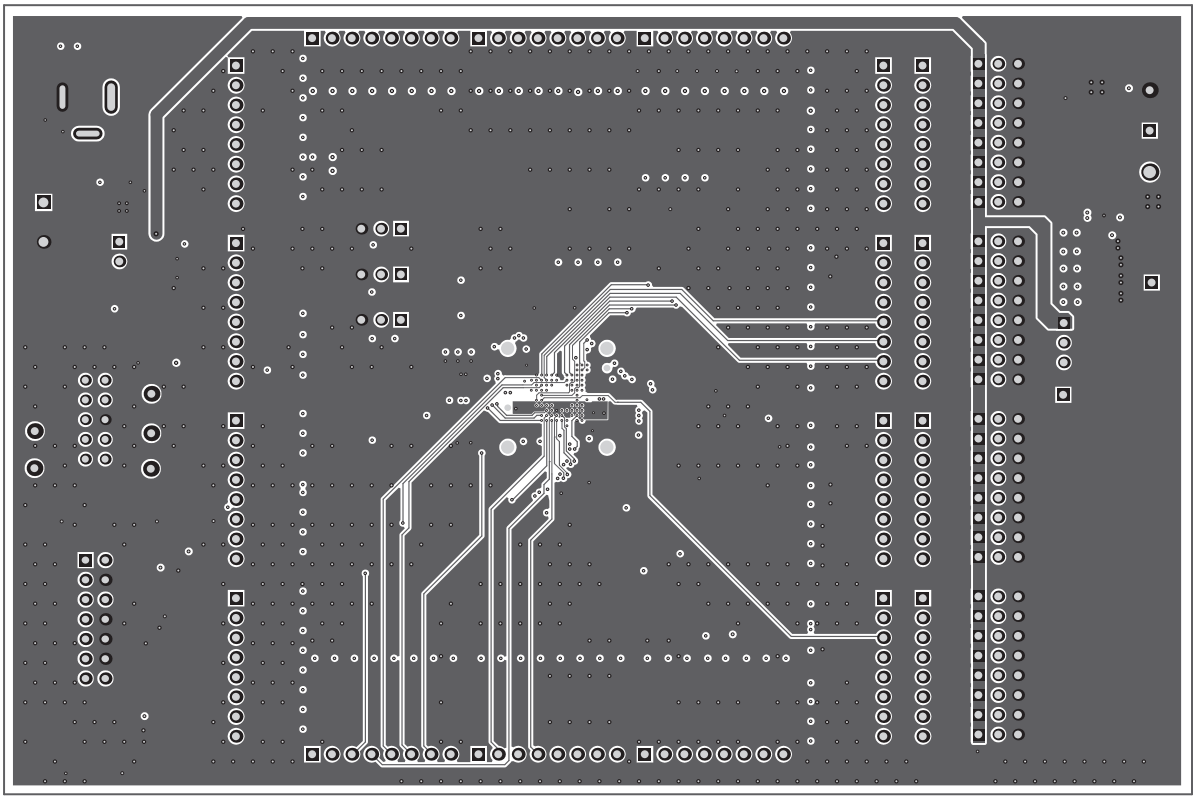


Figure 10. UCD90240EVM-704 Midlayer 2

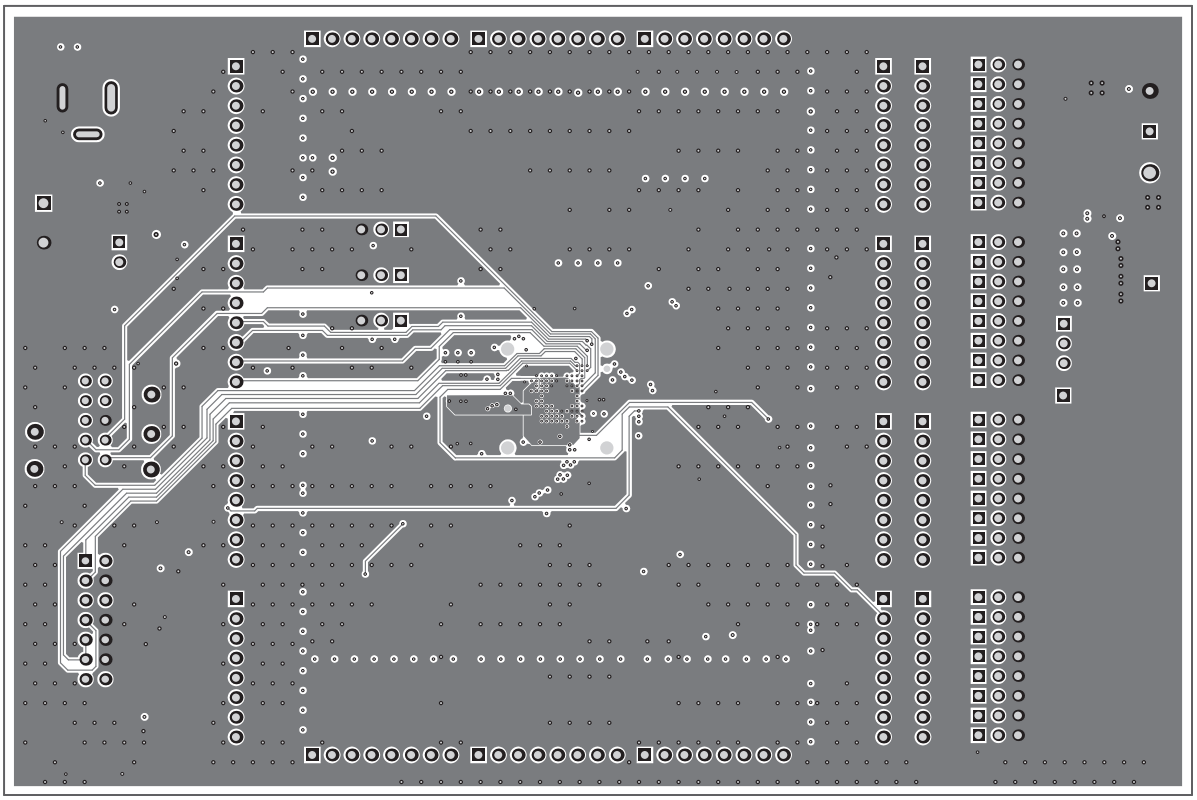


Figure 11. UCD90240EVM-704 Midlayer 3

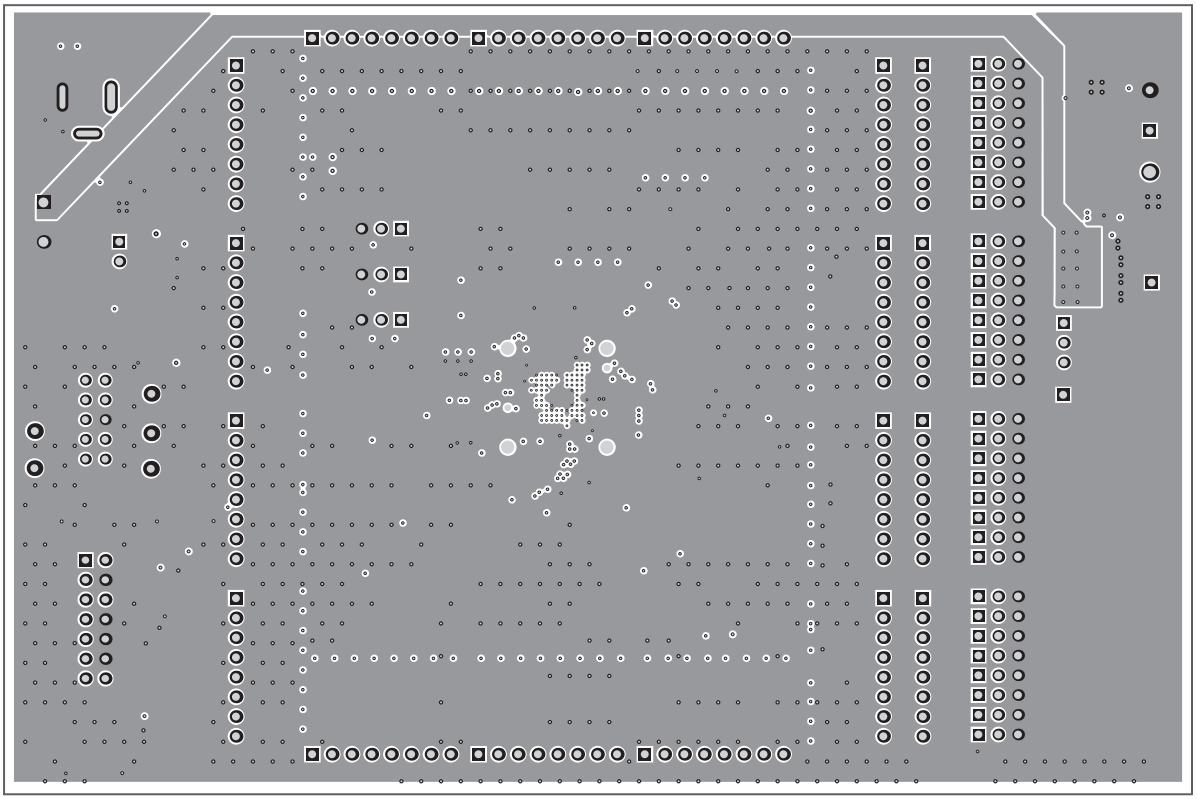


Figure 12. UCD90240EVM-704 Midlayer 4

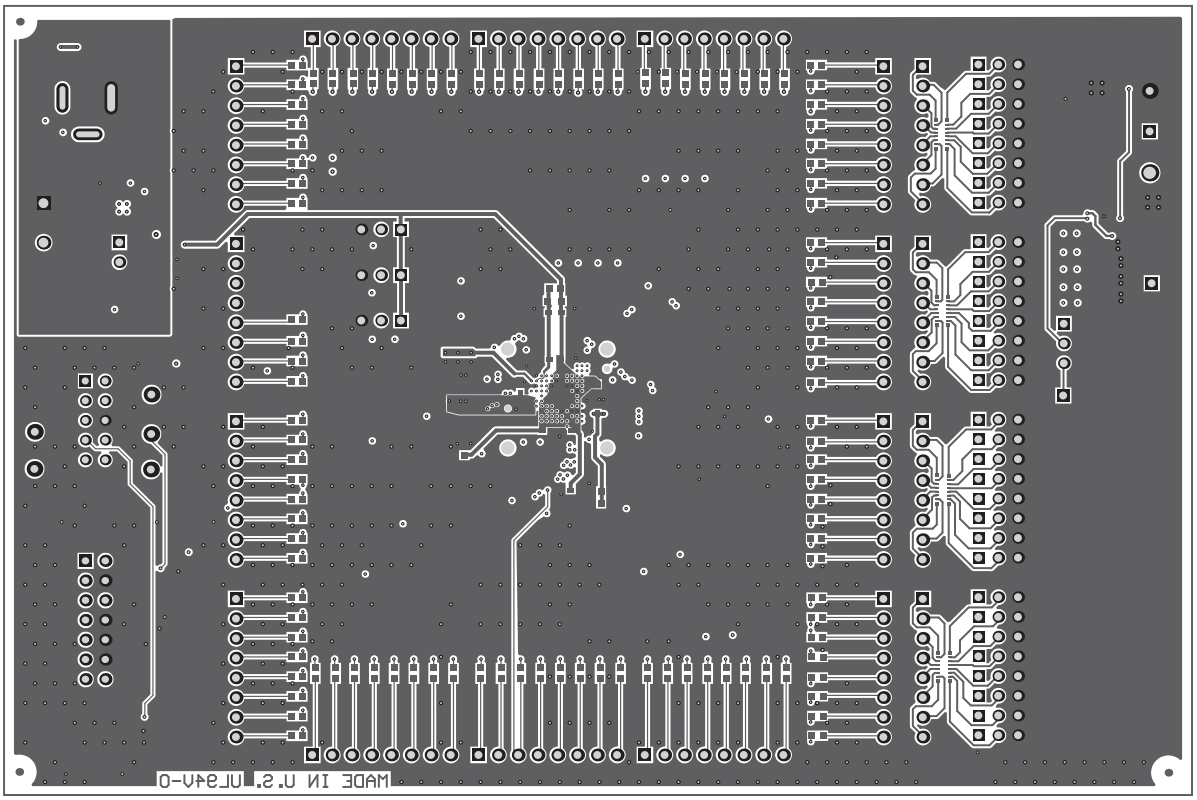


Figure 13. UCD90240EVM-704 Bottom Layer

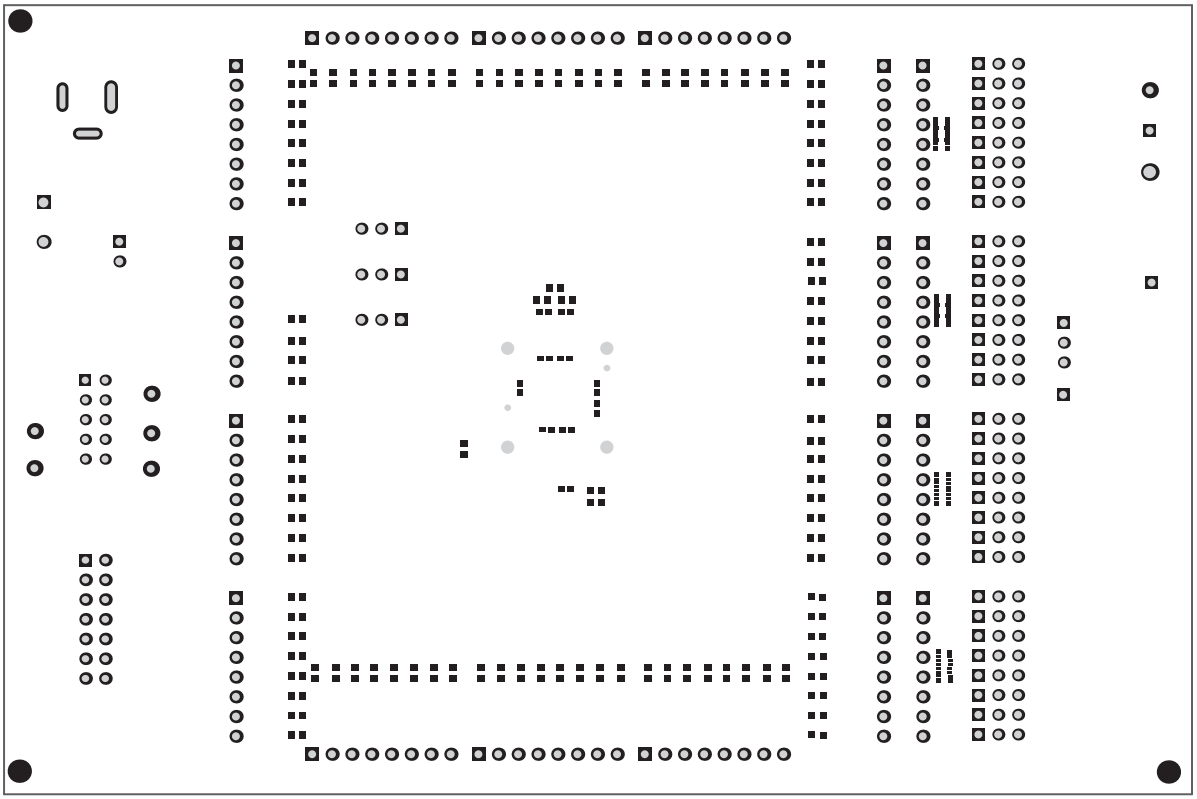


Figure 14. UCD90240EVM-704 Bottom Solder Mask

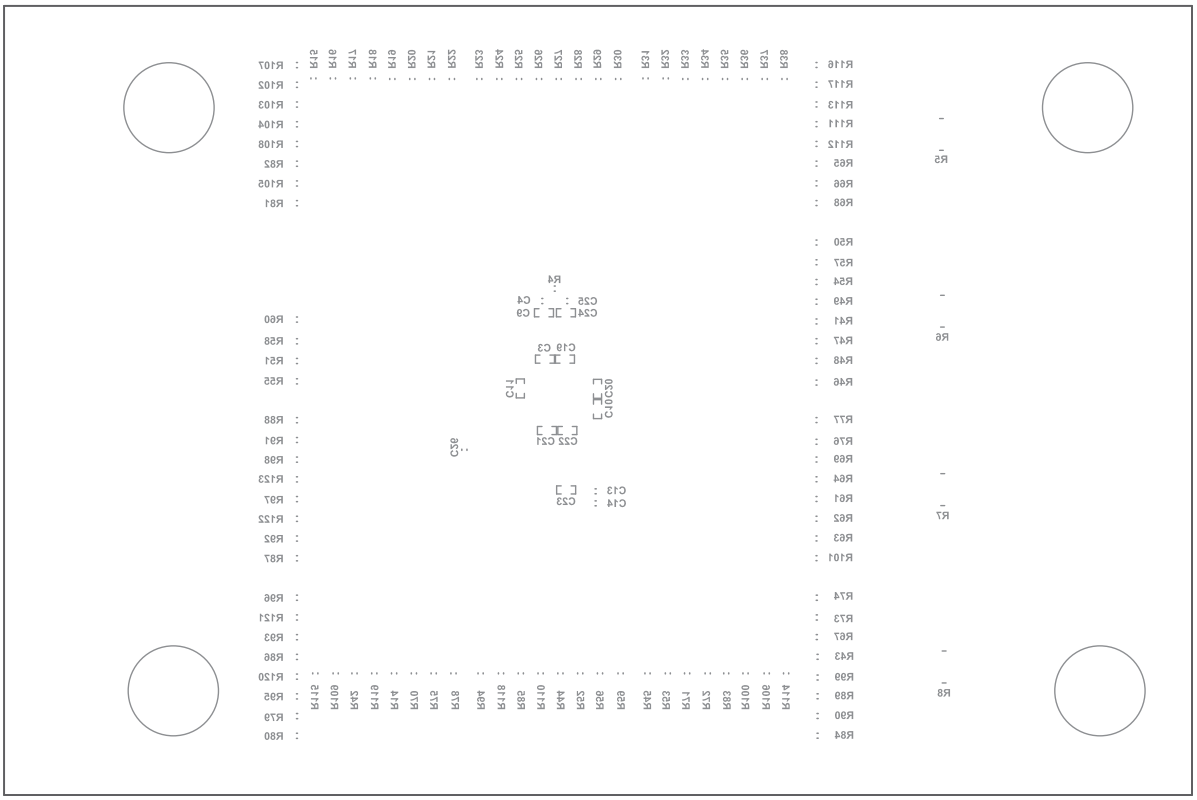


Figure 15. UCD90240EVM-704 Bottom Overlay

Fill and Plat Shut All 6mil Vias *(Area of 6mil vias is rectangle in drill drawing)*

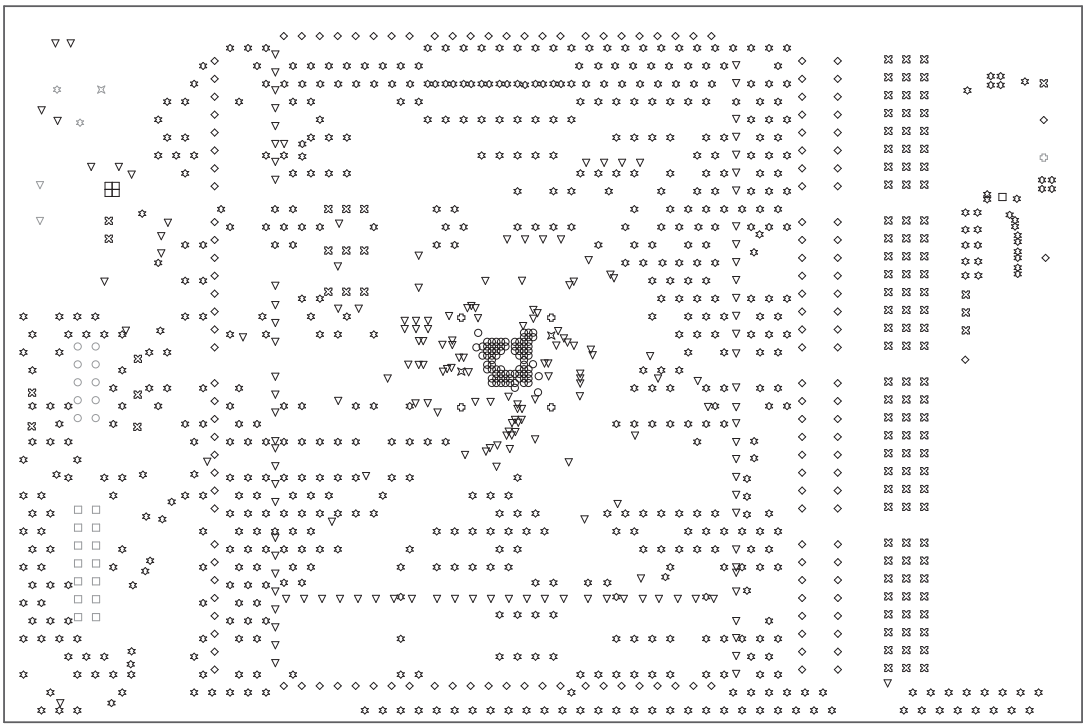


Figure 16. UCD90240EVM-704 Drill Drawing

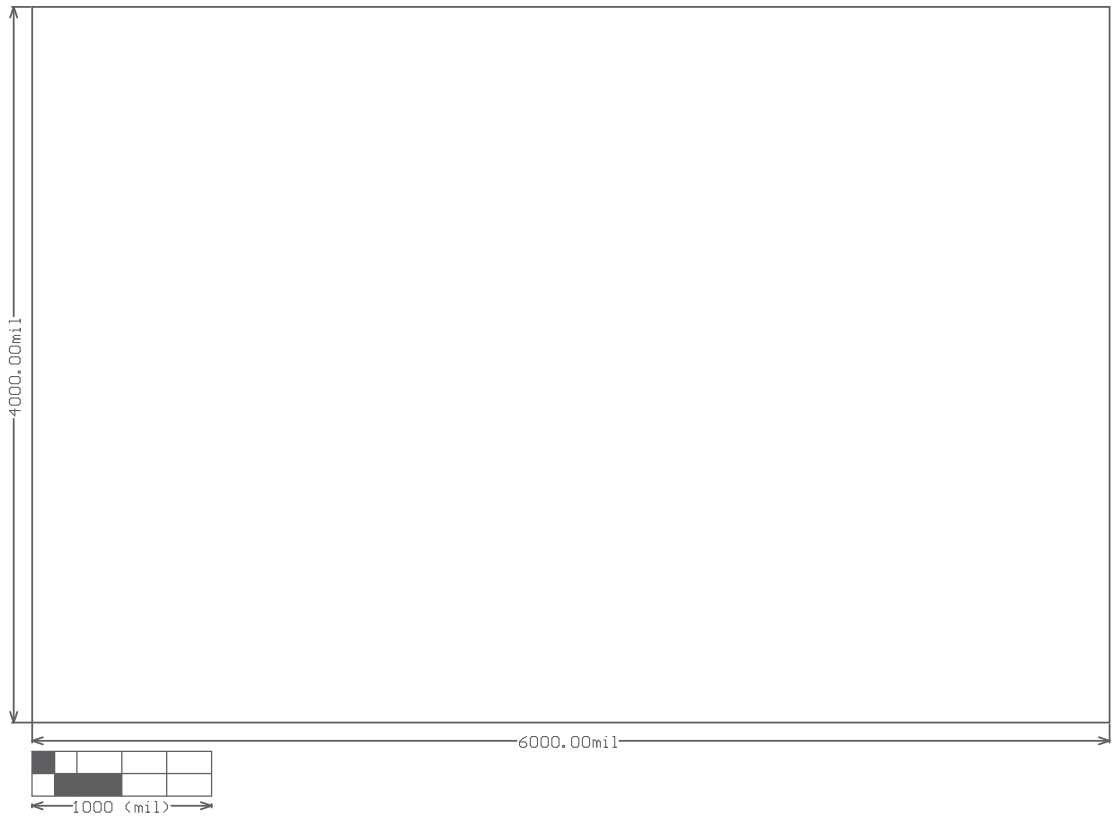


Figure 17. UCD90240EVM-704 Board Dimensions

9 Bill of Materials (BOM)

Table 4. UCD90240EVM-704 Bill of Materials

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
C1, C3, C18–C20	5	0.01uF	CAP, CERM, 0.01 µF, 16 V, ±10%, X7R, 0402	0402	C1005X7R1C103K	TDK		
C2, C9–C11, C21–C24	8	0.1uF	CAP, CERM, 0.1 µF, 6.3 V, ±10%, X5R, 0402	0402	C1005X5R0J104K	TDK		
C4, C7, C8, C12–C14, C16, C25, C26	9	1uF	CAP, CERM, 1 µF, 25 V, ±10%, X5R, 0603	0603	C1608X5R1E105K080AC	TDK		
C5	1	1000pF	CAP, CERM, 1000pF, 50V, ±5%, X7R, 0603	0603	C0603C102J5RACTU	Kemet	-	-
C15, C27	2	10uF	CAP, CERM, 10 µF, 6.3 V, ±10%, X6S, 0805	0805	GRM219C80J106KE39D	Murata		
C17	1	0.01uF	CAP, CERM, 0.01 µF, 50 V, ±5%, X7R, 0603	0603	C0603C103J5RACTU	Kemet		
C28, C32	2	0.1uF	CAP, CERM, 0.1 µF, 16 V, ±10%, X5R, 0402	0402	GRM155R61C104KA88D	Murata		
C29–C31	3	22uF	CAP, CERM, 22 µF, 6.3 V, ±20%, X5R, 0805	0805	GRM21BR60J226ME39L	Murata		
C33	1	1000pF	CAP, CERM, 1000 pF, 50 V, ±5%, X7R, 0603	0603	C0603C102J5RACTU	Kemet		
C34–C37	4	22uF	CAP, CERM, 22 µF, 6.3 V, ±20%, X5R, 0603	0603	C1608X5R0J226M080AC	TDK		
C38	1	2700pF	CAP, CERM, 2700 pF, 50 V, ±10%, X7R, 0402	0402	GRM155R71H272KA01D	Murata		
D1–D84	84	Green	LED, Green, SMD	1.7x0.65x0.8mm	LG L29K-G2J1-24-Z	OSRAM		
D85, D86	2	Green	LED, Green, SMD	LED_0805	LTST-C171GKT	Lite-On		
D87	1	Red	LED, Red, SMD	LED_0805	LTST-C170KRKT	Lite-On		
H9, H10, H11, H12	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M		
J1–J11, J14–J20	18		Header, 100mil, 8x1, Tin, TH	Header, 8x1, 100mil, TH	PEC08SAAN	Sullins Connector Solutions		
J12	1		Header (shrouded), 100mil, 5x2, Gold, TH	TH, 10-Leads, Body 8.5x20mm, Pitch 2.54mm	XG4C-1031	Omron Electronic Components		
J13	1		Header (shrouded), 100mil, 7x2, Gold, TH	7x2 Header	N2514-6002-RB	3M		
J21–J23, J28, J31–J62	36		Header, 100mil, 3x1, Tin, TH	Header, 3 PIN, 100mil, Tin	PEC03SAAN	Sullins Connector Solutions		
J24	1		Header, 100mil, 2x1, Tin, TH	Header, 2 PIN, 100mil, Tin	PEC02SAAN	Sullins Connector Solutions		
J25	1		Power Jack, mini, 2.5mm OD, R/A, TH	Jack, 14.5x11x9mm	RAPC712X	Switchcraft		
J26	1		TERMINAL BLOCK 5.08MM VERT 2POS, TH	TERM_BLK, 2pos, 5.08mm	ED120/2DS	On-Shore Technology		
J27, J29, J30	3		Header, 1x1, Tin, TH	Header, 1x1	PEC01SAAN	Sullins Connector Solutions		
L1	1	1uH	Inductor, Shielded, Ferrite, 1 µH, 12 A, 0.0072 Ω, SMD	Inductor, 7.2x4x6.5mm	SRP6540-1R0M	Bourns		
Q1, Q2	2	60V	MOSFET, N-CH, 60 V, 0.17 A, SOT-23	SOT-23	2N7002-7-F	Diodes Inc.		None
R1, R10, R39, R40	4	4.7k	RES, 4.7 k, 5%, 0.1 W, 0603	0603	CRCW06034K70JNEA	Vishay-Dale		
R2, R133, R136	3	330	RES, 330, 5%, 0.1 W, 0603	0603	CRCW0603330RJNEA	Vishay-Dale		
R3	1	0.1	RES, 0.1, 1%, 0.1 W, 0603	0603	ERJ-3RSFR10V	Panasonic		
R4	1	1.0	RES, 1.0, 5%, 0.1 W, 0603	0603	CRCW06031R00JNEA	Vishay-Dale		
R5–R8	4	680	RES, 680, 5%, 0.0625 W, Resistor Array - 8x1	Resistor Array - 8x1	EXB-2HV681JV	Panasonic		
R9	1	0	RES, 0, 5%, 0.1 W, 0603	0603	ERJ-3GEY0R00V	Panasonic		
R11–R13	3	1.0k	RES, 1.0 k, 5%, 0.1 W, 0603	0603	RC0603JR-071KL	Yageo America		

Table 4. UCD90240EVM-704 Bill of Materials (continued)

Designator	Qty	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
R14, R41–R123	84	1.65k	RES, 1.65 k, 1%, 0.1 W, 0603	0603	RC0603FR-071K65L	Yageo America		
R15–R38	24	200	RES, 200, 0.1%, 0.1 W, 0603	0603	RG1608P-201-B-T5	Susumu Co Ltd		
R124	1	0	RES, 0, 5%, 0.063 W, 0402	0402	CRCW04020000Z0ED	Vishay-Dale		
R125	1	40.2	RES, 40.2, 1%, 0.1 W, 0603	0603	RC0603FR-0740R2L	Yageo America		
R126, R129	2	10k	RES, 10 k, 5%, 0.063 W, 0402	0402	CRCW040210K0JNED	Vishay-Dale		
R127, R128	2	20.0k	RES, 20.0 k, 1%, 0.063 W, 0402	0402	CRCW040220K0FKED	Vishay-Dale		
R130	1	97.6k	RES, 97.6 k, 1%, 0.1 W, 0603	0603	RC0603FR-0797K6L	Yageo America		
R131	1	100k	RES, 100 k, 1%, 0.1 W, 0603	0603	CRCW0603100KFKEA	Vishay-Dale		
R132	1	82.5k	RES, 82.5 k, 1%, 0.063 W, 0402	0402	CRCW040282K5FKED	Vishay-Dale		
R134, R135	2	30.1k	RES, 30.1 k, 1%, 0.1 W, 0603	0603	RC0603FR-0730K1L	Yageo America		
S1	1		Switch, Tactile, SPST-NO, 1VA, 32V, SMT	Switch, 6.3x5.36x6.6 mm, SMT	KT11P2JM34LFS	C&K Components		
TP1–TP7	7	SMT	Test Point, Compact, SMT	Testpoint_Keystone_Compact	5016	Keystone		
TP8	1	Red	Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint	5010	Keystone		
TP9	1	Black	Test Point, Miniature, Black, TH	Black Miniature Testpoint	5001	Keystone		
TP10–TP14	5	Yellow	Test Point, Miniature, Yellow, TH	Yellow Miniature Testpoint	5004	Keystone		
U1	1		24-Rail PMBus Power Sequencer and Power Manager, ZRB0157A	ZRB0157A	UCD90240ZRBR	Texas Instruments	UCD90240ZRBT	Texas Instruments
U2	1		Low Noise, Very Low Drift, Precision Voltage Reference, -40°C to 125°C, 8-pin MSOP (DGK), Green (RoHS & no Sb/Br)	DGK0008A	REF5030AIDGKT	Texas Instruments	Equivalent	None
U3	1		2.95 V to 6 V Input, 6 A Output, 2 MHz, Synchronous Step DOWN Switcher With Integrated FET (SWIFT™), RTE0016F	RTE0016F	TPS54678RTER	Texas Instruments	TPS54678RTET	Texas Instruments
U4	1		Single Output Low Noise LDO, 400 mA, Fixed 3.3 V Output, 1.7 to 5.5 V Input, with Reverse Current Protection, 8-pin SON (DRB), -40°C to 85°C, Green (RoHS & no Sb/Br)	DRB0008A	TPS73633DRBR	Texas Instruments	Equivalent	None
U5	1		Single Inverter Gate, DBV0005A	DBV0005A	SN74LVC1G04DBVR	Texas Instruments	SN74LVC1G04DBVT	Texas Instruments
C6	0	DNP	CAP, CERM, 22 pF, 50 V, ±5%, C0G/NP0, 0402	0402	GRM1555C1H220JA01D	Murata		
FID1– FID6	0		Fiducial mark. There is nothing to buy or mount.	N/A	N/A	N/A		
	Quantity	**Value**	**Description**	**Package Reference**	**Part Number**	**Manufacturer**	**Alternate Part Number**	**Alternate Manufacturer**
	2.93780573	0.01uF	CAP, CERM, 0.01 µF, 16 V, ±10%, X7R, 0403	0402	C1005X7R1C103K	TDK		
	2.809618195	0.1uF	CAP, CERM, 0.1 µF, 6.3 V, ±10%, X5R, 0403	0402	C1005X5R0J104K	TDK		

NOTE: Unless otherwise noted in the Alternate Part Number and/or Alternate Manufacturer columns, all parts may be substituted with equivalents.

10 UCD90240EVM-704 Schematics

Figure 18 through Figure 23 illustrate the UCD90240EVM-704 schematics.

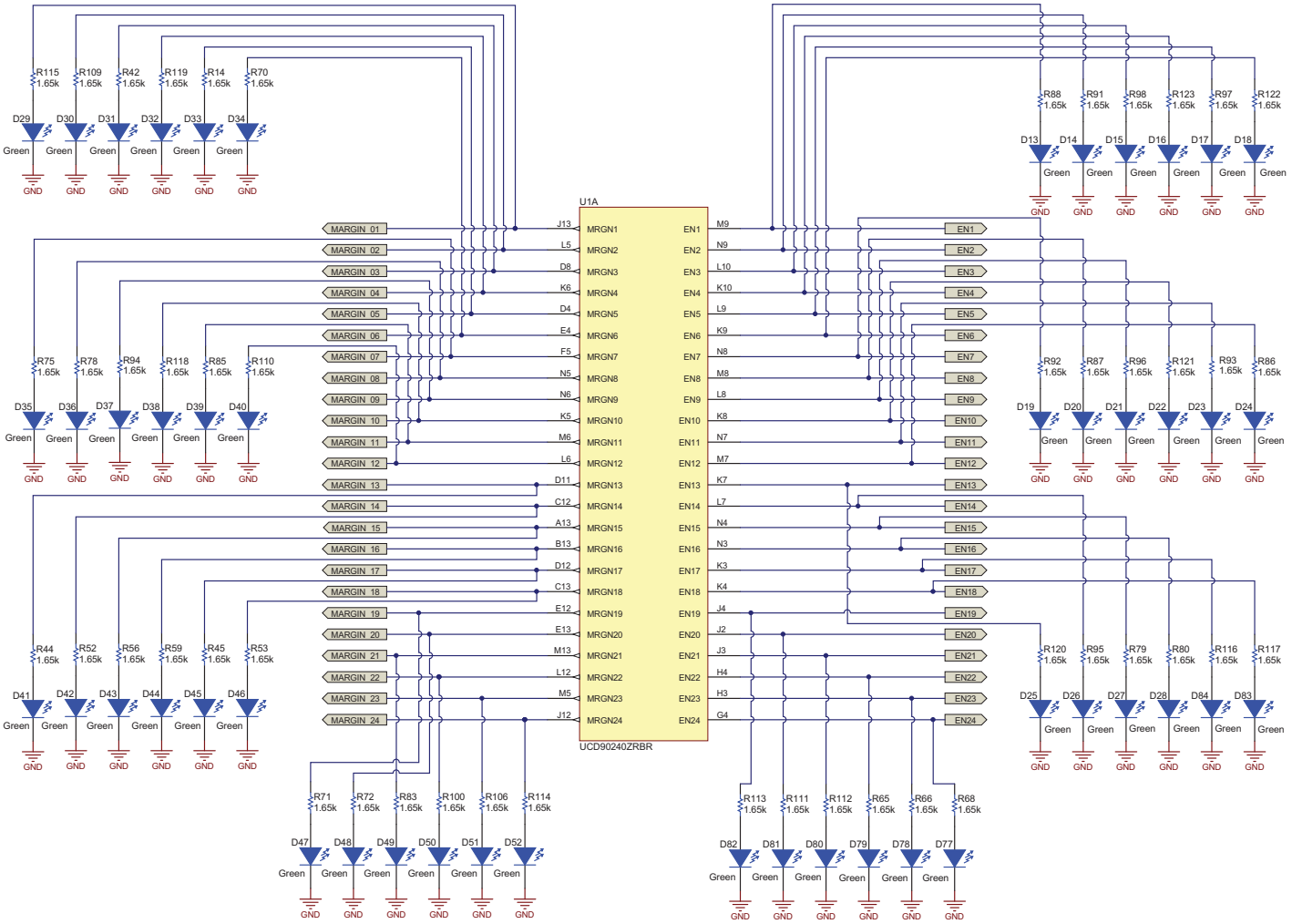


Figure 18. UCD90240EVM Schematic (1 of 6)

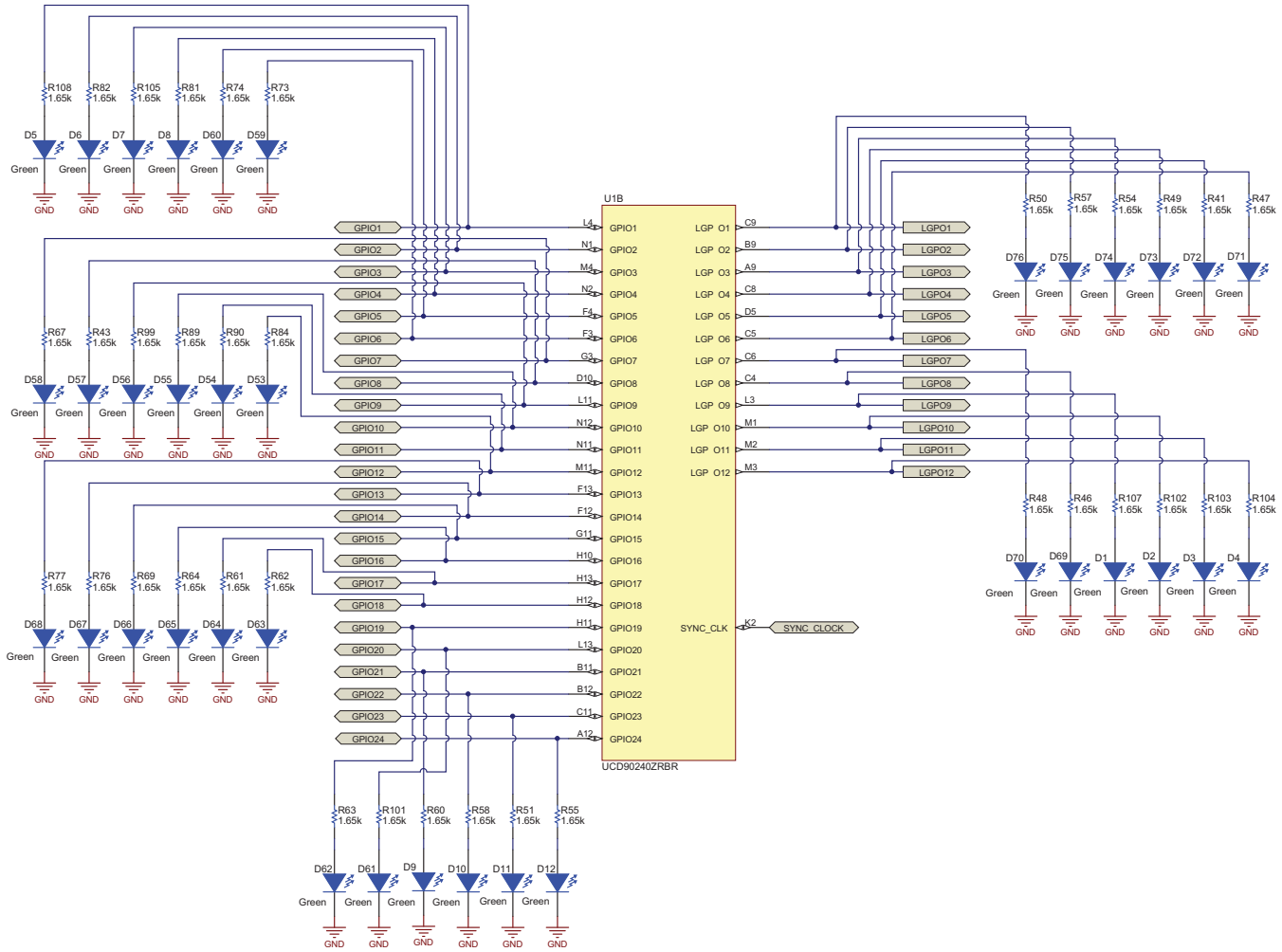


Figure 19. UCD90240EVM Schematic (2 of 6)

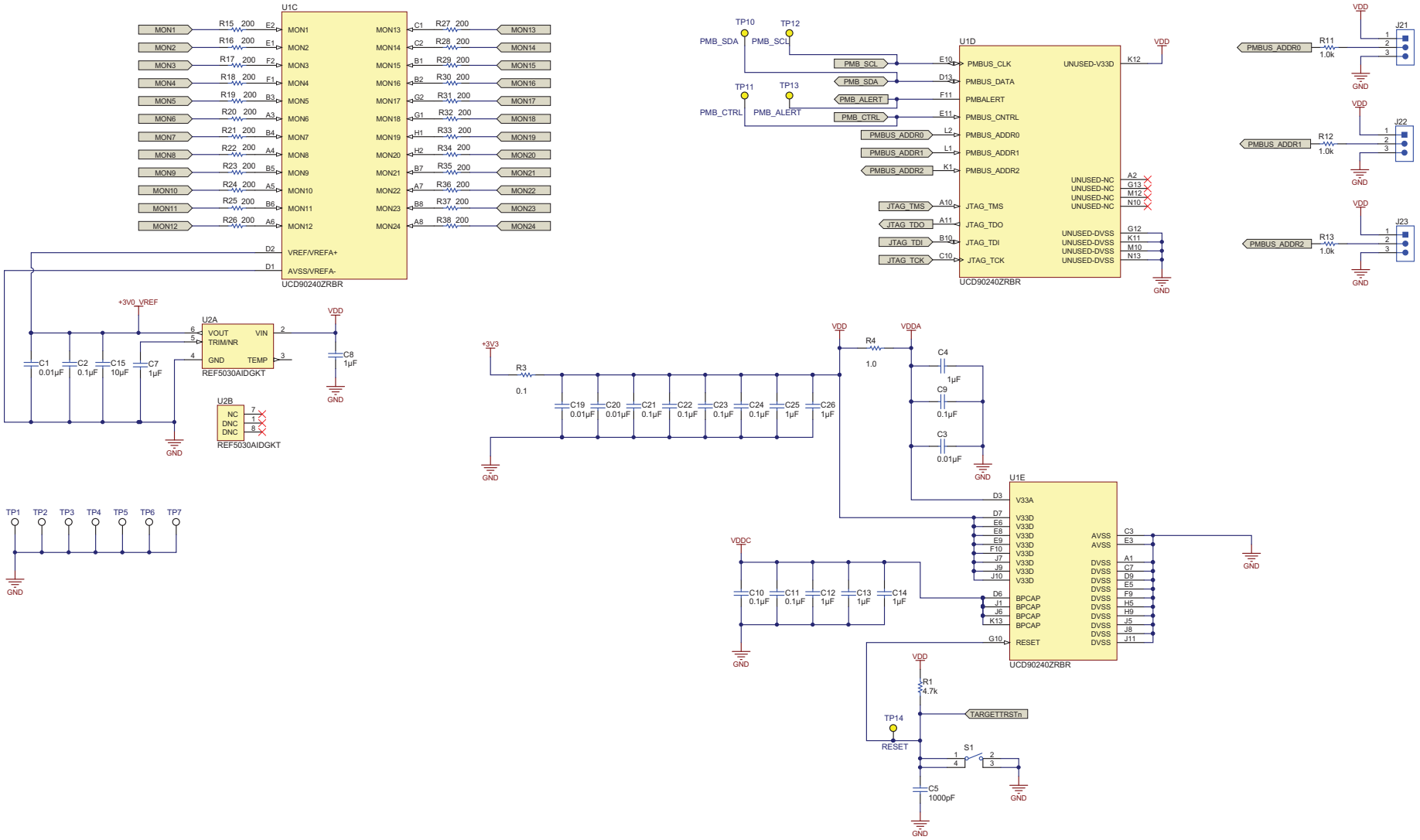


Figure 20. UCD90240EVM Schematic (3 of 6)

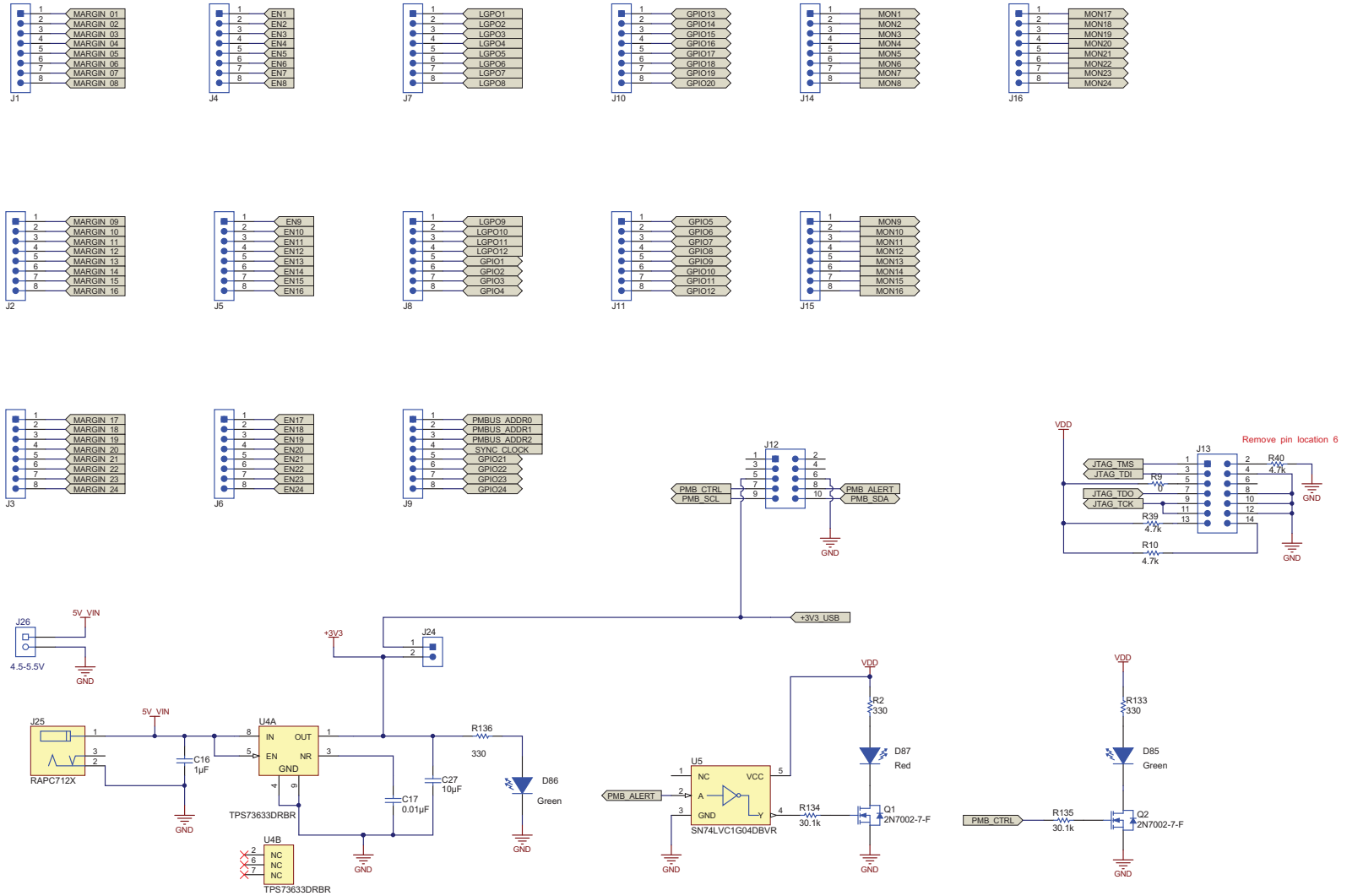


Figure 21. UCD90240EVM Schematic (4 of 6)

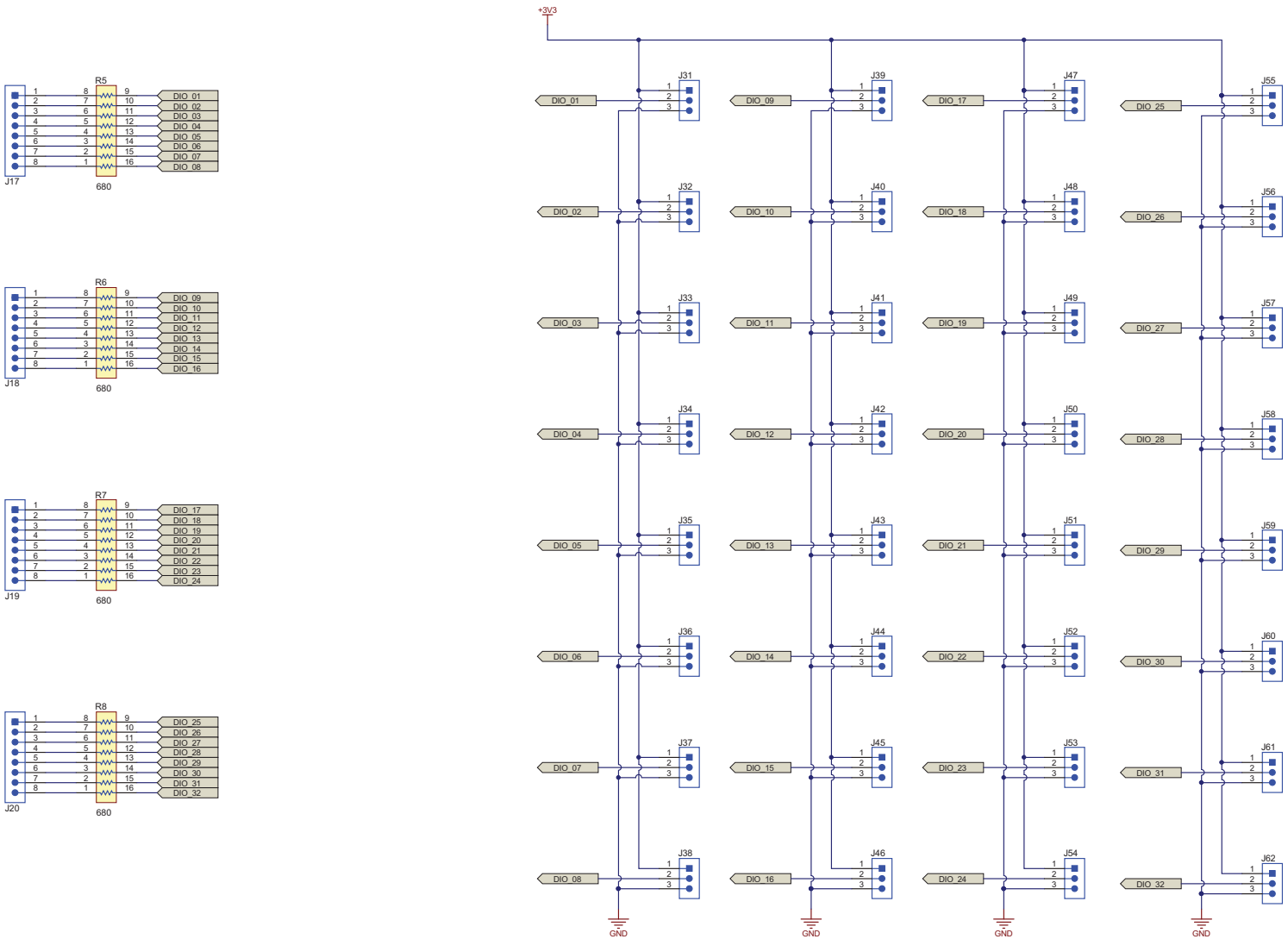


Figure 22. UCD90240EVM Schematic (5 of 6)

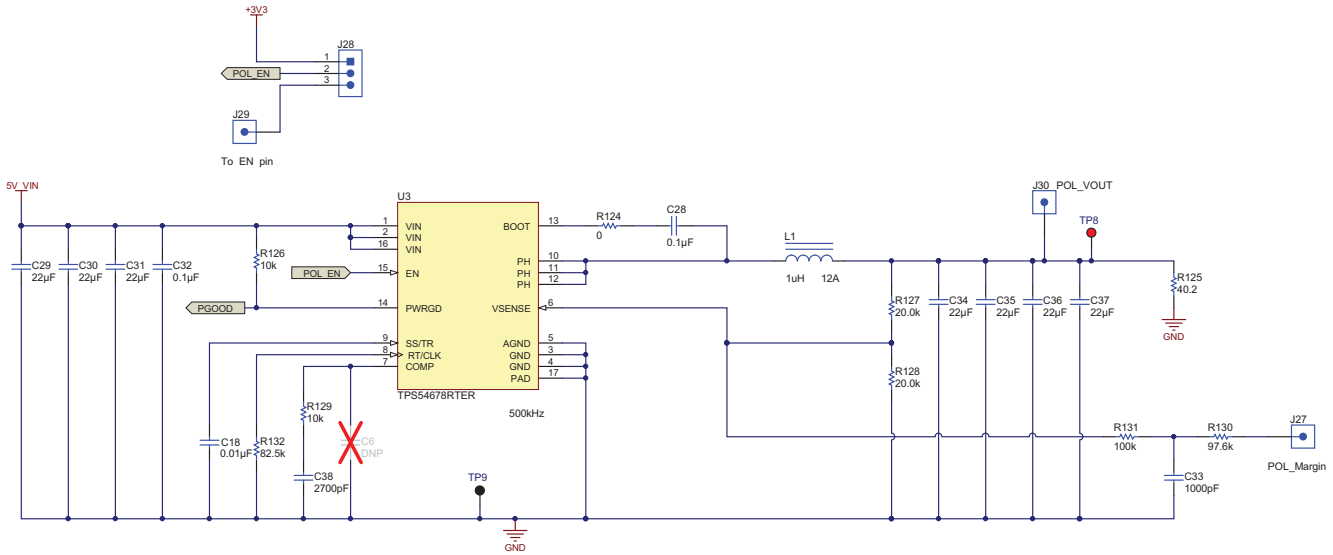


Figure 23. UCD90240EVM Schematic (6 of 6)

Revision History

Changes from Original (March 2015) to A Revision	Page
• Changed input current to 135 mA in *UCD90240EVM-704 Electrical Performance Specifications* table	3
• Changed typo in device name in several figure titles. Corrected to UCD90240EVM-704.	16

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms and conditions that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.

   2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY WRITTEN DESIGN MATERIALS PROVIDED WITH THE EVM (AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

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7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS AND CONDITIONS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

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9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

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