TPD1E01B04DPY Evaluation Module

This user's guide describes the characteristics, operation, and use of the TPD1E01B04DPY EVM evaluation module (EVM). This EVM includes six TPD1E01B04DPYs in various configurations for testing. Five TPD1E01B04DPYs are configured for IEC 61000-4-2 compliance testing and one is configured for 2-port s-parameter analysis. This user's guide includes setup instructions, schematic diagrams, a bill of materials, and printed-circuit board layout drawings for the evaluation module.

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1 Introduction

Texas Instrument's TPD1E01B04DPY evaluation module helps designers evaluate the operation and performance of the TPD1E01B04DPY device. The TPD1E01B04DPY is a unidirectional TVS ESD protection diode for HDMI 2.0 and USB 3.1 Gen II Super-speed data line protection. The TPD1E01B04DPY is rated to dissipate ESD strikes at the maximum level specified in the IEC 61000-4-2 international standard (Level 4).

The EVM contains six TPD1E01B04DPYs. Five TPD1E01B04DPYs (D1 – D5) are configured with test points for striking ESD to the protection pins. One TPD1E01B04DPY (D6) is configured with 2 SMA (J1 and J2) connectors for 2-port analysis with a vector network analyzer. TPD1E01B04DPY (D6) can also be used for capturing clamping waveforms with an oscilloscope during an ESD test. Caution must be taken when capturing clamping waveforms during an ESD event so as not to damage the oscilloscope. A proper procedure is outlined in *Section 3.3.1*.

2 Definitions

Contact Discharge — a method of testing in which the electrode of the ESD simulator is held in contact with the device-under-test (DUT).

Air Discharge — a method of testing in which the charged electrode of the ESD simulator approaches the DUT, and a spark to the DUT actuates the discharge.

ESD Simulator — a device that outputs IEC 61000-4-2 compliance ESD waveforms shown in Figure 1 with adjustable ranges shown in Table 1 and Table 2.

IEC 61000-4-2 has 4 classes of protection levels. Classes 1 – 4 are shown in Table 1. Stress tests should be incrementally tested to level 4 as shown in Table 2 until the point of failure. If the DUT does not fail at 8-kV, testing can continue in 2-kV increments until failure.

Table 1. IEC 61000-4-2 Test Levels

Contact Discharge		Air Discharge	
Class	Test Voltage [± kV]	Class	Test Voltage [± kV]
1	2	1	2
2	4	2	4
3	6	3	8
4	8	4	15

Table 2. Waveform Parameters in Contact Discharge Mode

Stress Level Step	Simulator Voltage [kV]	Ipeak ±15% [A]	Rise Time ±25% [nS]	Current at 30 ns ±30% [A]	Current at 60 ns ±30% [A]
1	2	7.5	0.8	4	2
2	4	15	0.8	8	4
3	6	22.5	0.8	12	6
4	8	30	0.8	16	8

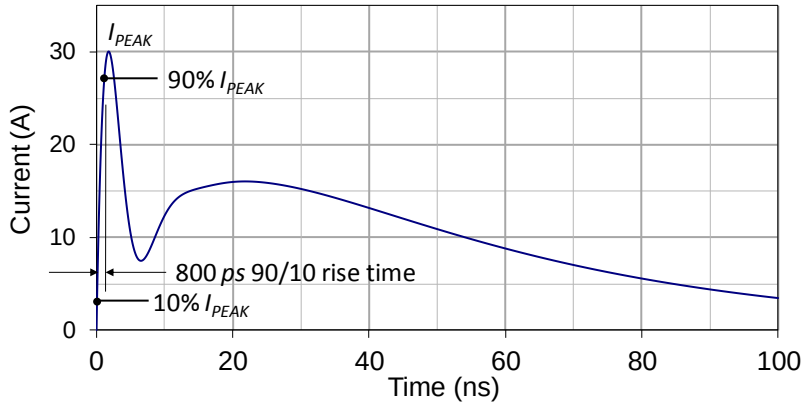

Figure 1. Ideal Contact Discharge Waveform of the Output Current of the ESD Simulator at 4-kV

3 Setup

This section describes the intended use of the EVM. A generalized outline of the procedure given in IEC 61000-4-2 is described here. IEC 61000-4-2 should be referred to for a more specific testing outline. Basic configurations for collecting s-parameters and ESD clamping waveforms are outlined as well.

3.1 IEC 61000-4-2 ESD Rating Tests

TPD1E01B04DPY (D1 – D5) can be used for destructive electrostatic discharge (ESD) pass or fail strikes. Specifically, they can be used for both IEC 61000-4-2 air and contact discharge tests. The procedure in Section 3.1.1 ensures proper testing setup and method for both discharge tests. Each IO has a Test Pad (TP1 – TP5) directly connected to it for striking ESD.

3.1.1 Test Method and Set-Up

An example test setup is shown in Figure 2. Details of the testing table and ground planes can be found in the IEC 61000-4-2 test procedure. Ground the EVM using the banana connector J3. Discharge the ESD simulator on any of the test points TP1 – TP5. Contact and air-gap discharge are tested using the same simulator with the same discharge waveform. While the simulator is in direct contact with the test point during contact, it is not during air-gap.

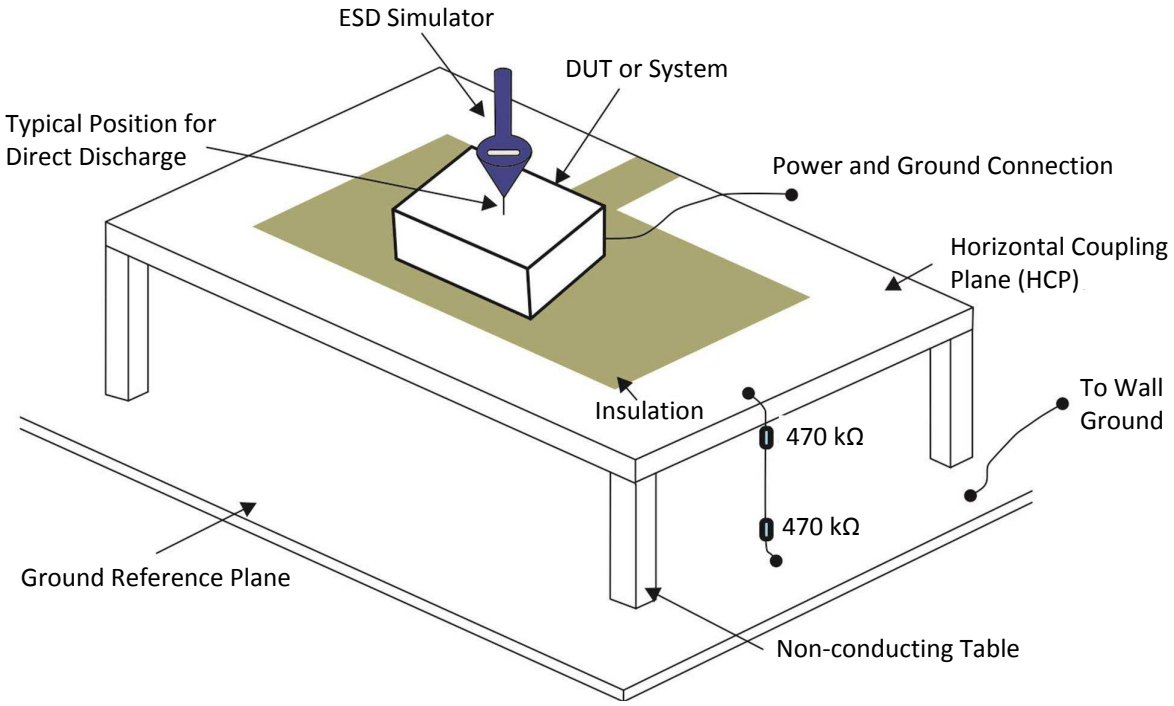

Figure 2. System Level ESD Test Setup

3.1.2 Evaluation of Test Results

Connect the tested device on the EVM to a curve tracer both before and after ESD testing. After each incremental level, if the IV-curve of the ESD protection diode shifts ±0.1 V, or leakage current increases by a factor of ten, then the device is permanently damaged by ESD.

3.2 Scattering Parameters

A TPD1E01B04DPY (D6) is configured with 2 SMA (J1 and J2) connectors to allow 2-port analysis with a vector network analyzer. Connect Port 1 to J1 and Port 2 to J2. This configuration allows for the following terminology in 2-port analysis:

- S_{11}: Return loss
- S_{21}: Insertion loss

3.3 ±8-kV ESD Clamping Waveforms

A TPD1E01B04DPY (D6) has two SMA connectors (J1 and J2) which can be used for capturing clamping waveforms with an oscilloscope during an ESD strike. Caution must be taken when capturing clamping waveforms during an ESD event so as not to damage the oscilloscope. The procedures in Section 3.3.1 outlines a proper method.

3.3.1 Oscilloscope Setup

Without a proper procedure, capturing ESD clamping waveforms exposes the oscilloscope to potential voltages higher than the rating of the equipment. Proper methodology can mitigate any risk in this operation.

Recommended Measurement Equipment:

- One 2-GHz bandwidth (minimum of 1 GHz) oscilloscope.
- Two 10X 50-Ω attenuators
- One 50-Ω shielded SMA cable.

Procedure

In order to protect the oscilloscope, attenuation of the measured signal is required. Here is a procedure for testing D3:

1. Ground the EVM using the banana connector J3.
2. Attach two 10X attenuators in series to the oscilloscope channel being used.
3. Attach the 50-Ω shielded SMA cable between J2 and the attenuators.
4. Set the scope attenuation factor to 100X.
5. Set the oscilloscope to trigger on a positive edge for (+) ESD and a negative edge for (–) ESD strikes. The trigger voltage magnitude should be set to 20 V.
6. Following Section 3.1.1, strike contact ESD to J1.Pin1.

Recommended settings for the time axis is 20 ns/div and for the voltage axis is 10 V division.

The voltage levels of the ESD applied to J1.Pin1 should not exceed ±8 kV while capturing clamping waveforms.

4 Board Layout

This section provides the TPD1E01B04DPYEVM board layout. TPD1E01B04DPYEVM is a 4-layer board of FR408HR at 0.062 inch thickness. Layers 2, 3, and 4 are ground planes and not shown here.

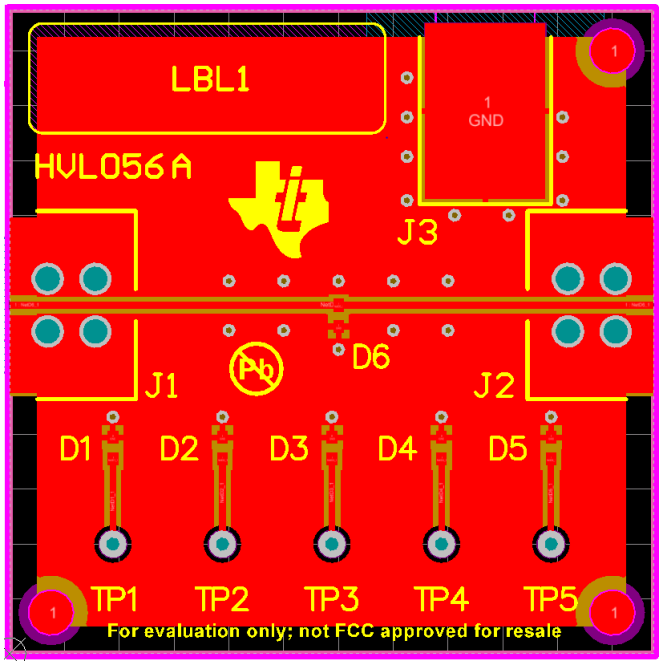

Figure 3. TPD1E01B04DPYEVM Top Layer and Silkscreen

5 Schematics

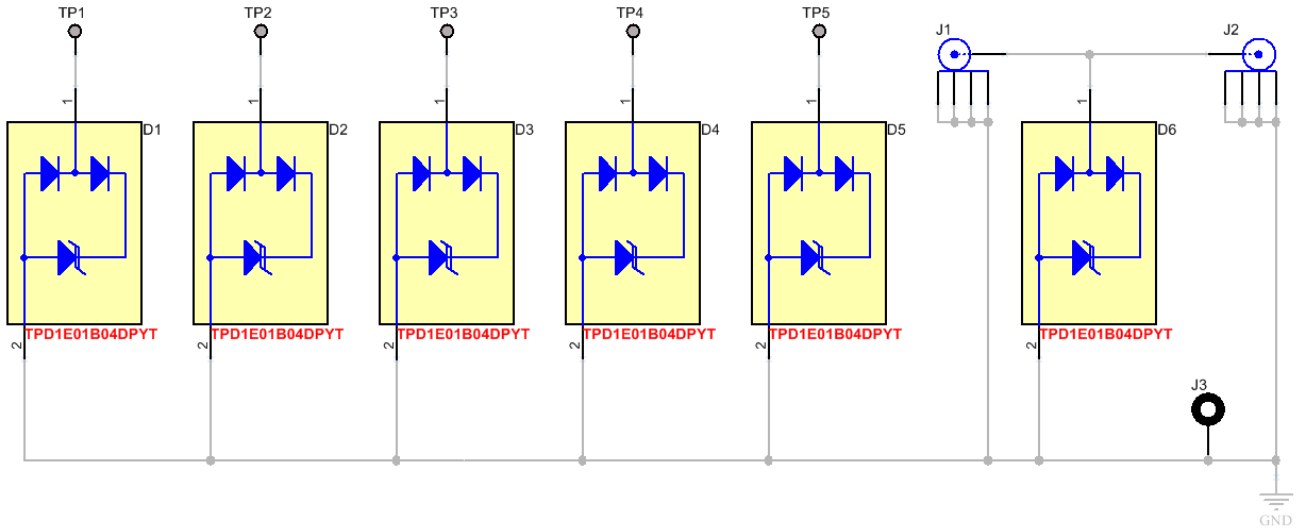

Figure 4. TPD1E01B04DPYEVM Schematic

6 Bill of Materials

Table 3. Bill of Materials

Count	RefDes	Description	Package Reference	Part Number	MFR
6	D1, D2, D3, D4, D5, D6	1-Channel ESD Protection Device for Super-Speed (up to 6 Gbps) Interface, DPY0002A	DPY0002A	TPD1E01B04DPY	Texas Instruments
2	J1, J2	Connector, TH, End launch SMA 50 Ω	Connector, TH, End launch SMA	142-0761-881	Johnson
1	J3	Standard Banana Jack, Insulated, Black	6092	6092	Keystone

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