

TRF2443 Integrated IF Transceiver Evaluation Module

This document provides an easy guide for evaluating the TRF2443 integrated IF transceiver for broadband wireless applications. Included in this guide are equipment setup procedures, software GUI configurations, and test procedures that allow a user to quickly and accurately measure the TRF2443 performance.

The TRF2443 is a fully integrated IF transceiver operating at a transmitter IF of 340 MHz (or 170 MHz) and a receiver IF of 140 MHz (or 280MHz). The IF transceiver is used to for up-conversion of signals from the transmit chain digital-to-analog convertor (DAC) to the RF upconverter device and for down-conversion of received IF signals to baseband for processing by the analog-to-digital convertor (ADC). The receiver allows for switching in an external SAW filter if needed or by-passing this filter and processing the signal completely internally. The TRF2443 also provides an Auxiliary Receiver which can be used for cross-polarization interference cancellation (XPIC). This document describes how to test the TRF2443 as well as the many options for trimming the device configuration to meet your application needs.

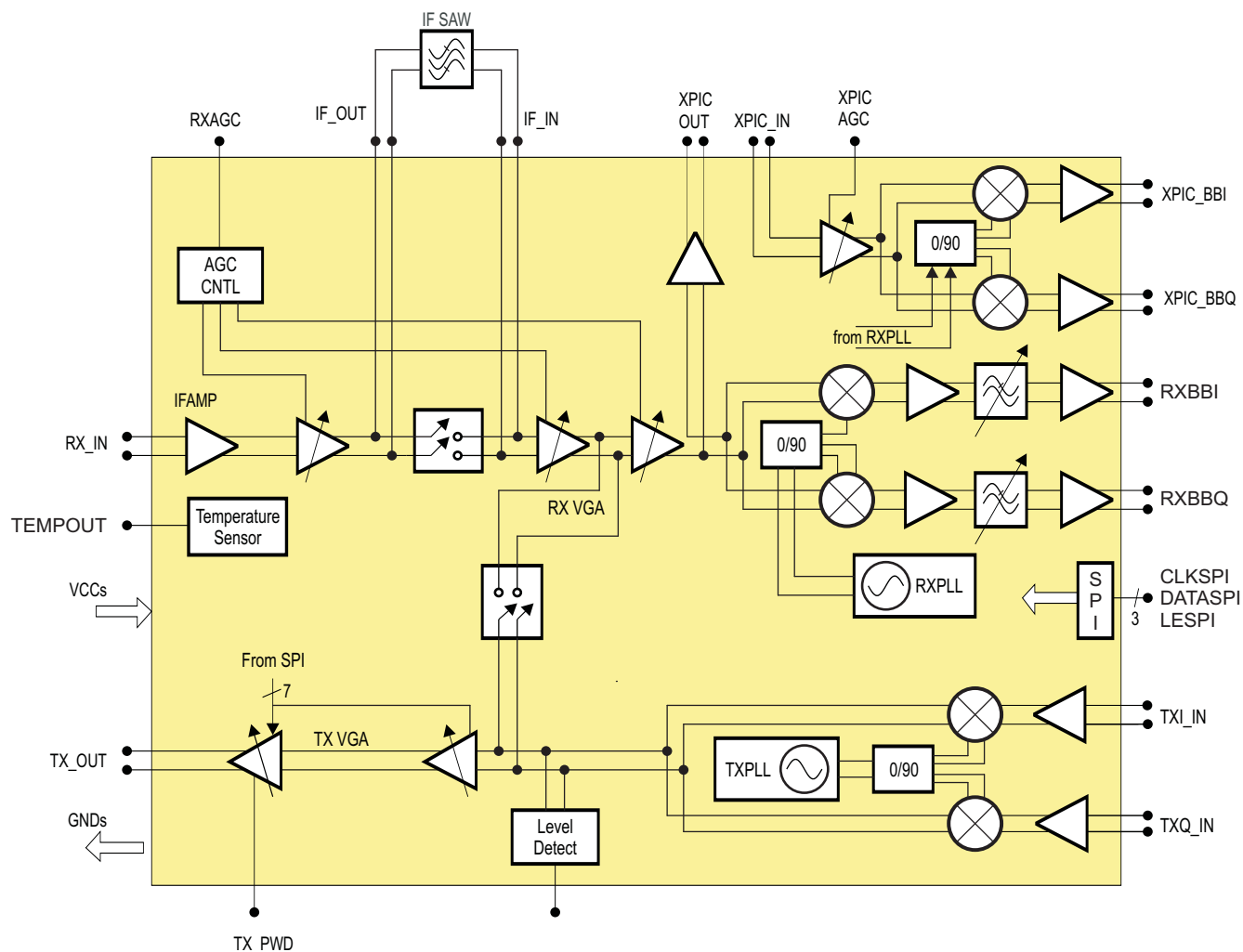


Figure 1. TRF2443 Block Diagram

Contents

1	EVM Circuit Overview	4
	1.1 DC POWER	4
	1.2 Reference Clock	5
	1.3 Communications	5
	1.4 Transmitter.....	5
	1.5 Receiver.....	6
	1.6 XPIC Receiver.....	9
2	GUI Overview	10
	2.1 GUI for Synthesizers.....	12
	2.2 GUI for Receiver.....	14
	2.3 GUI Transmitter.....	15
	2.4 GUI for XPIC Receiver	15
3	TRF2443 EVM Operating Procedures.....	16
	3.1 Power Up	16
	3.2 Receiver	17
	3.3 XPICOUT Amplifier	18
	3.4 Transmitter	19
	3.5 EEPROM	20
	3.6 XPIC RECEIVER	21
4	Physical Description	23
	4.1 EVM Top Layer Drawing	23
	4.2 Bill of Materials	24
	4.3 Schematics.....	26

List of Figures

1	TRF2443 Block Diagram.....	1
2	TXPWD Header JP1 Schematic	4
3	EVM DC Power: J1, J2, and JP1	4
4	EVM Reference Clock J3 and USB Port J5	5
5	TX Baseband Inputs.....	6
6	J7 (RXIN)	6
7	RX Baseband Outputs	7
8	SAW Filter Path	8
9	XPIC RX	9
10	TRF2443 GUI Quick-Set Tab.....	10
11	TRF2443 GUI Advanced Tab.....	11
12	Load All Registers.....	12
13	Reset USB	12
14	Synthesizer Programming.....	12
15	RX GUI	14
16	RX AGC GUI.....	14
17	Transmitter GUI.....	15
18	XPIC Receiver GUI	15
19	XPIC AGC GUI	15
20	Programmed ICC GUI Settings.....	16
21	Load All Registers.....	16
22	Receiver SAW Disabled GUI Settings.....	17
23	Receiver SAW Enabled GUI Settings	18
24	Receiver XPICOUT GUI Settings	19
25	TX Max Gain GUI Settings.....	19
26	GUI Settings for TX Carrier Leakage	20
27	GUI Show Readback	20

28	GUI Select EEPROM Readback	20
29	Read I/Q Carrier Leakage Trim Values B<10,5>	21
30	TX Carrier Leakage Trim	21
31	XPIC Receiver Max Gain GUI	22
32	XPIC Receiver Min Gain GUI	22
33	TRF2443 EVM Top Layer	23
34	Schematic (1 of 5)	26
35	Schematic (2 of 5)	27
36	Schematic (3 of 5)	28
37	Schematic (4 of 5)	29
38	Schematic (5 of 5)	30

List of Tables

1	Bill of Materials	24
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1 EVM Circuit Overview

1.1 DC POWER

The TRF2443 EVM requires a 3.3V dc power-supply connected to between J1 (3.3V) and J2 (GND). The TRF2443 allows for analog or digital control of the transmitter power supply. Pin 1 (TXPWD) of the device provides the analog control and is connected to header JP1 (TXPWD) on the EVM. When pins 1 and 2 of header JP1 are shorted, 3.3V is fed to the TXPWD pin and the transmitter is disabled. When pins 2 and 3 of header JP1 are shorted, 0V is fed to the TXPWD pin and the transmitter is enabled (see [Figure 2](#) and [Figure 3](#)). With header JP1 enabling the transmitter, it is still possible for the transmitter to be off due to the state of the digital TX control.

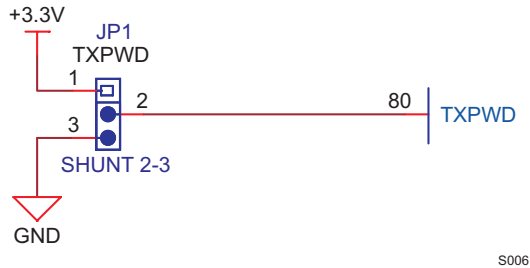


Figure 2. TXPWD Header JP1 Schematic

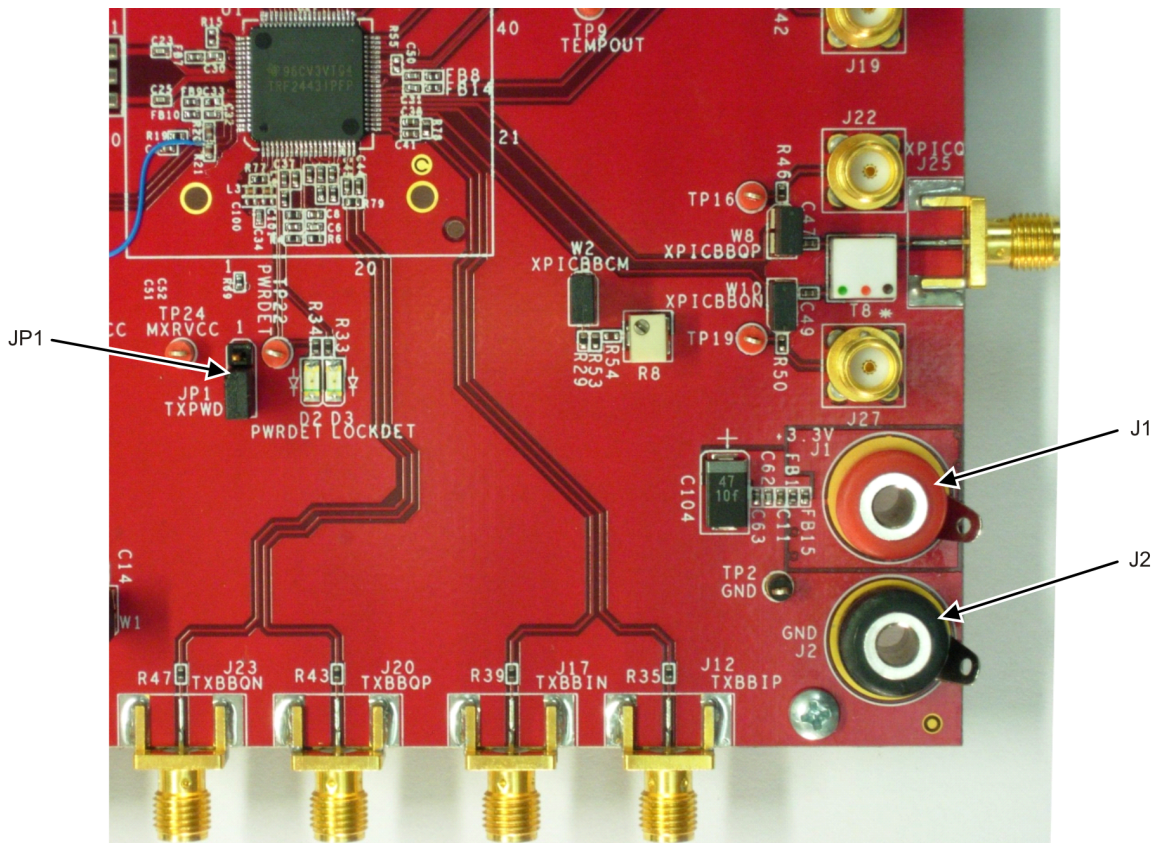


Figure 3. EVM DC Power: J1, J2, and JP1

1.2 Reference Clock

The TRF2443 EVM allows for either an external reference chosen by the user or an internal oscillator at 20 MHz provided on the EVM board. If an external reference is to be used the signal should be fed into SMA connector J3 (EXTREF) and jumpers W1 and W12 should be removed (see [Figure 4](#)).

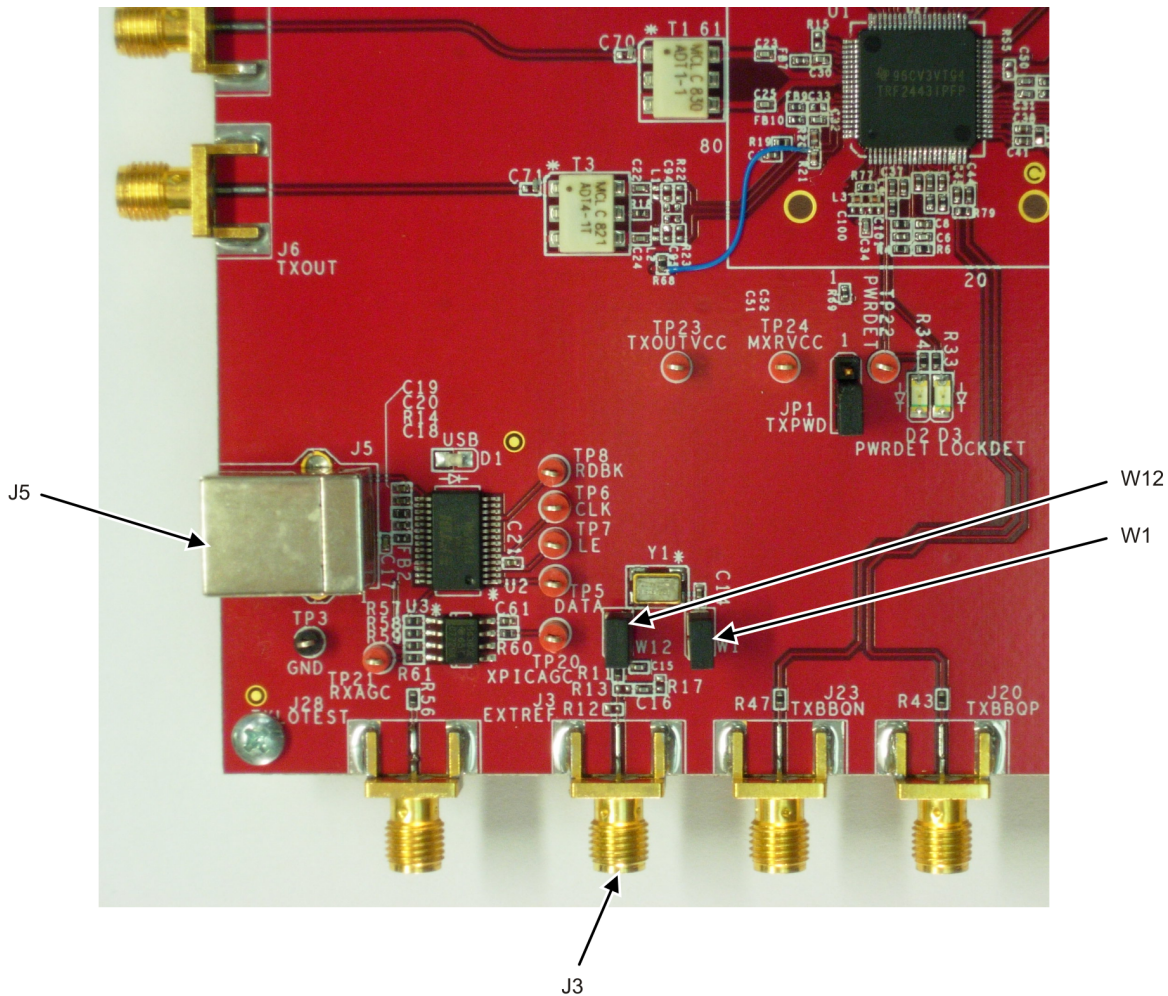


Figure 4. EVM Reference Clock J3 and USB Port J5

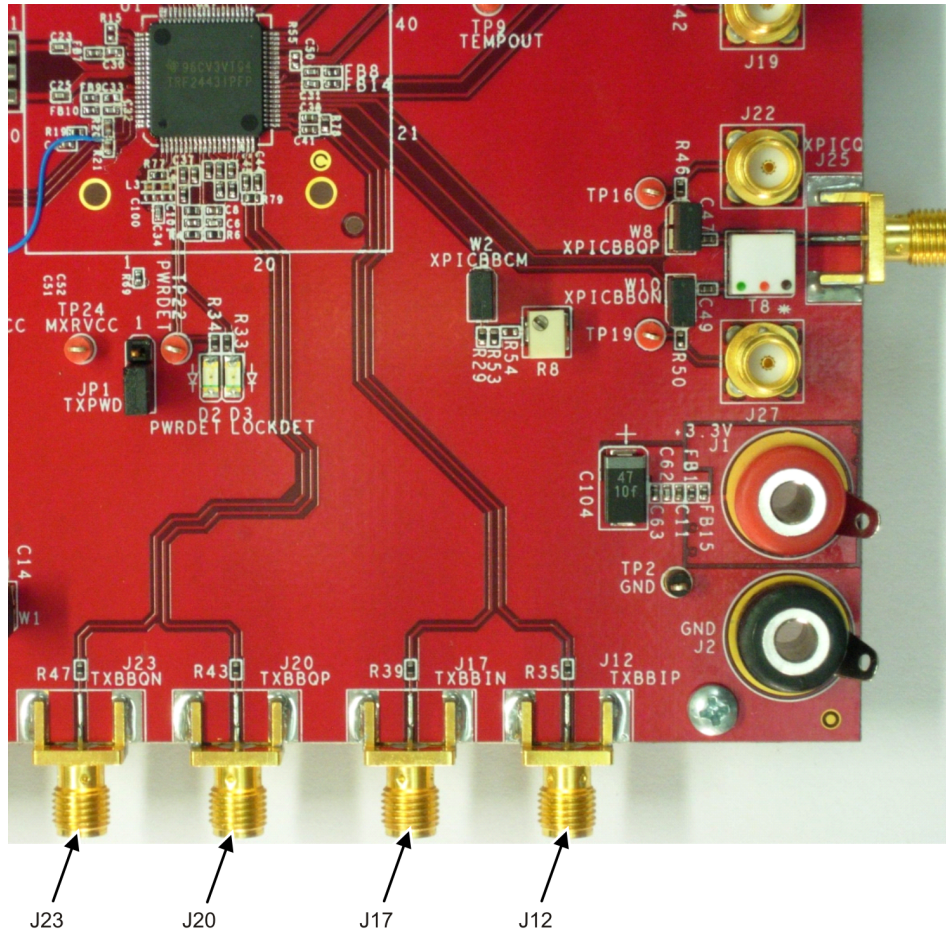
J002

1.3 Communications

The EVM is equipped with USB communications which provide the interface between a computer's USB port and the TRF2443s SPI port via J5 as shown in [Figure 4](#). A CD containing the GUI to control the TRF2443 is provided within the EVM kit. An overview of the GUI is provided in this document

1.4 Transmitter

The EVM is configured for differential I/Q input signals via four SMA connectors. For the upper sideband, the I signals are connected to J12 (TXBBIP) and J17 (TXBBIN). The Q signals are connected to J23 (TXBBQN) and J20 (TXBBQP) (see [Figure 5](#)). SMA connector J6 (TXOUT), not shown below, is used to monitor the RF output signal from the transmitter.

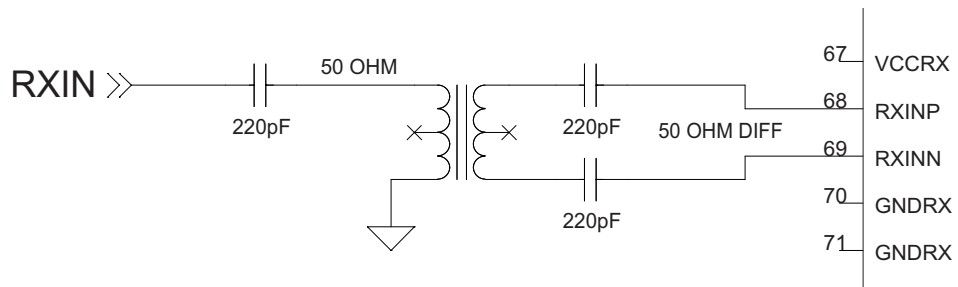


J006

Figure 5. TX Baseband Inputs

1.5 Receiver

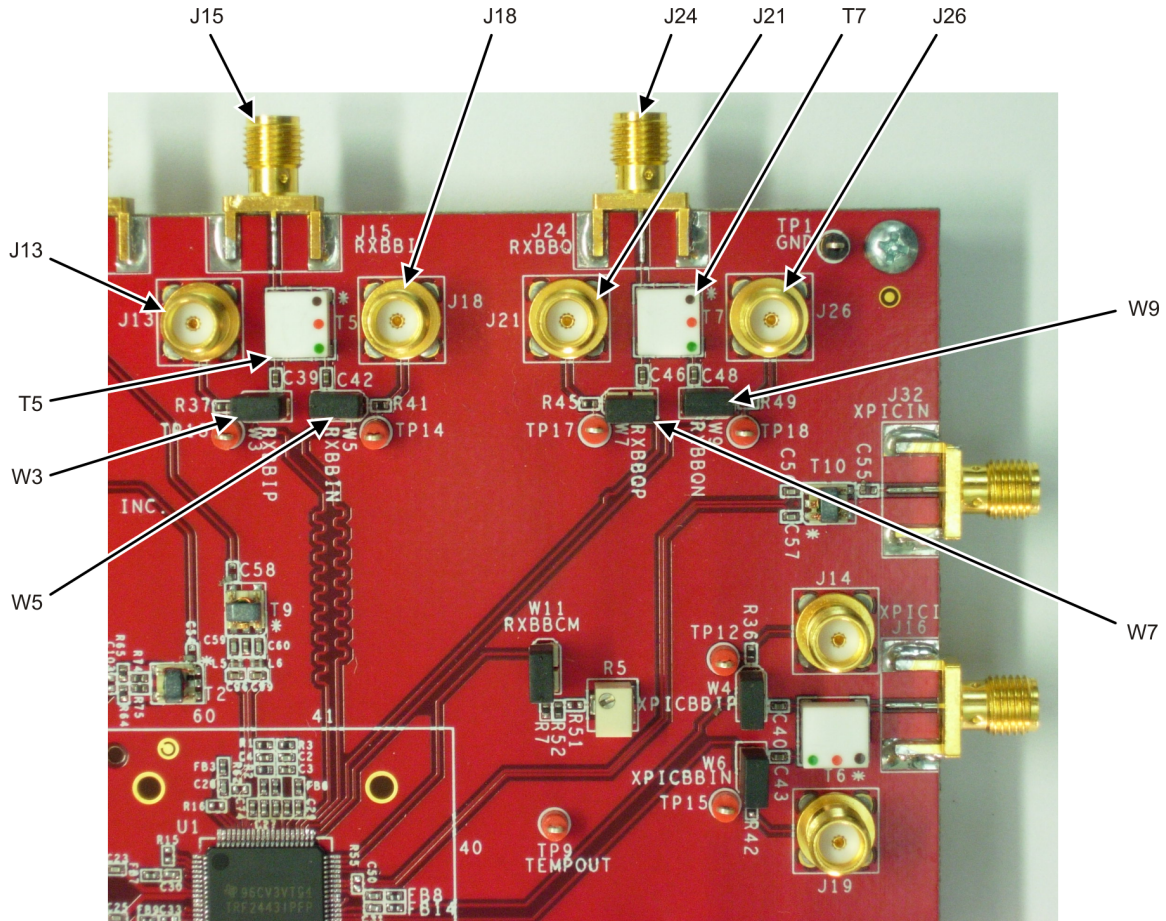
The EVM is configured for single ended RX input signal via SMA connector J7 (RXIN). This input is taken through a 1:1 balun to provide differential inputs to the device. The device presents 50 so no external termination resistor is required.



S007

Figure 6. J7 (RXIN)

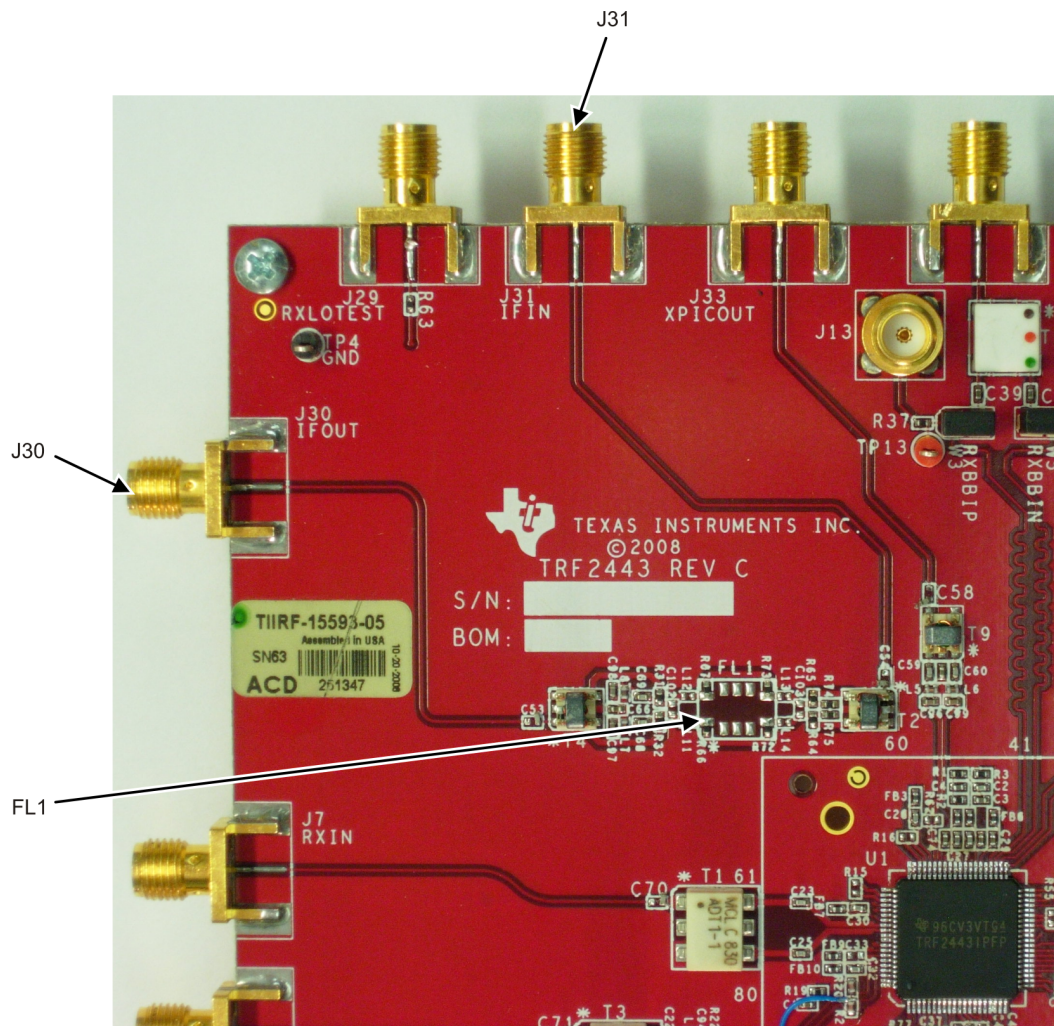
The baseband I/Q signals can be measured balanced or unbalanced. The I output is taken from the unbalanced port J15 (RXBBT) through balun T5 or from the balanced ports of J13 (I+) and J18 (I-). Likewise, the Q output is taken from the unbalanced port J24 (RXBBQ) through balun T7 or the balanced ports of J21 (Q+) and J26 (Q-). For balanced mode measurements, jumpers W3, W5, W7 and W9 must be removed.



J003

Figure 7. RX Baseband Outputs

The TRF2443 RX path allows the use of an external SAW filter. An internal switch, which is programmable through the serial interface, gives the flexibility to utilize the external filter (see Figure 1). The internal switch is controlled via the serial programming interface through bit EN_SAW. By programming EN_SAW to 1, the external path is selected, whereas a 0 engages the internal bypass switch. When EN_SAW is set to 1 the IF signal will be routed out of the IC to SMA connector J30 (IFOUT) (see Figure 8). At this point, the user has the flexibility to insert a filter of choice outside the TRF2443 EVM. (The board does contain a place holder (FL1) for a SAW filter but is not populated. In this way, the user has the flexibility to use a filter of his choice). For initial evaluation, an 8-10 dB pad can be used in lieu of a filter to emulate the insertion loss of a typical filter. The user must route the signal from J30 (IFOUT) to J31 (IFIN) with the filter or pad included.



J004

Figure 8. SAW Filter Path

1.6 XPIC Receiver

The TRF2443 provides an auxiliary receiver chain that can be used for cross-polarization interference cancellation purposes. The EVM is configured for a single-ended output signal (intended for the secondary XPIC RX path) at J33 (XPICOUT). The input to the XPIC receiver (from the XPICOUT of the secondary XPIC RX path) is available at SMA connector J32 (XPICIN). This input is taken through a 1:1.5 balun to provide differential inputs to the device. The device presents 75 Ω so no external termination resistor is required. The XPIC baseband I and Q signals can be measured balanced or unbalanced. The I output is taken from the unbalanced port J16 (XPICI) through balun T6 or from the balanced ports of J14 (I+) and J19 (I-). Likewise, the Q output is taken from the unbalanced port J25 (XPICQ) through balun T8 or the balanced ports of J22 (Q+) and J27 (Q-). For balanced mode measurements, jumpers W4, W6, W8, and W10 must be removed (see Figure 9).

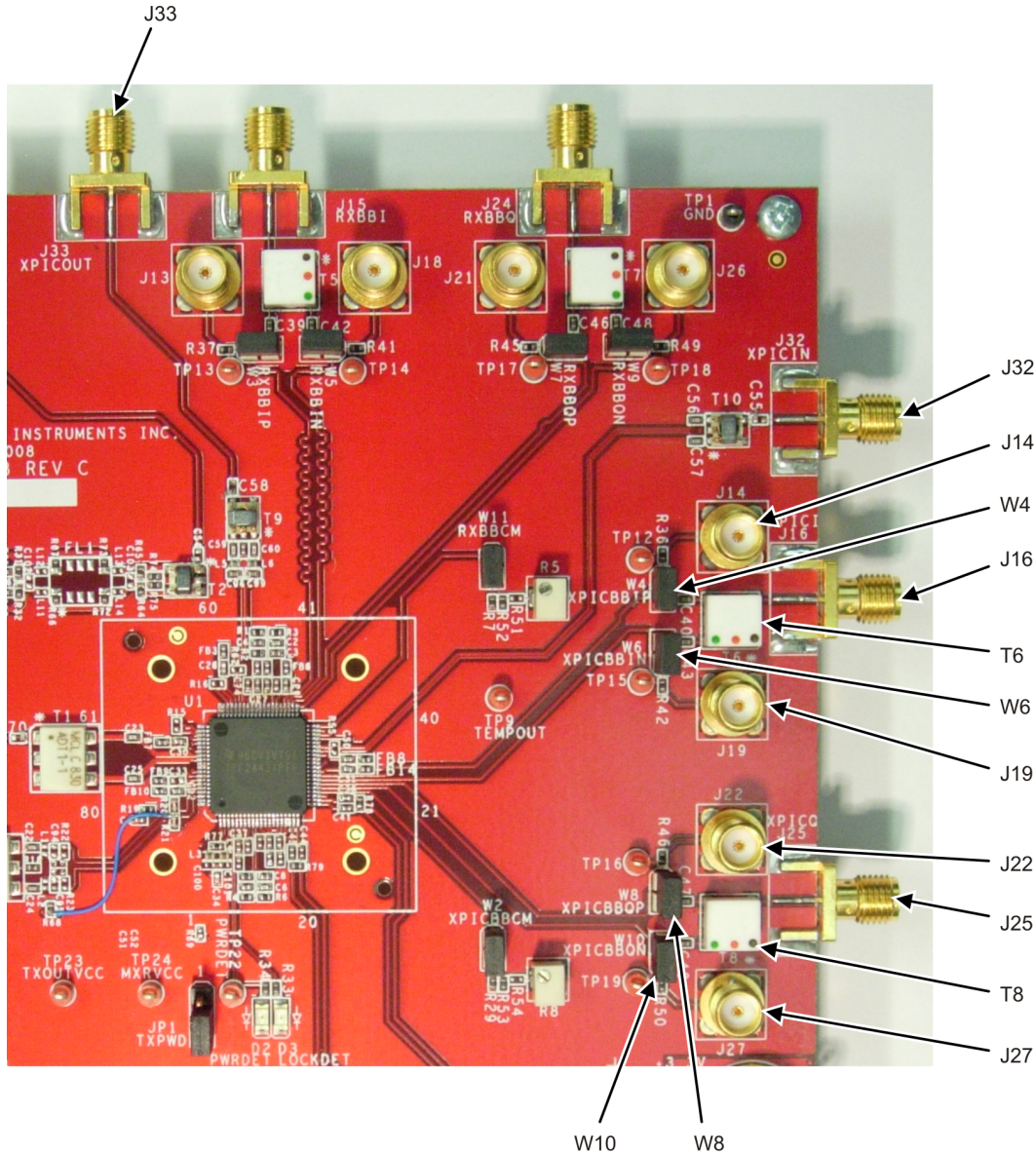


Figure 9. XPIC RX

J005

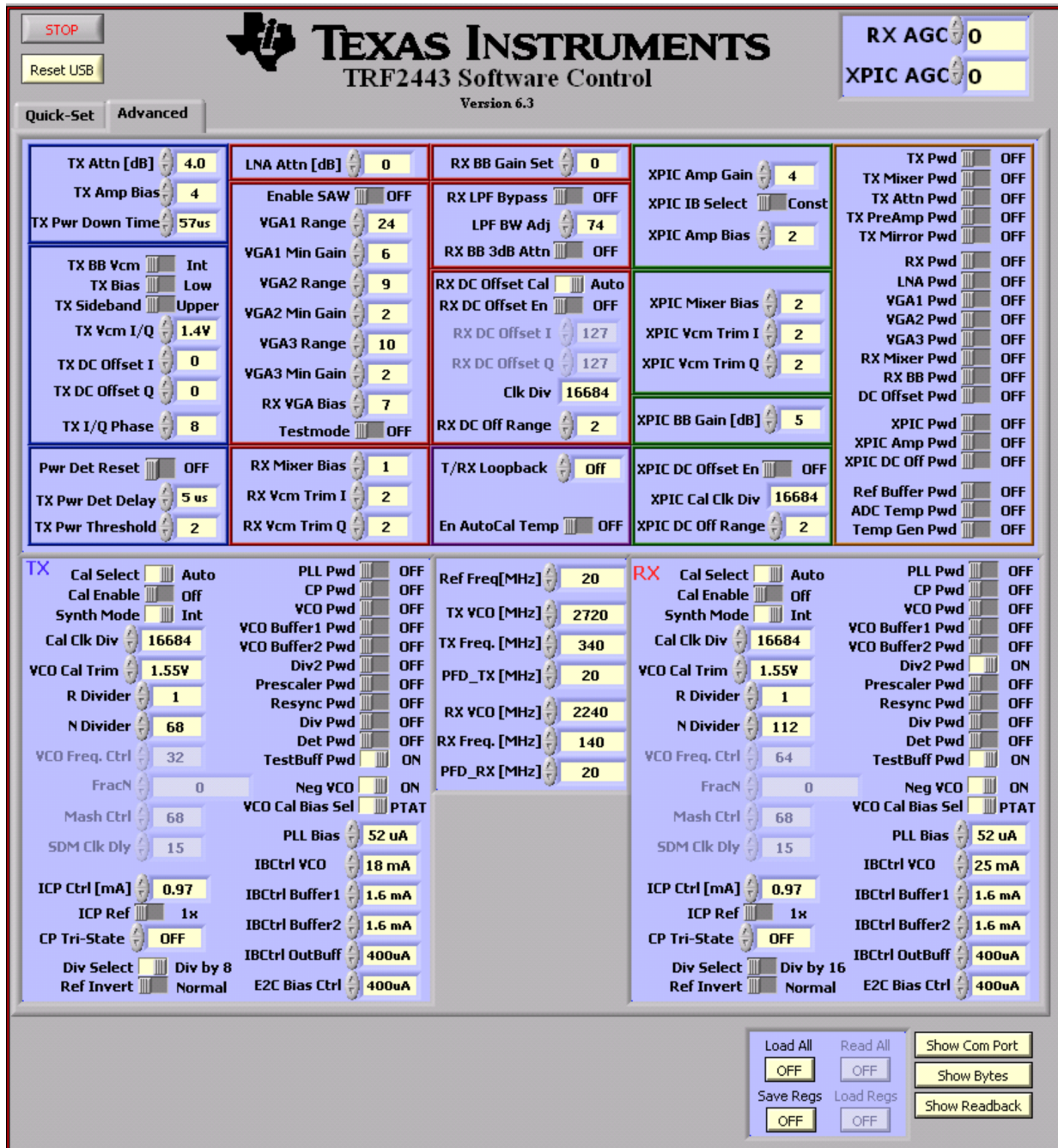
2 GUI Overview

The TRF2443 EVM kit includes a graphical user interface for controlling the device. The GUI contains two tabs labeled "Quick-set" and "Advanced" (see Figure 10 and Figure 11)

The screenshot displays the TRF2443 Software Control GUI, Version 6.4. The interface is divided into two main sections: 'Quick-TRX' and 'Quick-Synth'. The 'Quick-TRX' section contains several control blocks with sliders and checkboxes for parameters such as LNA Attn [dB], TX Attn [dB], Enable SAW, T/RX Loopback, RX BB Gain Set, XPIC BB Gain Set, RX DC Offset En, XPIC DC Offset En, RX LPF Bypass, LPF BW Adj, and RX BB 3dB Attn. The 'Quick-Synth' section includes sliders for Ref Freq [MHz], TX VCO [MHz], TX Freq. [MHz], PFD_TX [MHz], RX VCO [MHz], and RX Freq. [MHz], along with checkboxes for T/Rx Cal Enable, TX Synth Range, and RX Synth Range. Below these controls is a detailed block diagram of the TRF2443 chip, showing the internal architecture including AGC CNTL, IF AMP, RX VGA, TX VGA, TXPLL, and RXPLL blocks, and their connections to various pins like RX_IN, IF_OUT, IF_IN, XPIC_OUT, XPIC_IN, XPIC_BBI, XPIC_BBO, TXI_IN, TXO_IN, TX_OUT, and TX_PWD. At the bottom right of the GUI, there are buttons for 'Load All', 'Read All', 'Show Com Port', 'Save Regs', 'Load Regs', 'Show Bytes', and 'Show Readback'.

C001

Figure 10. TRF2443 GUI Quick-Set Tab



C002

Figure 11. TRF2443 GUI Advanced Tab

Evaluation and testing of the device can be done entirely using on the "Quick-set" tab. The "Advanced" tab is used for debugging and specific optimization of the device if required by an application. Using the "Advanced" tab without an understanding of what is being controlled can result in an unrecoverable state of the IC whereby a power reset would be required.

When an input to the GUI is changed, the GUI should send this new value to the device automatically once the cursor has clicked on another field besides the field being changed. It is good practice, however, to reload all registers once changes to inputs have been made. This can be achieved by clicking on the "OFF" button below "Load All" in the bottom right corner of the GUI (see [Figure 12](#)).

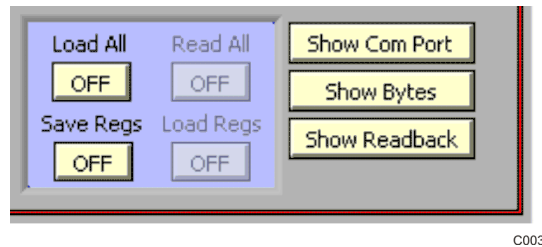


Figure 12. Load All Registers

If there is ever a doubt as to the integrity of the communications between the GUI and the device, a USB reset is in order. Press the Reset USB button near the top left corner of the GUI and then reload all registers again (see [Figure 13](#)).

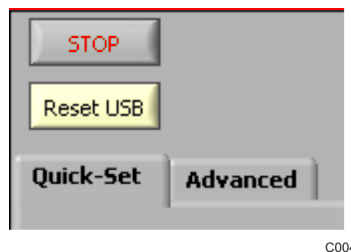


Figure 13. Reset USB

An explanation of all the fields within the Quick-set tab is provided by device functionality beginning with the synthesizers.

2.1 GUI for Synthesizers

The TX and RX synthesizers are controlled using the group of dialog boxes under "Quick-Synth" (see [Figure 14](#)).

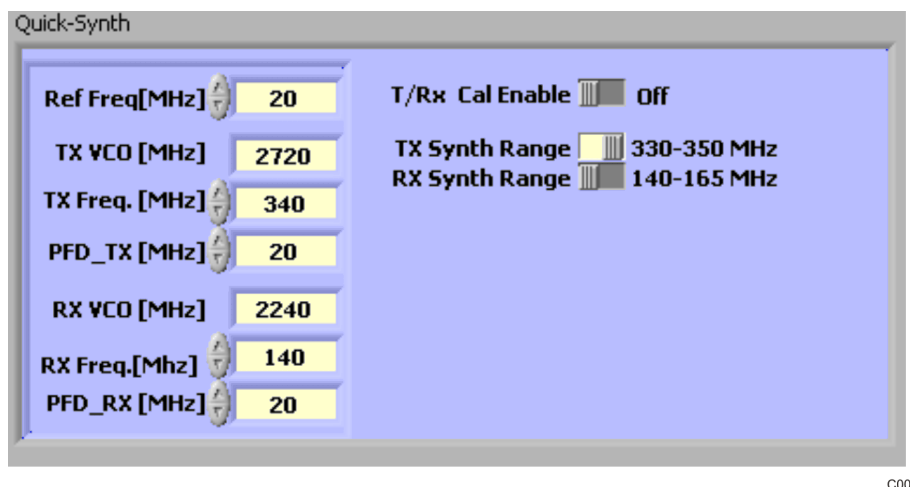


Figure 14. Synthesizer Programming

Ref Freq[MHz]

Specify the reference frequency being provided to the EVM. If the on-board oscillator is used, this will be 20MHz. If an external oscillator is to be used, specify its frequency in this field.

TX VCO [MHz]

This field is a calculation based on the other inputs provided. The TX VCO is guaranteed to operate between 2640MHz and 2800MHz.

TX Freq. [MHz]

The TX LO Frequency can be programmed to a frequency within the TX Synth Range selected previously. Entering a value outside of this range is not permitted and will default to the closest value within this range. When TX Freq. is specified, the corresponding TX VCO will be calculated.

PFD_TX [MHz]

Specify the channel resolution desired of the LO by selecting the PFD frequency. Note that the PLL loop filters are optimized for a PFD frequency of 20MHz. Deviating from 20MHz will impact the phase noise of the system.

RX VCO [MHz]

This field is a calculation based on the other inputs provided. The RX VCO is guaranteed to operate between 2240MHz and 2640MHz.

RX Freq. [MHz]

The RX LO Frequency can be programmed to a frequency within the RX Synth Range selected previously. Entering a value outside of this range is not permitted and will default to the closest value within this range. When RX Freq. is specified, the corresponding RX VCO will be calculated.

PFD_RX [MHz]

Specify the channel resolution desired of the LO by selecting the PFD frequency. Note that the PLL loop filters on the EVM are optimized for a PFD frequency of 20MHz. Deviating from 20MHz will impact the stability and phase noise of the system.

T/RX Cal Enable

Toggleing this invokes a calibration of the RX and TX PLLs and initiates locking the synthesizers. This field must be toggled ON in order to lock the synthesizers. Loading all registers using the button on the bottom right corner of the GUI does not perform this task.

TX Synth Range

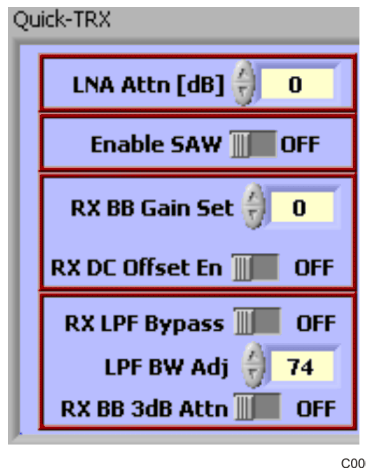
The TRF2443 transmitter LO can be programmed to a frequency between 165–175MHz or 330–350MHz. Select the range that covers the desired to program the appropriate dividers.

RX Synth Range

The TRF2243 receiver LO can be programmed to a frequency between 140–165MHz or 280–330MHz. Select the range that covers the desired application to program the appropriate dividers.

2.2 GUI for Receiver

The TRF2243 receiver is controlled using the group of dialog boxes to the left half of the Quick-TRX section (see [Figure 15](#)).



C006

Figure 15. RX GUI

LNA Attn [dB]

Specifies the LNA attenuation desired in dB.

Enable SAW

Specifies whether the external SAW filter path or the internal bypass path is used for the receiver.

RX BB Gain Set

Specifies the gain setting for the RX baseband section. The value entered here is a gain setting and not gain in dB. This value is 9 dB less than the actual gain (i.e., enter 0 for 9dB of gain; enter 24 for 33dB of gain on the RX baseband).

RX DC Offset En

Toggling this button invokes a DC offset calibration of the RX baseband circuitry. This is recommended after changing the RX BB Gain.

RX LPF Bypass

Specify whether to bypass the internal low pass filter or not.

LPF BW Adj

If RX LPF Bypass is OFF then the low pass filter is enabled and its corner frequency can be programmed to any of 128 states specified to cover 2 MHz to 11MHz corner frequency [see TRF2443 datasheet for detailed explanation ([SLWS217](#))]

RX BB 3dB Attn

Specify whether to enable a 3 dB attenuator at the output of the device. This can be used to tradeoff noise and IP3 in some configurations.

RX AGC

The analog gain control of the receiver chain is located in the upper right corner of the GUI and is in mV (see [Figure 16](#)) .

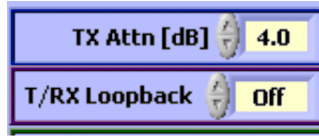


C007

Figure 16. RX AGC GUI

2.3 GUI Transmitter

Control of the transmitter is located in the second column within the Quick-TRX section (see [Figure 17](#)).



C008

Figure 17. Transmitter GUI

TX Attn [dB]

Controls the attenuation from maximum gain of the transmitter chain.

T/RX Loopback

Enables the path for looping back the TX signal into the receiver with a 0 dB loss or a 20 dB loss in the path depending on selection. This can be used for calibrating the RX baseband low pass filter corner frequency or calibrating the TX modulator LO leakage calibration [see TRF2443 datasheet for detailed explanation ([SLWS217](#))].

2.4 GUI for XPIC Receiver

Control of the XPIC receiver is located in the second column within the Quick-TRX section (see [Figure 18](#)).



C009

Figure 18. XPIC Receiver GUI

XPIC BB Gain [dB]

Specifies the gain setting for the XPIC RX baseband section. The value entered here is a gain setting and not gain in dB. This value is 9 dB less than the actual gain (i.e., enter 0 for 9dB of gain or enter 5 for 14dB of gain).

XPIC DC Offset En

Toggling this button invokes a DC offset calibration of the XPIC RX baseband circuitry. This is recommended after changed the XPIC BB Gain.

RX AGC

The analog gain control of the XPIC receiver chain is located in the upper right corner of the GUI and is in mV (see [Figure 19](#)).



C010

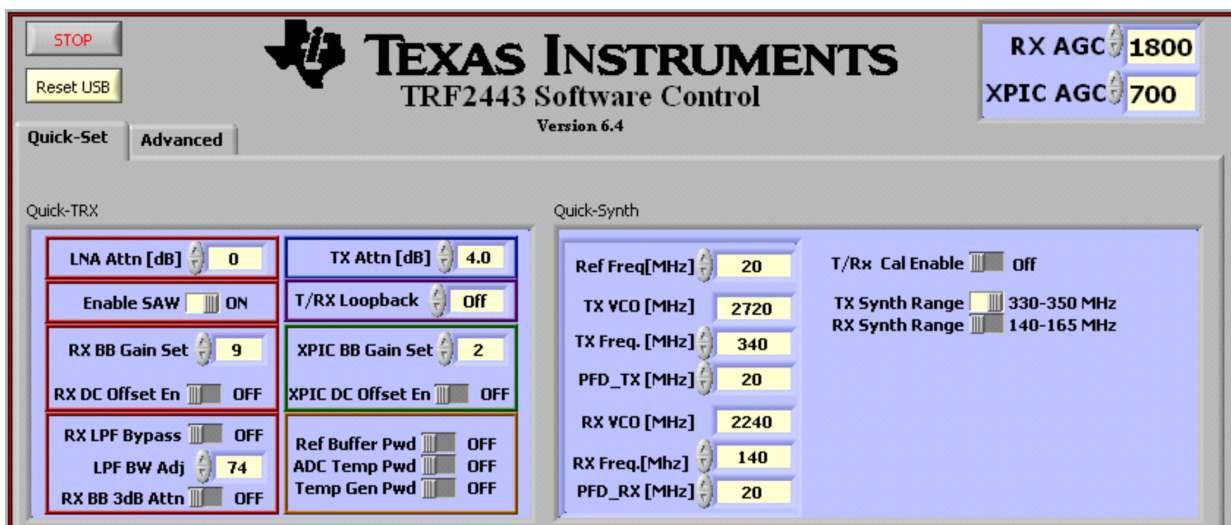
Figure 19. XPIC AGC GUI

3 TRF2443 EVM Operating Procedures

This section will outline step by step the procedures necessary to test the following functions of the TRF2443:

3.1 Power Up

- a. Initial ICC
 - i. Apply 3.3V DC between J1 and J2 connections on board.
 - ii. Approximately 760mA should be drawn from the power supply.
- b. Programmed ICC
 - i. Apply reference clock either externally or using on board oscillator (see section Reference Clock)
 - ii. Apply USB connection between computer with loaded GUI and USB port J5 on the EVM and press the Reset USB button in the upper left corner of the GUI.
 - iii. Change the GUI inputs as shown in [Figure 20](#).



C011

Figure 20. Programmed ICC GUI Settings

- iv. Load all registers by pressing the OFF button below Load All in the bottom right corner of the GUI to load all registers to the device (see [Figure 21](#)).



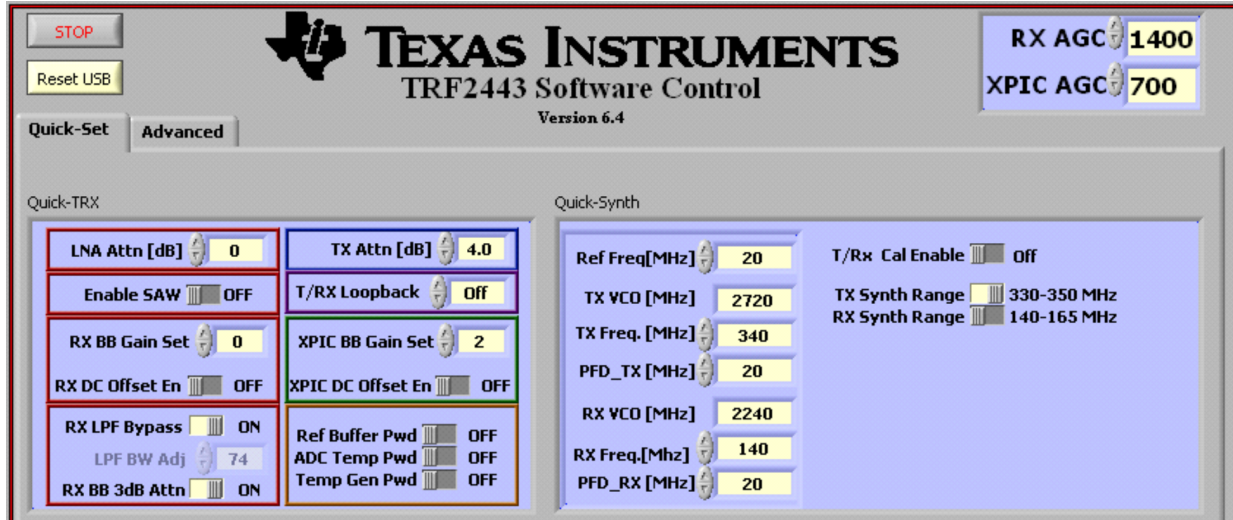
C012

Figure 21. Load All Registers

- v. Toggle the T/Rx Cal Enable button to lock the synthesizers.
- vi. Approximately 1070mA of current should be drawn from the power supply with this device configuration.

3.2 Receiver

- a. SAW path disabled
 - i. Program GUI as shown in [Figure 22](#).
 - ii. Toggle the T/Rx Cal Enable button to lock the synthesizers.

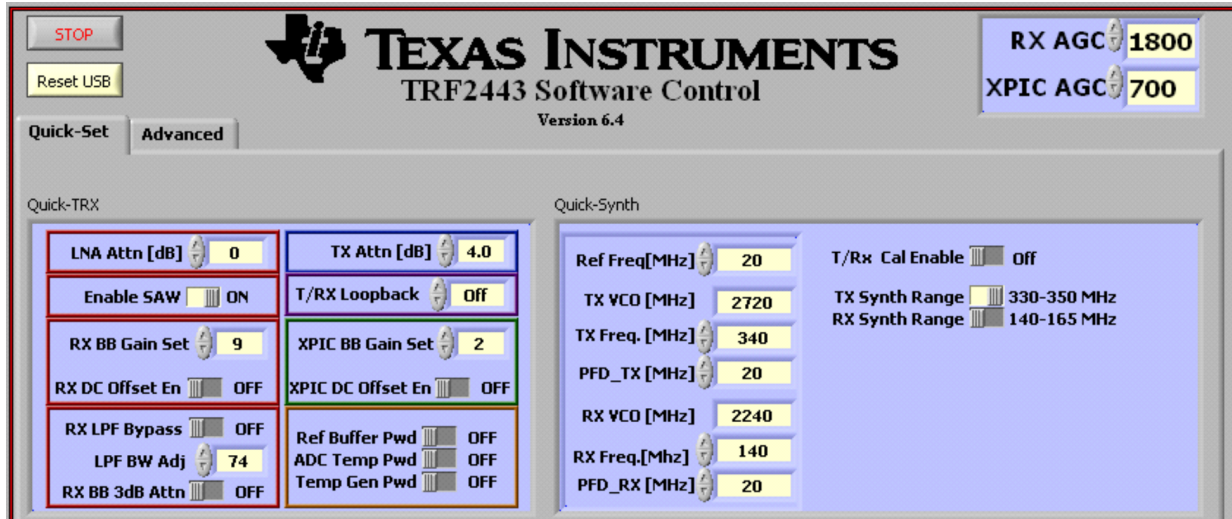


C013

Figure 22. Receiver SAW Disabled GUI Settings

- iii. Apply CW signal to J7-RXIN port at 140.1MHz, -88dBm.
- iv. Measure output on spectrum analyzer at J15 (RXBBI) or J24 (RXBBQ) at 100kHz.
- v. In this configuration, the chip typically shows about 84dB gain. Therefore, one should typically see -4dBm at the output of the TRF2443. However, transformers T5 and T7 at the RX baseband outputs transform 800-ohms to 50-ohms resulting in a 12dB loss factor. There is an additional 1-dB of losses in the path. Therefore, -4dBm at the output of the TRF2443 will be -17dBm at the 50-ohm input of the spectrum analyzer. Gain is calculated as Power at the spectrum analyzer + 13dB - Pin.

2. SAW path enabled
 - i. Configure EVM with a cable connecting J30 (IFOUT) to J31 (IFIN). Insert a SAW filter or a 10dB pad if desired (see [Section 1.5](#)).
 - ii. Program GUI as shown in [Figure 23](#).
 - iii. Toggle the T/Rx Cal Enable button to lock the synthesizers.



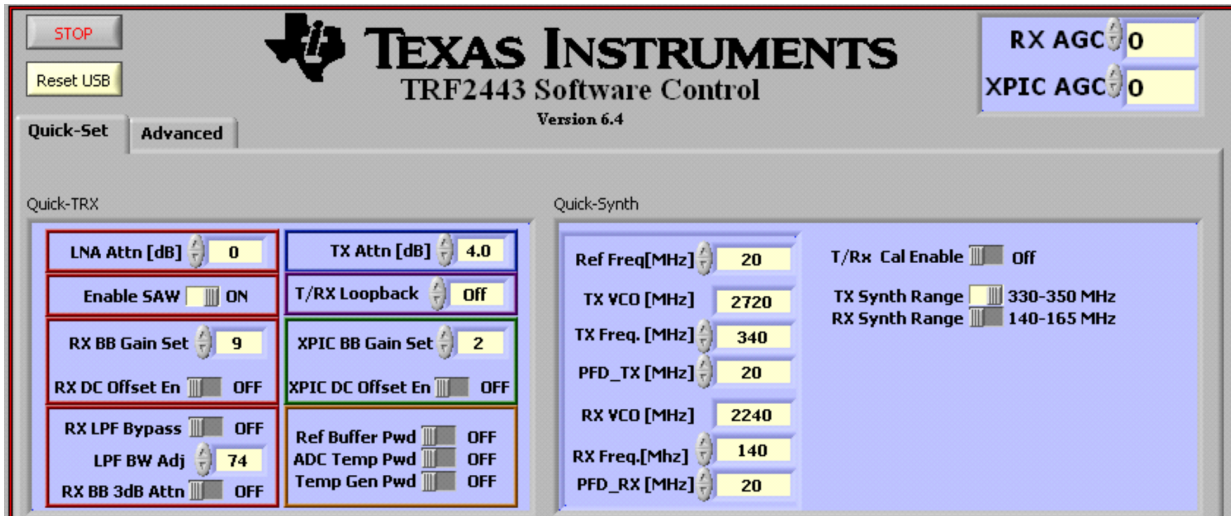
C014

Figure 23. Receiver SAW Enabled GUI Settings

- iv. Apply CW signal to J7(RXIN) port at 140.1MHz, -90dBm.
- v. Measure output on spectrum analyzer at J15(RXBBI) or J24(RXBBQ) at 100kHz.
- vi. In this configuration, the chip typically shows about 86dB gain. Therefore, one should typically see -4dBm at the output of the TRF2443. However, transformers T5 and T7 at the RX baseband outputs transform 800- Ω to 50- Ω resulting in a 12dB loss factor. There is an additional 1-dB of losses in the path. Therefore, -4dBm at the output of the TRF2443 will be -17dBm at the 50- Ω input of the spectrum analyzer. Gain is calculated as Power at the spectrum analyzer + 13dB - Pin.

3.3 XPICOUT Amplifier

- a. GAIN
 - i. Program GUI as shown in [Figure 24](#).
 - ii. Toggle the T/Rx Cal Enable button to lock the synthesizers.



C015

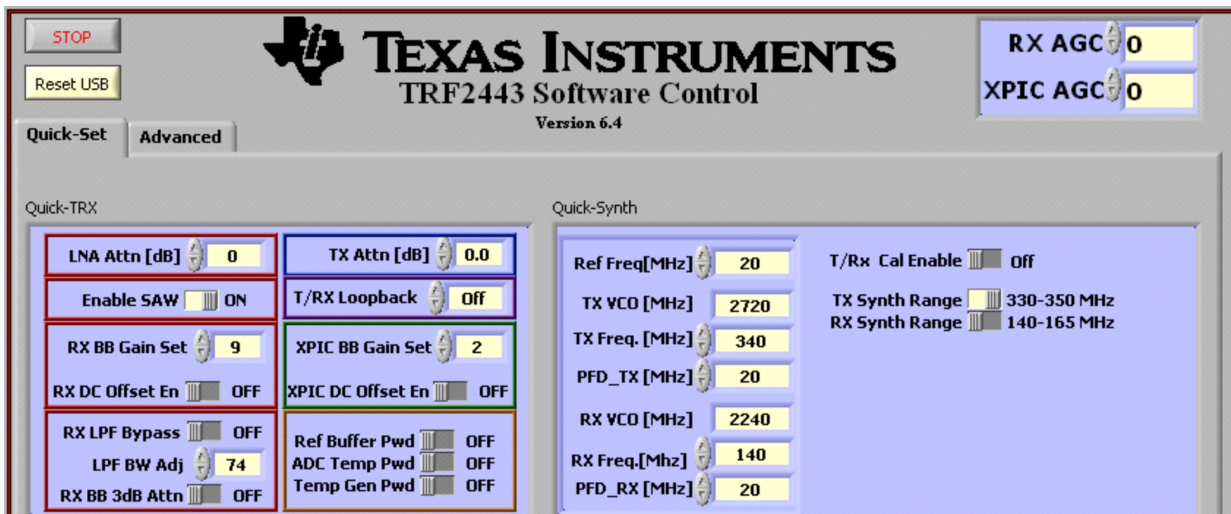
Figure 24. Receiver XPICOUT GUI Settings

- iii. Apply CW signal to J7 (RXIN) port at 140MHz, -32dBm.
- iv. Measure output on spectrum analyzer at J15 (RXBBI) or J24 (RXBBQ) at 100kHz.
- v. Adjust RX AGC voltage until -17dBm is measured at spectrum analyzer (corresponds to -4dBm at TRF2443 output).
- vi. Once this is achieved measure J33 (XPICOUT) port with a spectrum analyzer. Power out should be between -10dBm and -14dBm.

3.4 Transmitter

a. GAIN

- i. Program GUI as shown in Figure 25.
- ii. Toggle the T/Rx Cal Enable button to lock the synthesizers.



C016

Figure 25. TX Max Gain GUI Settings

- iii. Using a DAC or Arbitrary Waveform generator to create IQ baseband signals, apply IQ signals to J23 (TXBBQN), J20 (TXBBQP), J17 (TXBBIN), J12 (TXBBIP). Set instrument to 50-Ω output impedance. Each of the four IQ signals should be 1MHz, -16dBm (corresponding to -13dBm differentially on 100-Ω differentially, or, -23dBVrms-diff.)
- iv. Measure output on spectrum analyzer at J6 (TXOUT) at 341MHz. The chip typically shows 4dBm

output power.

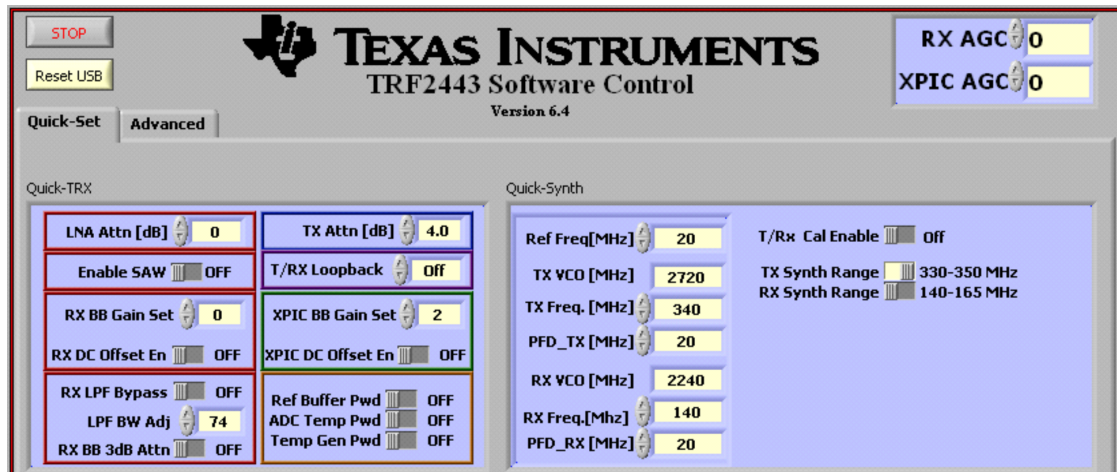
b. GAIN RANGE

- i. Change the TX ATTN [dB] setting in the GUI to determine that the output power is dropping approximately 1.0 every 2nd step.

3.5 EEPROM

- a. The purpose of this section is to Readback EEPROM content and verify EEPROM contains the stored trim values to optimize TX Carrier leakage. See TRF2443 EEPROM User's Guide for detailed explanation of the EEPROM within the TRF2443 (SLWU064)].

- i. Program GUI as shown in Figure 26.



C017

Figure 26. GUI Settings for TX Carrier Leakage

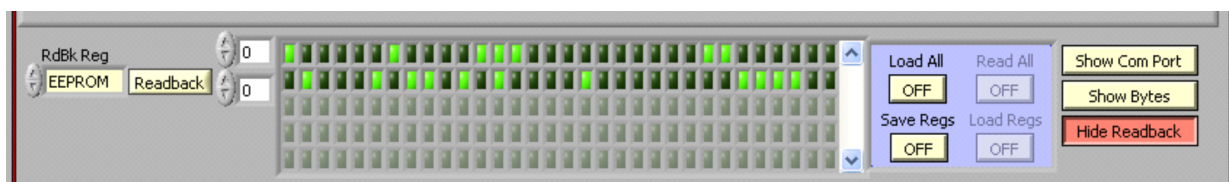
- ii. At bottom of GUI on Quick-set page, click on Show Readback Button as shown in Figure 27.



C018

Figure 27. GUI Show Readback

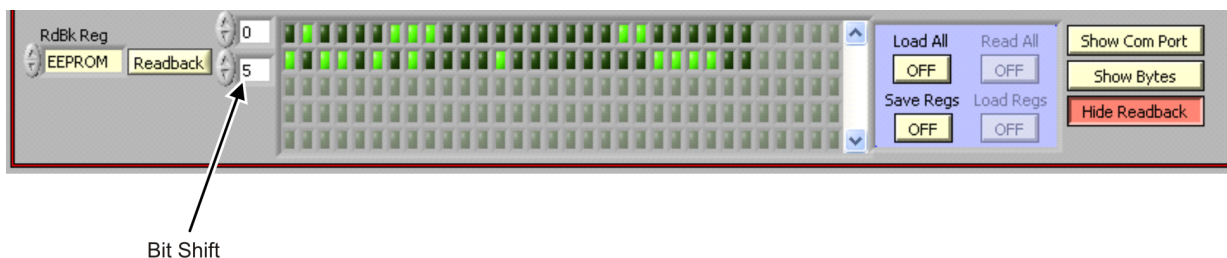
- iii. Set the RdBk Reg field to EEPROM and click the Readback Button.
- iv. The contents of EEPROM register 1 and 2 will be shown as is evident by the first five address bits (LSB) to the left as shown in Figure 28.



C019

Figure 28. GUI Select EEPROM Readback

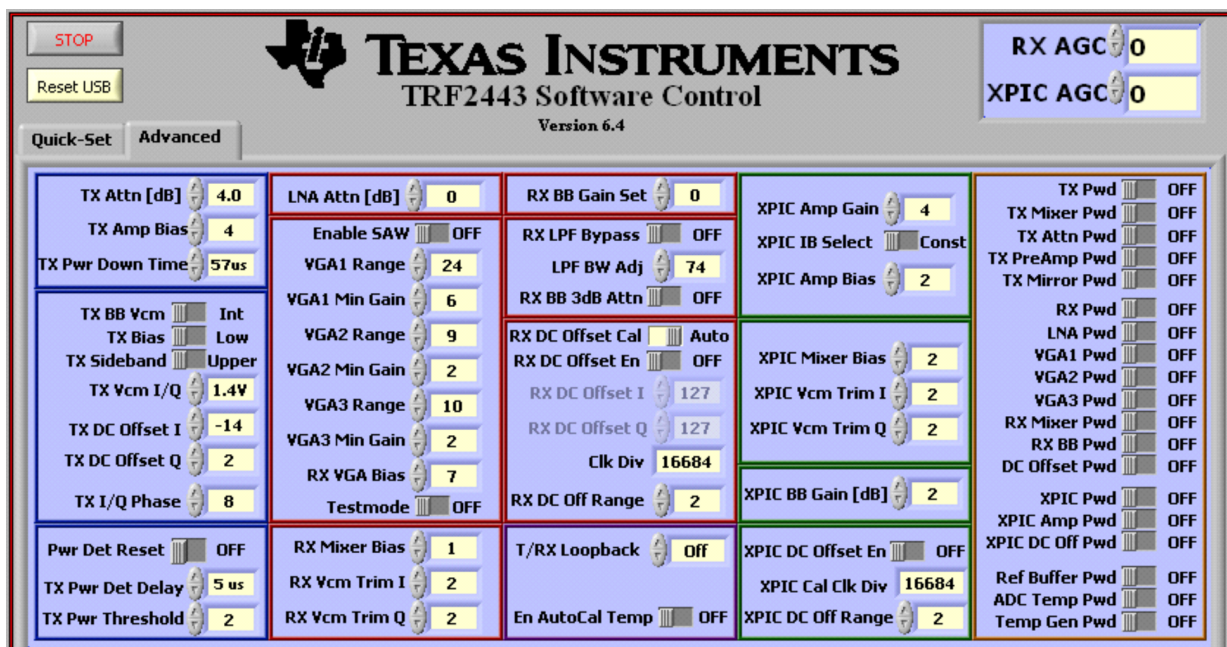
- v. The data from REG 1<10,5> is Q-trim data and from REG2<10,5> is the I-trim data. One can scroll to bit 5 by using the bottom scroll dialog box as shown in Figure 29 below.



C023

Figure 29. Read I/Q Carrier Leakage Trim Values B<10,5>

- vi. Record the decimal equivalent of REG 1<10,5> as the Q-trim data and the decimal equivalent of REG2<10,5> as the I-trim data (in this example I=45 and Q=2).
- vii. The two decimal trim values obtained above must be translated. If the decimal value is between 0 and 31, no translation is necessary and the decimal value is the value needed for the subsequent operation. However, if the decimal value is between 32 and 63, translate the value by 31 - Decimal Trim Value (ie. in this example, I=-14 and Q=2).
- viii. Click the Advanced tab at the top of the GUI. The second subsection of the first column contains two fields called TX DC OFFSET I and TX DC OFFSET Q. Set these two fields to the corresponding values that were translated in the previous step. Figure 30 shows a value of -14 for the I-trim value and 2 for the Q-trim value. Determine that the data has been written to the device by clicking the mouse in some other field other than these two fields.



C020

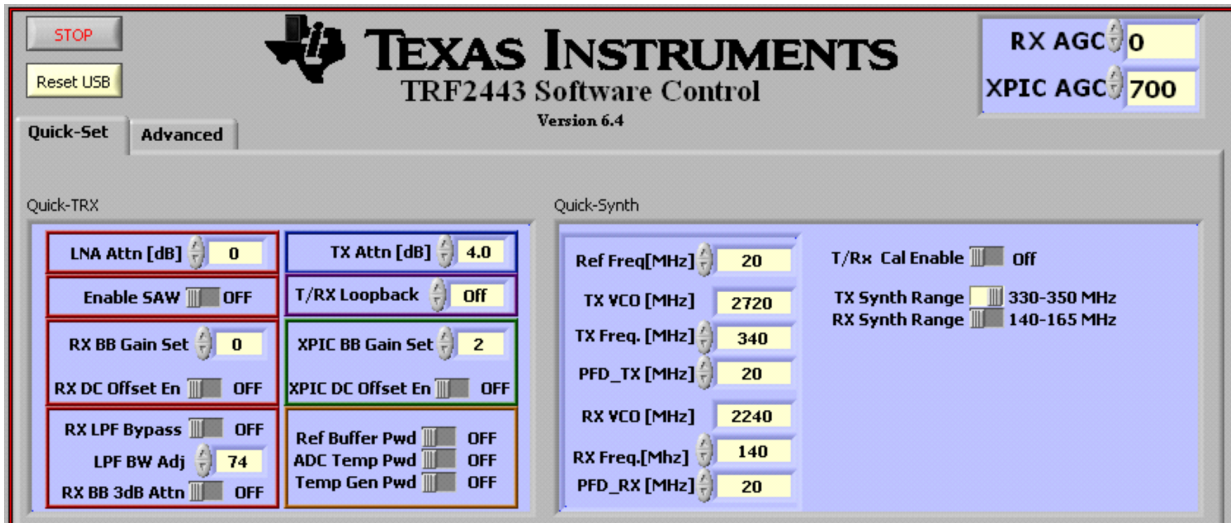
Figure 30. TX Carrier Leakage Trim

- ix. With the input signal setup as in 4.a.iii, measure the carrier leakage at SMA connector J6 (TXOUT). The typical value should be lower than -40dBm.

3.6 XPIC RECEIVER

a. GAIN Max

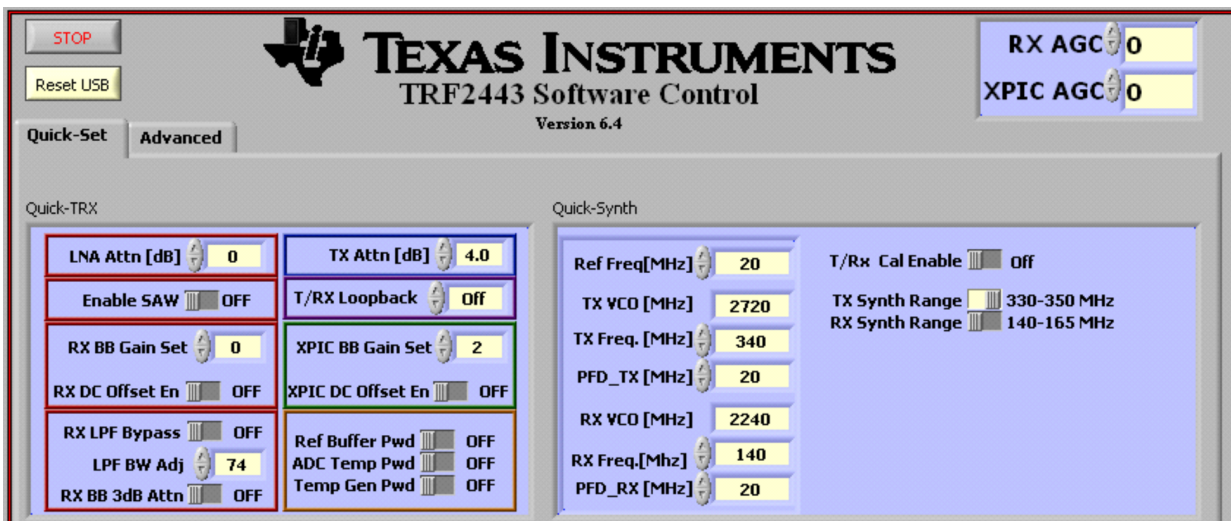
- i. Program GUI as shown in Figure 31.
- ii. Toggle the T/Rx Cal Enable button to lock the synthesizers.



C021

Figure 31. XPIC Receiver Max Gain GUI

- iii. Apply CW signal to J32 (XPICIN) of 140.1 MHz, -32dBm.
 - iv. Measure output at 100kHz at J16 (XPICI) or J25 (XPICQ) on a spectrum analyzer.
 - v. Calculate Gain = (Pout at spectrum analyzer + 13) - Pin. Typical gain value should be greater than 25dB.
- b. MIN GAIN
- i. Change XPIC AGC voltage from 700mV to 0mV as shown in [Figure 32](#).



C022

Figure 32. XPIC Receiver Min Gain GUI

- ii. Adjust Pin until -17dBm is measured on output spectrum analyzer.
- iii. Calculate Gain = (Pout at spectrum analyzer +13) - Pin. Typical value should be around 4dB.

4 Physical Description

4.1 EVM Top Layer Drawing

ASSEMBLY TOP
COMPONENT SIDE (S01)
TRF2443 REV C

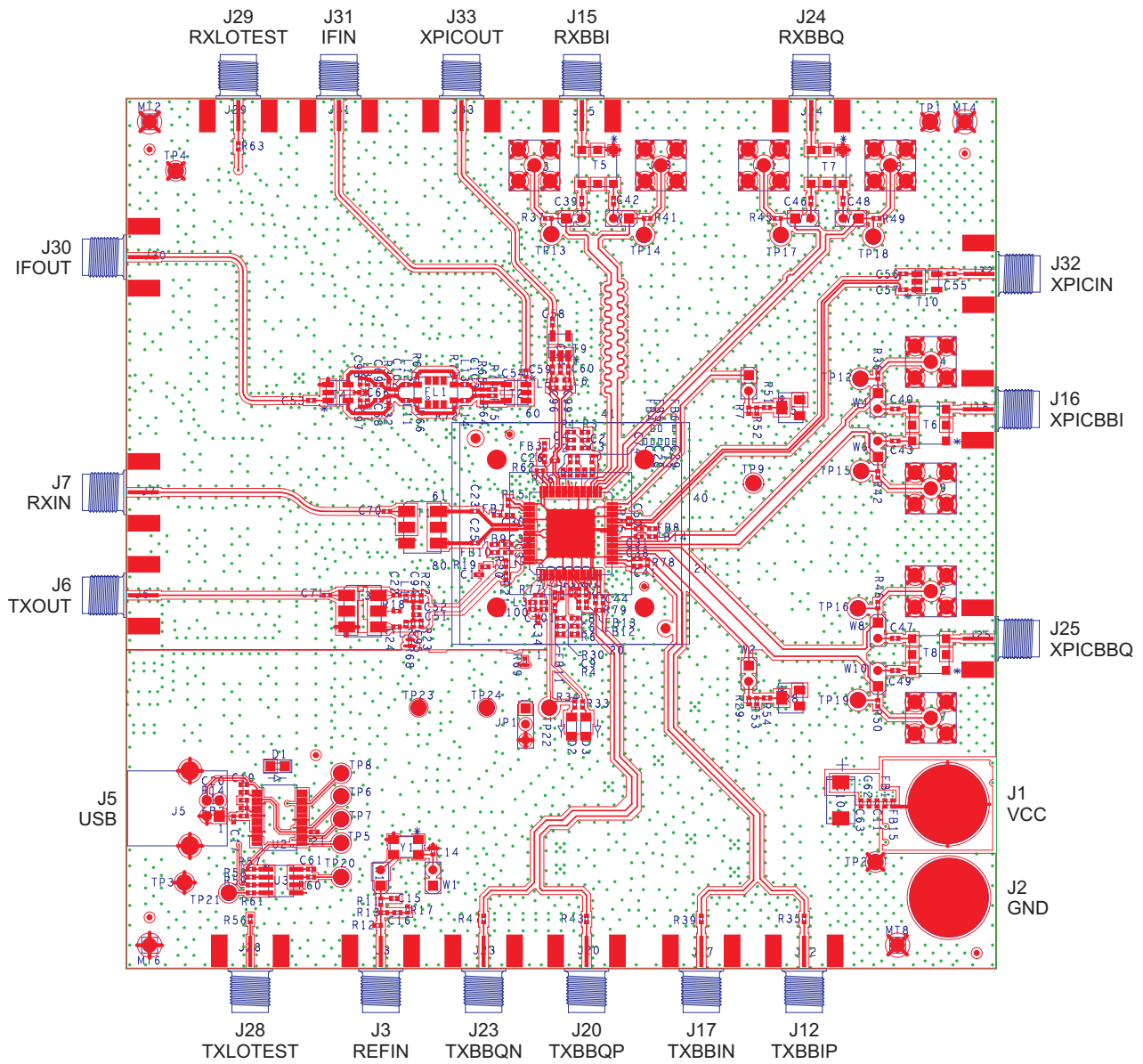


Figure 33. TRF2443 EVM Top Layer

4.2 Bill of Materials

Table 1. Bill of Materials

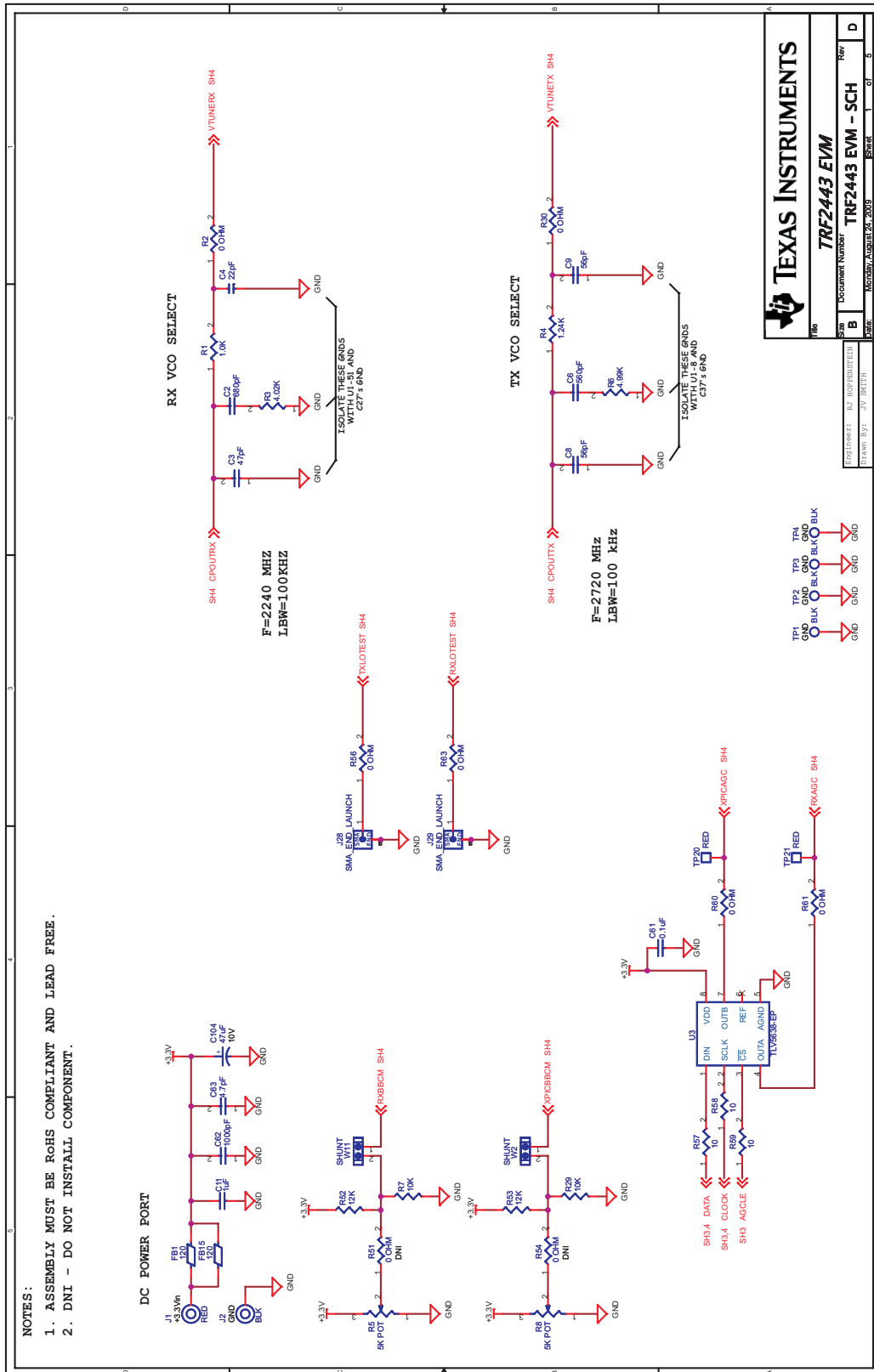
Item No.	QTY	Part Reference	Value	PCB Footprint	Mfr_Name	Mfr_Part_Number	Note
1	17	C1 C14 C18 C21 C29 C33 C36 C51 C52 C61 C64 C65 C66 C67 C72 C73 C74	0.1µF	0402	PANASONIC	ECJ-0EB1C104K	
2	1	C2	680pF	0402	MURATA	GRM1555C1H681JA01D	
3	1	C3	47pF	0402	MURATA	GRM1555C1H470JZ01D	
4	1	C4	22pF	0402	MURATA	GRM1555C1H220JZ01D	
5	1	C6	560pF	0402	MURATA	GRM1555C1H561JA01D	
6	2	C8 C9	56pF	0402	MURATA	GRM1555C1H560JD01D	
7	5	C11 C38 C41 C44 C45	1µF	0402	PANASONIC	ECJ-0EB1A105M	
8	9	C15 C26 C30 C31 C32 C34 C50 C62 C75	1000pF	0402	MURATA	GRM1555C1H102JA01D	
9	1	C17	0.01µF	0402	PANASONIC	ECJ-0EB1E103K	
10	2	C19 C20	47pF	0402	PANASONIC	ECJ-0EC1H470J	
11	3	C22 C24 C71	100pF	0402	MURATA	GRM1555C1H101JZ01D	
12	13	C23 C25 C53 C54 C55 C56 C57 C58 C59 C60 C68 C69 C70	220pF	0402	MURATA	GRM1555C1H221JA01D	
13	5	C27 C28 C35 C37 C63	4.7pF	0402	MURATA	GRM1555C1H4R7CZ01D	
14	8	C39 C40 C42 C43 C46 C47 C48 C49	2.2µF	0402	KEMET	C0402C225M9PAC	
15	0	C94 C95	4.7pF	0402	MURATA	GRM1555C1H4R7CZ01D_	DNI
16	4	C96 C97 C98 C99	15pF	0402	PANASONIC	ECJ-0EC1H150J	
17	0	C100 C101	470pF	IND_0402	MURATA	GRM155R71H471KA01D_	DNI
18	2	C102 C103	150	0402	PANASONIC	ERJ-2RKF1500X_DNI	DNI
19	1	C104	47µF	TANT_D	NIC COMPONENTS CORPS	NTC-T476K10TRD	
20	1	D1	BLUE	LED_0805	PANASONIC	LNJ906W5BUX	
21	2	D2 D3	GREEN	LED_1206	LITE-ON	LTST-C150KGKT	
22	15	FB1 FB2 FB3 FB4 FB5 FB6 FB7 FB8 FB9 FB10 FB11 FB12 FB13 FB14 FB15	120	0402	MURATA	BLM15AG121SNIB	
23	0	FL1	140MHz	SM_FILTER_197X275_10	TAI-SAW TECHNOLOGY	TB0364A_DNI	DNI
24	1	J1	RED	JACK_THVT_BANANA_500DIA	ALLIED ELECTRONICS	ST-351A	
25	1	J2	BLK	JACK_THVT_BANANA_500DIA	ALLIED ELECTRONICS	ST-351B	
26	17	J3 J6 J7 J12 J15 J16 J17 J20 J23 J24 J25 J28 J29 J30 J31 J32 J33	SMA_END_LAUNCH	SMA_ALT_2	Johnson Components	142-0701-851	
27	1	J5	USB_B_S_F_B_TH	CON_THRT_USB_B_F	SAMTEC	USB-B-S-F-B-TH	
28	8	J13 J14 J18 J19 J21 J22 J26 J27	SMA_THVT	SMA_THVT_320X320	Johnson Components	142-0701-231	
29	1	JP1	JUMPER_1X3_100	HDR_THVT_1x3_100_M	SAMTEC	TSW-103-07-L-S	(SHUNT 2-3)
30	0	L1 L2	560nH	IND_0402	COILCRAFT	0402AF-561XJLB_DNI	DNI
31	2	L3 L4	68nH	IND_0402	COILCRAFT	0402CS-68NXJLU	
32	4	L5 L6 L7 L8	82nH	ind_0402	COILCRAFT	0402CS-82NXJLW	
33	0	L11 L12	36	ind_0402	PANASONIC	ERJ-2RKF36R0X_DNI	DNI
34	0	L13 L14	0	ind_0402	PANASONIC	ERJ-2GE0R00X_DNI	DNI
35	2	L15 L16	39nH	0402	COILCRAFT	0402CS-39NXGL	
36	4	MT2 MT4 MT6 MT8	STANDOFF	mfg125_plated	KEYSTONE	3480	
37	1	R1	1.0K	0402	PANASONIC	ERJ-2RKF1001X	

Table 1. Bill of Materials (continued)

Item No.	QTY	Part Reference	Value	PCB Footprint	Mfr_Name	Mfr_Part_Number	Note
38	29	R2 R11 R19 R30 R31 R32 R35 R36 R37 R39 R41 R42 R43 R45 R46 R47 R49 R50 R56 R60 R61 R63 R64 R65 R67 R72 R73 R74 R75	0	0402	PANASONIC	ERJ-2GE0R00X	
39	1	R3	4.02K	0402	PANASONIC	ERJ-2RKF4021X	
40	1	R4	1.24K	0402	PANASONIC	ERJ-2RKF1241X	
41	2	R5 R8	5K POT	VAR_RES_SMVT_3214W	BOURNS	3214W-1-502E	
42	1	R6	4.99K	0402	PANASONIC	ERJ-2RKF4991X	
43	2	R7 R29	10K	0402	PANASONIC	ERJ-2GEJ103X	
44	0	R12 R15 R16	49.9	0402	PANASONIC	ERJ-2RKF49R9X_DNI	DNI
45	0	R51 R54	0	0402	PANASONIC	ERJ-2GE0R00X_DNI	DNI
46	1	R14	15K	0402	PANASONIC	ERJ-2GEJ153X	
47	1	R18	49.9	0402	PANASONIC	ERJ-2RKF49R9X	
48	0	R22 R23	100	0402	PANASONIC	ERJ-2RKF1000X_DNI	DNI
49	2	R33 R34	1K	0402	PANASONIC	ERJ-2GEJ102X	
50	2	R52 R53	12K	0402	PANASONIC	ERJ-2GEJ123X	
51	0	R55 R62	75	0402	PANASONIC	ERJ-2RKF75R0X_DNI	DNI
52	3	R57 R58 R59	10	0402	PANASONIC	ERJ-2RKF10R0X	
53	1	R66	0	0402	PANASONIC	ERJ-EGE0R00X	
54	2	R68 R69	0	0805	PANASONIC	ERJ-2GEY0R00V	
55	1	R77	590	0402	PANASONIC	ERJ-2RKF5900X	
56	2	R78 R79	100	0402	PANASONIC	ERJ-2RKF1000X	
57	1	T1	ADT1-1	TRANS_SMVT_CD542_6	MINI-CIRCUITS	ADT1-1	
58	2	T2 T4	TC1-1	XFMR_5_150X150_50	MINI-CIRCUITS	TC1-1	
59	1	T3	ADT4-1T	TRANS_SMVT_CD542_6	MINI-CIRCUITS	ADT4-1T	
60	4	T5 T6 T7 T8	TTWB-16-BL	TRANS_SMVT_TTWB_6	CoilCraft	TTWB-16-BL	
61	2	T9 T10	TC1.5-52T	XFMR_5_150X150_50	MINI-CIRCUITS	TC1.5-52T+	
62	4	TP1 TP2 TP3 TP4	BLK	TP_THVT_100_RND	KEYSTONE	5001	
63	18	TP5 TP6 TP7 TP8 TP9 TP12 TP13 TP14 TP15 TP16 TP17 TP18 TP19 TP20 TP21 TP22 TP23 TP24	RED	TP_THVT_100_RND	KEYSTONE	5000	
64	1	U1	TRF2443 SOCKET QFP	QFP_80_OZTEK_0P50MM_CUSTOM	Texas Instruments	TRF2443	
65	1	U2	FT245RL	ssop_28_413x220_26	FTDI Chip	FT245RL	
66	1	U3	TLV5638-EP	SOIC_8_197X157_50	TI	TLV5638QDREP	
67	12	W1 W2 W3 W4 W5 W6 W7 W8 W9 W10 W11 W12	JUMPER - 2 PIN	HDR_THVT_1x2_100_M	SAMTEC	HTSW-102-07-L-S	
68	1	Y1	20MHz	OSC_4_SM_205X134	FOX ELECTRONICS	FOX924B-20	
69	4	FOR THE STANDOFFS	SCREW PANHEAD 4-40 3/8		Building Fasteners	PMSSS 440 0038 PH	OR EQUIVALENT
70	12	FOR ITEM 67	SHUNT		KELTRON	MJ-5.97-G OR EQUIVALENT	SHUNT FOR JUMPER
71	1	FOR ITEM 29	SHUNT2-3		KELTRON	MJ-5.97-G OR EQUIVALENT	SEE NOTES
72	1	TRF2443 REV D BARE BOARDS			TI	TRF2443 REV D	

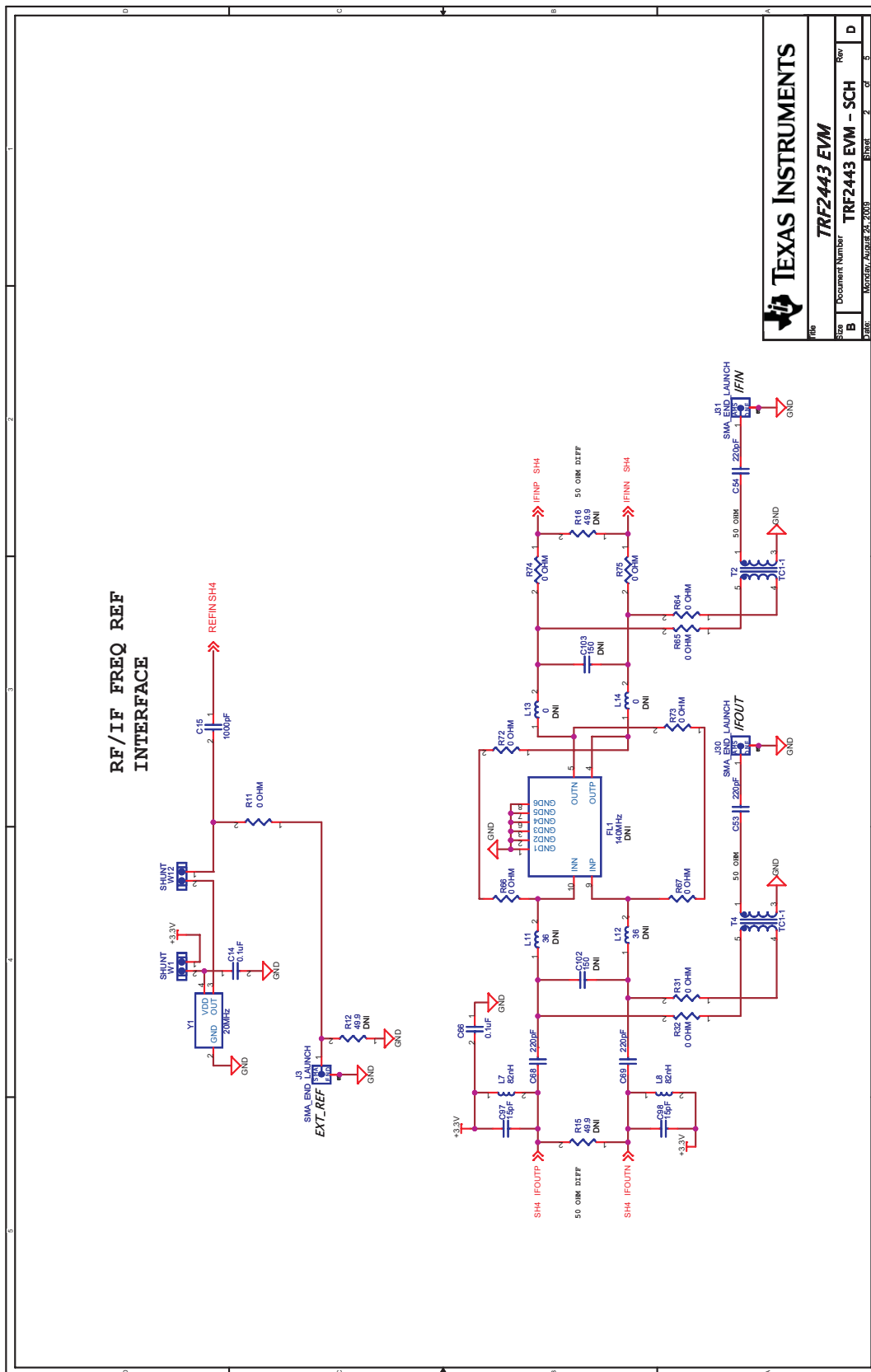
Notes: 1. USE WATER SOLUBABLE FLUX DURING BOARD ASSEMBLY.
2. DNI = DO NOT INSTALL COMPONENT.
3. INSTALL ITEM 71 JP1 SHUNT 2-3
4. RoHS COMPLIANT AND LEAD FREE ASSEMBLY.

4.3 Schematics



S001

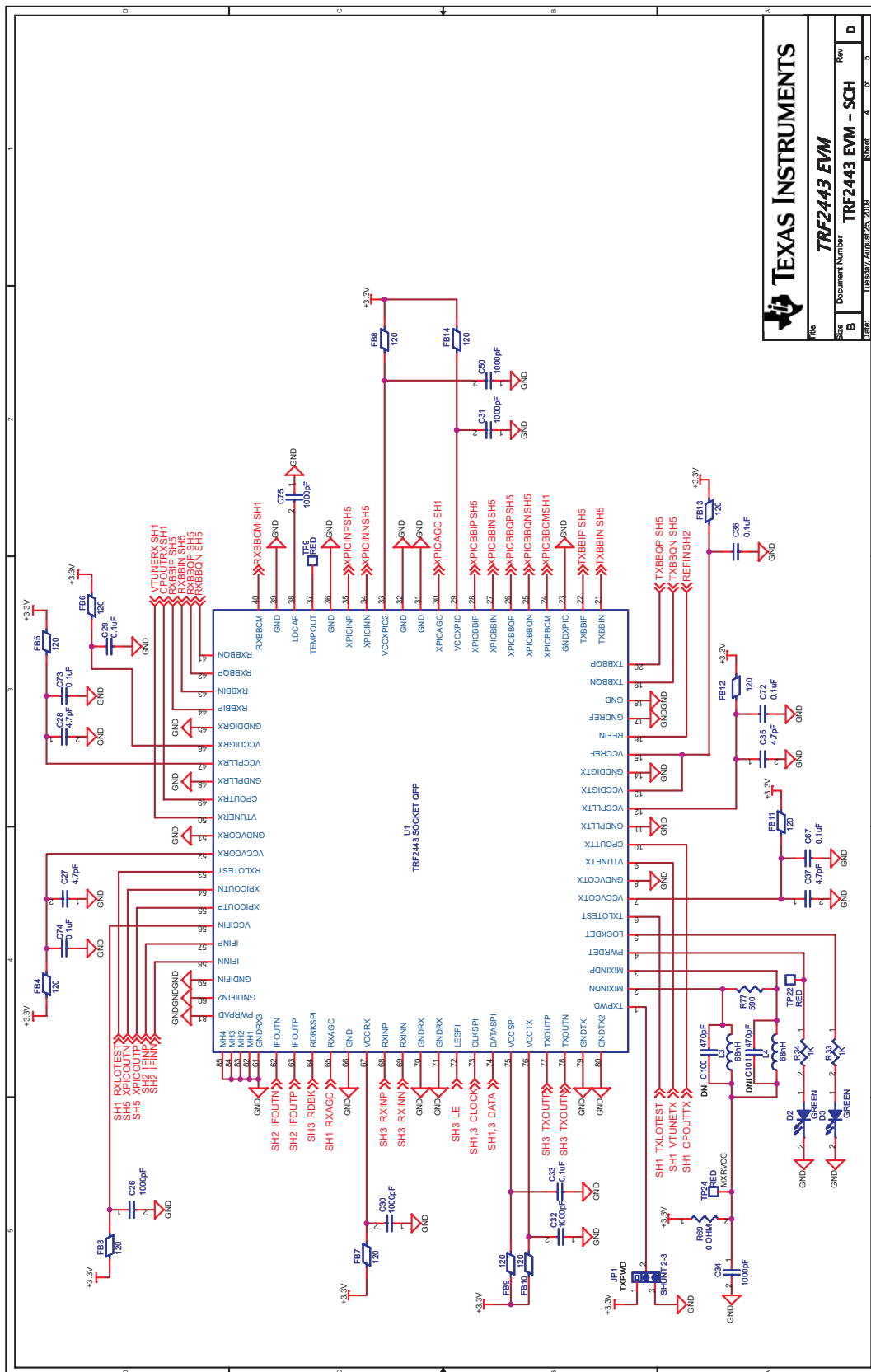
Figure 34. Schematic (1 of 5)



TRF2443 EVM				
Doc#	Document Number	Rev	of	D
B	TRF2443 EVM - SCH		2	5
DATE	MODIFIED	AUTHOR	25	2008

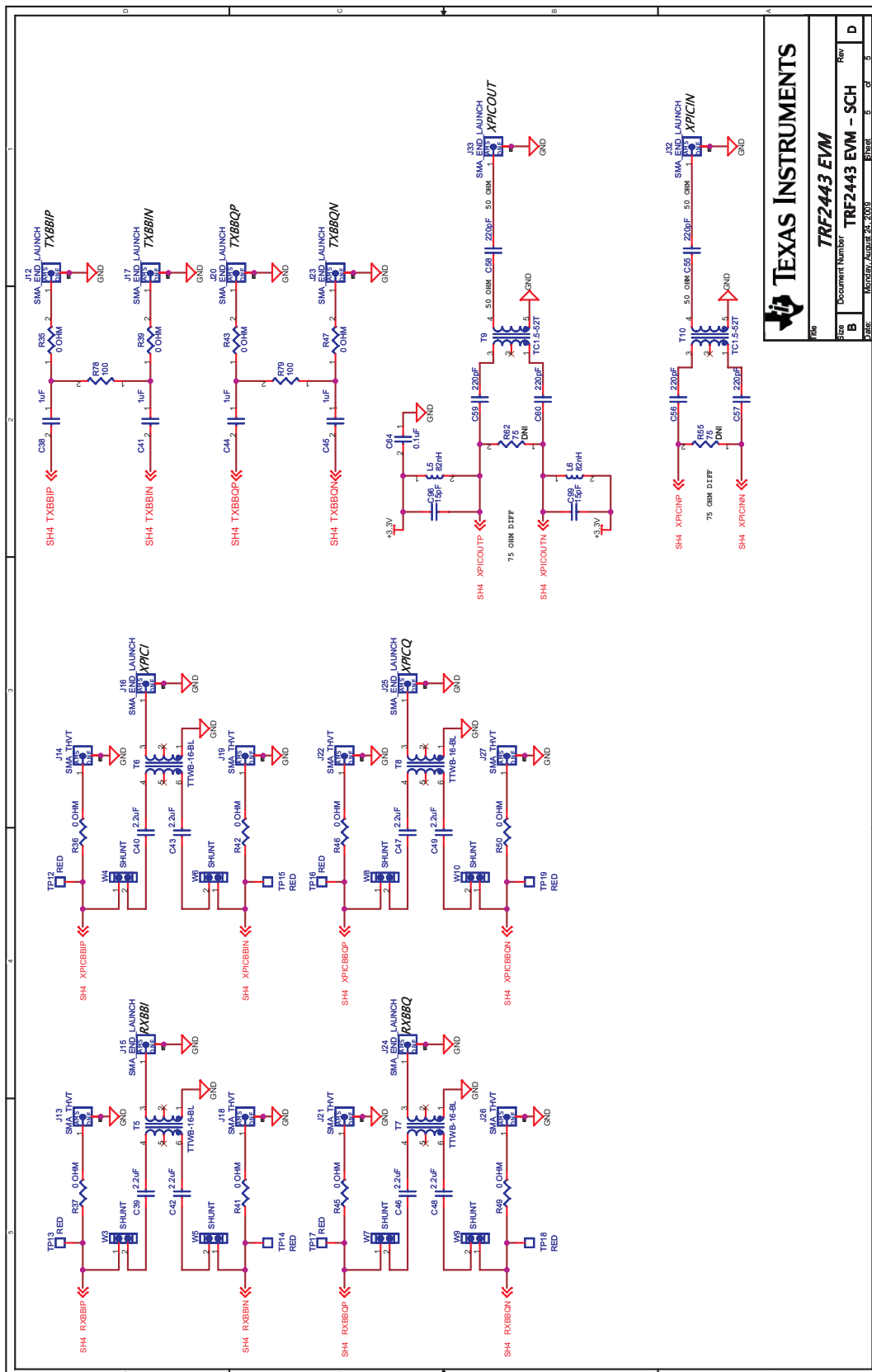
S002

Figure 35. Schematic (2 of 5)



S004

Figure 37. Schematic (4 of 5)



S005

Figure 38. Schematic (5 of 5)

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