Using SPI synchronous communication with data converters—interfacing the MSP430F149 and TLV5616

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Introduction

Sophisticated analog waveform generation is often a requirement in modern microcontroller unit (MCU) applications. A few examples of these applications include DTMF, low-baud-rate modems, and stimulation of sensors. Most MCUs integrate some form of basic analog-to-digital converter (ADC), but few include a true digital-to-analog converter (DAC). Techniques such as pulse-width modulation (PWM) or resistor ladders can be used to generate simple analog signals, but such solutions can be resource-intensive and require complicated external filtering to smooth the final waveform. Using SPI synchronous communications, an MCU can easily interface to an external DAC that exactly matches the requirements of the application. This article describes how to interface the MSP430F149 USART serial port to the TLV5616 12-bit DAC. See Figure 1.

Serial interface

The MSP430F149 includes two identical USART modules (USART0 and USART1). The USART supports the transfer of serial data from the MSP430 to another device in either a synchronous (SPI) or asynchronous (UART) mode as a master or slave. User firmware configures the USART for the desired mode of operation as described under "Configuring USART0," which follows.

The physical interface between the MSP430F149 and TLV5616 is glueless, using three or four signal pins to communicate. The TLV5616 is a synchronous slave device requiring an external clock and data signals. USART0 on the MSP430F149 is configured for SPI operation in master mode. Serial data is output from the MSP430F149 on the slave-in/master-out (SIMO) pin and is synchronized to a clock signal generated on the USART clock (UCLK) pin. The TLV5616 receives data and clock on data-in (DIN) and serial clock (SCLK), respectively. There are two additional signals associated with the MSP430 USART in SPI mode—slave-out/master-in (SOMI) and slave-transmit-enable (STE). SOMI and STE are used with bi-directional SPI communications and are not required to communicate with the TLV5616. The TLV5616 is a slave only when receiving data and clock. No data is returned to the master. A frame-sync (FS) signal is sent to the TLV5616 with any MSP430 general-purpose port pin configured as an output (P3.0 is used in this example). A chip select ($\overline{CS}$) is also available on the TLV5616 that can place all other signal pins on the device in a high-impedance state when brought high. $\overline{CS}$ can be used in applications where several devices are present on the same bus. Using $\overline{CS}$, the MCU can directly enable and disable individual devices. In this article, it is assumed that $\overline{CS}$ is tied to ground, keeping the TLV5616 permanently enabled.

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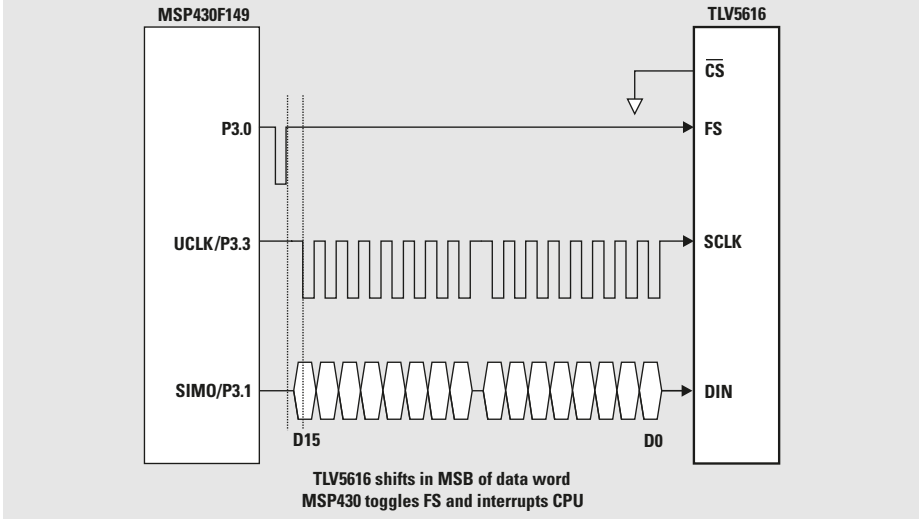
Figure 1. MSP430F149-to-TLV5616 interface



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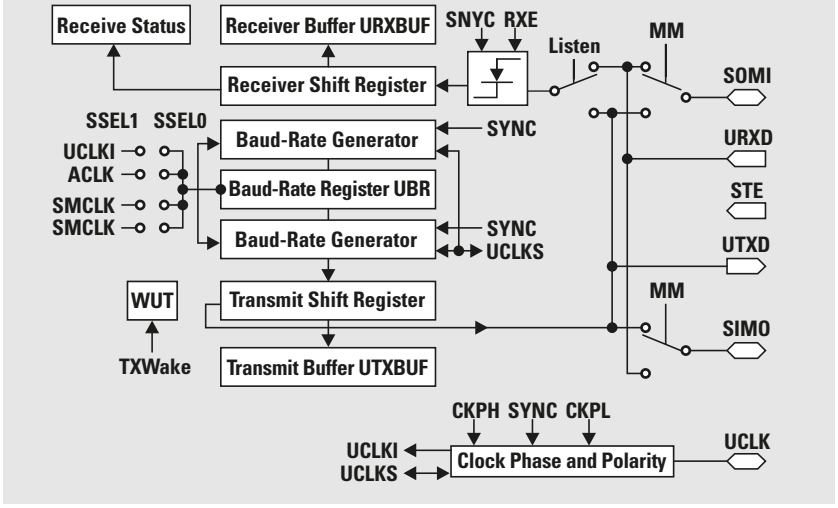
Configuring USART0

The USART is a completely independent asynchronous MSP430 module. The USART module incorporates a 16-bit baud-rate generator, 8-bit modulator, control and interrupt logic, and shift register/buffers for both transmit and receive paths. A simplified diagram of the MSP430 USART module is shown in Figure 2.

The USART first must be configured with control registers. MSP430 control registers are always collected in the lowest 256 bytes of the 64-kB memory map. The individual device data sheet will detail all peripherals and registers contained in a specific device. Three special-function, four port 3 (P3), and eight dedicated USART0-configuration registers are associated with USART0. See Table 1.

Figure 2. MSP430 USART module



The three special-function registers associated with USART0 are the interrupt enable register 1 (IE1), the interrupt flag register 1 (IFG1), and the module enable register 1 (ME1). The bit details of these registers are seen in Figure 3.

If USART0 interrupt capability is required, individual interrupt vectors are available for the transmit and receive paths and are enabled in IE1 using control bit UTXIE0 and URXIE0, respectively. As with any interrupt in the MSP430, the general interrupt enable (GIE) must also be set in the status register (SR). Interrupt capability is not used in the example given in this article, and these bits are left in their default (reset) condition. The interrupt flags for receive and transmit paths UTXIFG0 and URXIFG0 are located in IFG1. Setting USPIIE0 in ME1 enables the USART0 SPI function. This is important because USPIIE0 enables or disables all USART0 SPI functionality regardless of other bit configurations.

Figure 3. MSP430F149 special-function registers used with USART0

	7							0
IE1 00h	UTXIE0	URXIE0	ACCVIE	NMI	Unused	Unused	OFIE	WDTIE
IFG1 02h	UTXIFG0	URXIFG0	Unused	NMIIFG	Unused	Unused	OFIFG	WDTIFG
ME1 04h	UTXE0	UTXE0 USPIIE0	Unused	Unused	Unused	Unused	Unused	Unused

Table 1. MSP430F149 registers associated with USART0

REGISTER	SHORT FORM	REGISTER TYPE	ADDRESS
Interrupt enable 1	IE1	Read/write	000h
Interrupt flag 1	IFG1	Read/write	002h
Module enable 1	ME1	Read/write	004h
P3 input	P3IN	Read only	018h
P3 output	P3OUT	Read/write	019h
P3 direction	P3DIR	Read/write	01Ah
P3 select	P3SEL	Read/write	01Bh
USART control	UCTL0	Read/write	070h
Transmit control	UTCTL0	Read/write	071h
Receive control	URCTL0	Read/write	072h
Modulation control	UMCTL0	Read/write	073h
Baud rate 0	UBR0	Read/write	074h
Baud rate 1	UBR1	Read/write	075h
Receive buffer	URXBUF0	Read/write	076h
Transmit buffer	UTXBUF0	Read	077h

USART0 peripheral signals on the MSP430F149 are multiplexed on I/O port 3 (P3). It is important that the user carefully review the device-specific MSP430 data sheet to identify exactly on which port and pin a peripheral module is multiplexed. While the peripheral modules are identical on all MSP430 devices, the port pins on which the module is multiplexed may be different from device to device. On the MSP430F149, P3 pins can either be general-purpose I/O or selected as USART0 functions. There are six registers associated with port 3. In the example, user firmware selects the SIMO function multiplexed on P3.1 and UCLK on P3.3 by setting bits 2 and 4 in the P3 selection register (P3SEL). All PxSEL bits default to reset, general-purpose I/O. User firmware additionally sets the appropriate direction of USART0 pins required in the application using the P3 direction register (P3DIR). As UCLK and SIMO are both outputs from the MSP430, P3.1 and P3.4 (bits 2 and 5) are set in P3DIR. All PxDIR pins default to reset (input direction). The USART hardware will directly drive UCLK and SIMO during serial transfer. P3.0, which is used to control FS, is also set to the output direction by using P3DIR. The set/reset state of P3.0 is controlled with firmware by using the P3 output register (P3OUT).

In this example, the USART is configured as a transmit-only master in a synchronous mode using the MSP430 sub master clock (SMCLK) without interrupt capability. Only

the USART0 control register (UCTL0) and transmit control register (UTCTL0) have significance in this mode. Bit details of these two registers are shown in Figure 4.

UCTL0 configures the basic operation of USART0.

- SWRST = 1: The USART state machine is at reset, disabled.

  SWRST = 0: The USART state machine is ready.
- MM = 1: Master mode selected.

  MM = 0: Slave mode selected.
- SYNC = 1: Synchronous mode selected.

  SYNC = 0: Asynchronous mode selected.
- Listen = 1: Transmitted data is fed back to the receiver.

  Listen = 0: Receive data is received normally.
- CHAR = 1: 8 bits of data are transferred.

  CHAR = 0: 7 bits of data are transferred.

Setting the bits CHAR, SYNC, and MM in UCTL0 configures USART0 to transmit 8-bit characters in a synchronous master mode.

UTCTL0 configures the transmit operation of USART0. In the SPI master mode, the following are valid.

- TXEPT = 1: Flag is set when the transmitter shift register and UTXBUF are empty.

  TXEPT = 0: Flag is reset when data is written to UTXBUF.
- STC = 1: Four-pin mode, STE active.

  STC = 0: Three-pin mode, STE inactive.
- CKPL = 0: The inactive level is low; data is output with the rising edge of UCLK; input data is latched with the falling edge of UCLK.

  CKPL = 1: The inactive level is high; data is output with the falling edge of UCLK; input data is latched with the rising edge of SPICLK.
- CKPH = 0: Normal UCLK clocking scheme.

  CKPH = 1: UCLK is delayed by one half cycle.

  SSEL1, SSEL1: Define the clock source for baud rate clock (see Table 1).

To communicate with the TLV5616, CKPL and CKPH are both reset. As such, the USART presents data on the SIMO line synchronized on the rising edge of UCLK. The TLV5616 latches the relevant data on the falling edge of UCLK. Source select bits SSEL1 and SSEL0 select the baud rate clock (BRCLK). SSEL1 and SSEL0 are both set in the example, selecting SMCLK.

The USART0 control registers UBR10 and UBR00 concatenated define a 16-bit divider (UBR = UBR10, UBR00) such that UCLK0 = BRCLK/UBR. The maximum baud rate that can be selected for transmission in master mode is half of the BRCLK. In slave mode, the external clock applied to UCLK determines BRCLK. Modulation control is not used for serial synchronous communication. It is recommended to keep UMCTL reset.

TLV5616 configuration

Data is sent to the TLV5616 as 16 bits. The 4 most significant bits transfer the control bits as shown in Figure 4. The 12 least significant bits contain the new DAC code. The example in this article transfers all 0s for control bits. Only the DAC code is modified; thus the DAC is always powered up with 6-ms settling time.

Figure 4. USART0 control and transmit registers

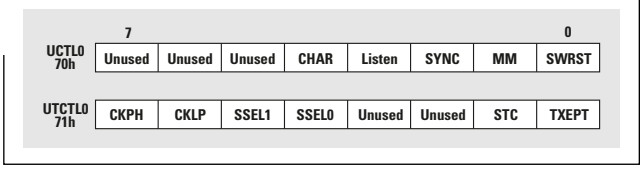
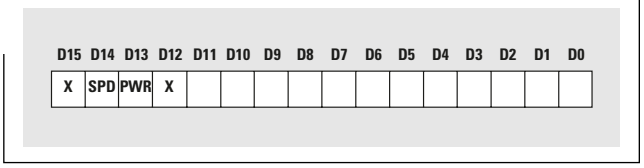


Figure 5. TLV5616 control register



- SPD = 1: 3-ms settling time

  SPD = 0: 6-ms settling time
- PWD power control 1 = Power down

  PWD power control 0 = Normal operation
- D11 ... D0 New 12-bit DAC code

USART0 operation

Once configuration is completed, using the MSP430 USART to transfer data is simple. Firmware initiates a transfer by writing a byte of data to the USART0 transmit buffer (UTXBUF0), which is automatically moved to the transmit shift register as soon as it is empty. Data is automatically shifted out at the selected baud rate. The USART will transfer data on the SIMO pin, with the most significant bit first, synchronized with UCLK. At the same time, if data is being received, it is shifted into the receive shift register; and, upon completion of receiving the selected number of bits, the received data is transferred to the USART receive buffer (URXBUF0). Receive and transmit always take place together, at opposite clock edges.

The TLV5616 requires a transfer of 16 bits of data. This can be accomplished efficiently by writing two byes back-to-back to UTXBUF0. The first byte written is loaded immediately from UTXBUF0 to the transmit shift register, making UTXBUF0 available for the second byte. The second byte can be written and will remain in UTXBUF0 until the first byte has transferred. USART0 will then automatically load the second byte to the shift register. The second byte is then transferred. Writing the two bytes back-to-back permits 16 bits to be effectively transferred in one operation. User firmware can poll the transmit-empty (TXEPT) flag in the UTXCTL0 to insure that no serial transfer takes place before data is loaded to the UTXBUF0. The TXEPT flag is set by USART hardware when both UTXBUF and the transmit shift register are empty. Writing data to UTXBUF0 clears the flag.

Description of the demonstration firmware

The demonstration firmware generates a repeating 12-bit ramp. After reset, firmware initializes the stack pointer and disables the watchdog. Port 3 and USART0 are configured, and the CPU register R4 is cleared. R4 contains the digital code 0 to 4095, which will be transferred to the

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TLV5616. The selection of R4 is random and not important. Any CPU register or RAM byte can be used to contain the digital code.

Inside the Mainloop program code, FS is toggled on P3.0. Toggling FS initiates the serial transfer to the TLV5616. The value from R4 is transferred to the TLV5616 as two bytes. As required by the TLV5616, the most significant byte is transferred first, followed immediately by the least significant byte. The two bytes are transferred to the TLV5616 by simply writing the individual bytes successively to UTXBUF0. The 12-bit value in R4 is then incremented and normalized to 0 to 4095. The transmit-empty (TXEPT) flag is polled to insure that the USART0 transfers all data from the transmit shift register and TXBUF before the firmware continues. This insures that the USART0 buffers are not overwritten with new data before the original data is shifted out. The loop repeats.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. "MSP430x1xx Family," User's Guide	slau049
2. "MSP430x13x, MSP430x14x Mixed Signal Microcontroller," Data Sheet	slas272
3. "TLV5616C, TLV5616I 2.7 V to 5.5 V Low Power 12-Bit Digital-to-Analog Converters with Power Down," Data Sheet	slas152

Related Web sites

www.dataconverter.com
www.ti.com/sc/device/tlv5616
www.ti.com/sc/msp430

MSP430F149-to-TLV5616 example program

```
#define _CPU_ 6
#include    "STD_DEF.h" ; Standard equations
;*******************************************************************************
NAME  140_5516  ; MSP-FET430P140 demonstration program to generate a
repeating 12-bit ramp sent via USART0 to a TLV5616
;
;           M. Buccini
;           Texas Instruments Inc.
;           September 2000
;*******************************************************************************

;-------------------------------------
            ORG         0F000h                  ; Program Start
;-------------------------------------
RESET       mov         #0A00h,SP               ; Initialize stackpointer
Init_Sys    mov         #WDTPW+WDTHOLD,&WDTCTL  ; Stop WDT
SetupP3     bis.b       #00Ah,&P3SEL            ; P3.1,3 SPI option select
            bic.b       #001h,&P3OUT            ; FS reset
            bis.b       #001h,&P3DIR            ; FS output direction
SetupSPI    bis.b       #040h,&ME1              ; Enable USART0 SPI
            mov.b       #CHAR+SYNC+MM,&UCTL0    ; 8-bit SPI master
            mov.b       #CKPL+SSEL1+SSEL1+STC,&UTCTL0
                                                ; SMCLK for TX, 3-pin mode
            mov.b       #02h,&UBR00             ; SMCLK/2 for baud rate
            clr.b       &UBR10                  ; SMCLK/2 for baud rate
            clr.b       &UMCTL0                 ; Clear modulation
            clr         R4                      ;
                                                ;
Mainloop    bis.b       #001h,&P3OUT            ; Pulse FS
            bic.b       #001h,&P3OUT            ;
            swpb        R4                      ; R4 = 3412
            mov.b       R4,&TXBUF0              ; High byte to SPI TXBUF
            swpb        R4                      ; R4 = 1234
            mov.b       R4,&TXBUF0              ; Low byte to SPI TXBUF
            inc         R4                      ; Increment DAC data
            and         #00FFFh,R4              ; R4 = 0 to 4095 (12 bits)
L1          bit.b       #TXEPT,&UTCTL0          ; TXBUF/shift reg. empty?
            jnc         L1                      ; 1 = empty
            jmp         Mainloop                ; Repeat
                                                ;
;-------------------------------------
            ORG         0FFFEh                  ; MSP430 RESET vector
;-------------------------------------
            DW          RESET                   ; POR, ext. Reset, Watchdog
            End
```

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