TEXAS INSTRUMENTS

Serial Presence Detect

Technical Reference

1998 Technical Documentation Services

Texas Instruments

Printed in U.S.A., January 1998

SMMU001

Book Type
Two Lines
Volume #

Book Type
Volume #

Book Type
Two Lines

Book Type

Title
Two Lines
Subtitle
Line Two

year

Title
Two Lines
Subtitle

Title
Two Lines

Title
Subtitle
Line Two

Title
Subtitle

Title

year

Serial Presence Detect Technical Reference

SMMU001
January 1998

Printed on Recycled Paper

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Contents

List of Figures

List of Tables

Serial Presence Detect Technical Reference

ABSTRACT

The serial-presence-detect (SPD) is a memory module detecting device that provides the host computer information about the memory module. The SPD definition is broken into a series of bytes describing the configuration of the memory module. The SPD describes required and/or optional features in one or more bytes. The required data describes the particular aspects of a module and are fixed in size by the SPD standard. The optional features include the manufacturers' ID, serial numbers, and other data.

1 Introduction

Memory devices are rapidly changing to meet the needs of today's technologies. Under the current parallel presence detect method, the flexibility to adapt new memory technologies to existing module form factors is not possible. Hence, the serial presence detect (SPD) method was developed. This scheme not only allows designers to implement current memory technologies, but to also implement new memory technologies without concern about existing module form factors.

The objective of this technical reference is to introduce the SPD, which, in its base form, is independent of the memory technology and module form factor. The implementation of any memory technology using SPD can be achieved as long as it has been defined in the SPD standard.

1.1 SPD Definition

The SPD data, which conforms to the current JEDEC standard, is written into a nonvolatile serial device by the DIMM manufacturer. The SPD definition is broken down into a series of bytes that describes the configuration of the memory module. Each required or optional feature of the SPD is described in one or more bytes that can consist of table look-up entries or binary data. The required data that describes particular aspects of a module is fixed in size by the SPD standard. The optional data, which is supplied by system integrators, can consist of manufacture's IDs, serial numbers, or other data. These optional features will be described in a future appendix.

Table 1 shows the general features that must be defined for an SPD to be implemented. When a specific memory technology (FPM, EDO, SDRAM,…) or feature is implemented in an SPD scheme, a corresponding appendix will be updated/added to this document.

Table 1. Serial-Presence-Detect Format

BYTE NUMBER	FUNCTION
0	Defines # of bytes written into the SPD device
1	Total # of bytes in the SPD device
2	Fundamental memory type
3–35	Defines features specific to the fundamental memory
36–61	Defines superset features
62–127	Manufacturing information
128+	User information

1.2 SPD Specifications and Device SPD Definitions

The SPD device is contained in a 2K-bit serial EEPROM located on the module. Table 2 refers to the SPD EEPROM specifications and the relevent appendix. Table 2 also references the SPD devices to the appropriate appendix containing SPD definitions.

Table 2. Serial-Presence-Detect (SPD) Definitions/Specifications

SPD DEVICE DEFINITIONS	APPENDIX
SPD for EDO/FPM Devices Definition	Appendix A
SPD for SDRAM Devices Definition	Appendix B
Manufacturer and System Integrator's SPD Format	Appendix C
EEPROM Component Specifications	Appendix D

Appendix A Serial-Presence-Detect Format for Fast-Page Mode and Extended-Data-Out DRAM Modules

This appendix describes the serial-presence-detect format for fast-page mode and extended data out DRAM modules. All features follow the JEDEC standard on the serial presence detect and will be updated when changes or new features become available. Table A–1 outlines these features; each feature is defined in section A.2.

A.1 SPD Format for FPM/EDO DRAM Modules

Table A–1. SPD Format for FPM/EDO DRAM Modules

BYTE NUMBER	FUNCTION
0	Defines number of bytes written into serial memory at module mfg.†
1	Total number of bytes of the SPD memory device‡
2	Fundamental memory type (FPM or EDO)
3	Number of row addresses on this assembly
4	Number of column addresses on this assembly
5	Number of module banks on this assembly
6	Data width of this assembly…
7	… Data width continuation
8	Voltage interface standard of this assembly
9	RAS access time of the module
10	CAS access time of the module
11	DIMM configuration type (nonparity, parity, ECC)
12	Refresh rate/type
13	DRAM width, base DRAM
14	Error-checking DRAM data width
15–31	Reserved for future offerings
32–61	Superset memory specific features (may be used in the future)
62	SPD revision designator
63	Checksum for bytes 0–62
64–71	Manufacturer’s JEDEC ID code per JEP-106E
72	Manufacturing location
73–90	Manufacturer’s part number
91–92	Revision code
93–94	Manufacturing date
95–98	Assembly serial number
99–125	Manufacturer specific data

† This is 128 bytes for FPM and EDO DRAM modules.
‡ This is typically 256 bytes.

Table A–1. SPD Format for FPM/EDO DRAM Modules (Continued)

BYTE NUMBER	FUNCTION
126–127	Vendor specific
128–135	System integrator's ID
136–150	System integrator's P/N
151–152	System integrator's D/C
153–165	System integrator's S/N
166	Checksum for bytes 128–165
167–189	Top-level system serial number
190–221	Open
222	Checksum for bytes 167–221
223–253	Open
254	Checksum for bytes 223–253
255	Checksum for bytes 0–128

A.2 SPD Bytes Defined

A.2.1 Byte 0: Number of Bytes Written Into Serial Memory by Module Manufacturer

This 8-bit field, shown in Table A–2, describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data.

Table A–2. Byte 0 Definition

NUMBER OF SPD BYTES	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

A.2.2 Byte 1: Total Number of Bytes of the SPD Memory Device

This 8-bit field, shown in Table A–3, describes the total size of the serial memory used to hold the serial-presence-detect data.

Table A–3. Byte 1 Definition

SERIAL MEMORY	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16264 Bytes	0	0	0	0	1	1	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
:	1	1	1	1	1	1	1	0
:	1	1	1	1	1	1	1	1

A.2.3 Byte 2: Fundamental Memory Type

This byte, shown in Table A–4, defines the fundamental memory type of the module.

Table A–4. Byte 2 Definition

FUNDAMENTAL MEMORY TYPE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	SEE APPENDIX
Reserved	0	0	0	0	0	0	0	0	N/A
Standard FPM	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**A**
EDO	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**A**
PNEDO	0	0	0	0	0	0	1	1	TBD
Sync. DRAM	0	0	0	0	0	1	0	0	B
TBD	0	0	0	0	0	1	0	1	TBD
TBD	0	0	0	0	0	1	1	0	TBD
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
TBD	1	1	1	1	1	1	0	1	TBD
TBD	1	1	1	1	1	1	1	0	TBD
255	1	1	1	1	1	1	1	1	TBD

A.2.4 Byte 3: Number of Row Addresses

This field describes the row addressing on the module. If there is one physical bank on the module, or, if there are two physical banks of the same size and organization, then bits 0–3 are used to represent the number of row addresses for each physical bank. If the module has two physical banks of asymmetric size, then bits 0–3 represent the number of row addresses for physical bank 1 and bits 4–7 represent the number of row addresses for physical bank 2. These do not include the bank address (BA) pin since physical bank selection on DIMM modules is asserted on dedicated BA pins. Note that if the module employs redundant addressing, then it is denoted in byte 21, bit 6. Examples of Byte 3 are shown in Table A–5. Table A–6 shows the byte definition.

Table A–5. Byte 3 Examples

# BANKS	# ROW ADDR BANK 1	# ROW ADDR BANK 2	MODULE ORGANIZATION	DISCRETE USED	BYTE 3 CONTENTS
1	11, RA0–RA10	N/A	2M x 64	2M x 8	0000 1011
2	11, RA0–RA10	11, RA0–RA10	2 x 2M x 64	2M x 8	0000 1011
2	11, RA0–RA10	11, RA0–RA10	2M x 64 & 1M x 64	2M x 8 & 1M x 16	1011 1011

Table A–6. Byte 3 Definition

# ROW ADDR					TABLE SUBFIELD A: Number of row addresses on Bank 1 –OR– Number of row addresses on Bank 1 or 2 if both banks are the same depth, bits 0–3			
					BIT 3	BIT 2	BIT 1	BIT 0
Undefined	See Subfield B				0	0	0	0
1/16					0	0	0	1
2/17					0	0	1	0
:					:	:	:	:
7					0	1	1	1
8					1	0	0	0
9					1	0	0	1
10					1	0	1	0
11					1	0	1	1
12					1	1	0	0
13					1	1	0	1
14					1	1	1	0
15					1	1	1	1
# ROW ADDR	TABLE SUBFIELD B: Number of row addresses on Bank 2 (if different from Bank 1), bits 4–7							
	BIT 7	BIT 6	BIT 5	BIT 4				
Undefined	0	0	0	0	See Subfield A			
1/16	0	0	0	1				
2/17	0	0	1	0				
:	:	:	:	:				
7	0	1	1	1				
8	1	0	0	0				
9	1	0	0	1				
10	1	0	1	0				
11	1	0	1	1				
12	1	1	0	0				
13	1	1	0	1				
14	1	1	1	0				
15	1	1	1	1				

A.2.5 Byte 4: Number of Column Addresses

This field describes the column addressing on the module. If there is one physical bank on the module, or, if there are two physical banks of the same size, then bits 0–3 are used to represent the number of column addresses for each physical bank. If the module has two physical banks of asymmetric size, then bits 0–3 represent the number of column addresses for physical bank 1 and bits 4–7 represent the number of column addresses for physical bank 2. Examples of Byte 4 are shown in Table A–7. Table A–8 shows the byte definition.

Table A–7. Byte 4 Examples

# BANKS	# COL ADDR BANK 1	# COL ADDR BANK 2	MODULE ORGANIZATION	DISCRETE USED	BYTE 3 CONTENTS
1	9, CA0–CA8	N/A	2M x 64	2M x 8	0000 1001
2	9, CA0–CA8	11, CA0–CA10	2 x 2M x 64	2M x 8	0000 1001
2	9, CA0–CA8	8, CA0–CA7	2M x 64 & 1M x 64	2M x 8 & 1M x 16	1000 1001

Table A–8. Byte 4 Definition

# COLUMN ADDR		TABLE SUBFIELD A: Number of column addresses on Bank 1 –OR– Number of row addresses on Bank 1 or 2 if both banks are the same depth, bits 0–3			
		BIT 3	BIT 2	BIT 1	BIT 0
Undefined	See Subfield B	0	0	0	0
1/16		0	0	0	1
2/17		0	0	1	0
:		:	:	:	:
7		0	1	1	1
8		1	0	0	0
9		1	0	0	1
10		1	0	1	0
11		1	0	1	1
12		1	1	0	0
13		1	1	0	1
14		1	1	1	0
15		1	1	1	1

# COLUMN ADDR	TABLE SUBFIELD B: Number of column addresses on Bank 2 (if different from Bank 1), bits 4–7				
	BIT 7	BIT 6	BIT 5	BIT 4	
Undefined	0	0	0	0	See Subfield A
1/16	0	0	0	1	
2/17	0	0	1	0	
:	:	:	:	:	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

A.2.6 Byte 5: Number of Banks

This field, shown in Table A–9, describes the number of banks on the DRAM module.

Table A–9. Byte 5 Definition

NUMBER OF BANKS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

A.2.7 Bytes 6 and 7: Module Data Width

This 16-bit field, divided among bytes 6 and 7, represents the data width of the module. Bit 0 of byte 6 represents the LSB of the 16-bit identifier, and bit 7 of byte 7 represents the MSB. If the width is less then 255 bits, then byte 7 becomes 00h. If the width is ≥ 256 bits, then bytes 6 and 7 are used to designate the total module width. Examples are shown in Table A–10. Table A–11 and Table A–12 show the byte definition.

Table A–10. Bytes 6 and 7 Examples

MODULE DATA WIDTH	BYTE 7	BYTE 6
64	0000 0000	0100 0000
72	0000 0000	0100 1000
780	0000 0011	0000 1100

Table A–11. Byte 6 (LSB Byte) Definition

DATA WIDTH	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
:	:	:	:	:	:	:	:	:
64	0	1	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
72	0	1	0	0	1	0	0	0
:	:	:	:	:	:	:	:	:
80	0	1	0	1	0	0	0	0
:	:	:	:	:	:	:	:	:
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

Table A–12. Byte 7 (MSB Byte) Definition

MODULE DATA WIDTH	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0(+)	0	0	0	0	0	0	0	0
256(+)	0	0	0	0	0	0	0	1
512(+)	0	0	0	0	0	0	1	0
1024(+)	0	0	0	0	0	0	1	1
2048(+)	0	0	0	0	0	1	0	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:

A.2.8 Byte 8: Module Interface Levels

This field, shown in Table A–13, describes the module's interface.

Table A–13. Byte 8 Definition

VOLTAGE INTERFACE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
5.0 Volt/TTL	0	0	0	0	0	0	0	0
LVTTL	0	0	0	0	0	0	0	1
HSTL 1.5	0	0	0	0	0	0	1	0
SSTL 3.3	0	0	0	0	0	0	1	1
SSTL 2.5	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
New Table	1	1	1	1	1	1	1	1

A.2.9 Byte 9: RAS Access Time (t_{RAC})

This field, shown in Table A–14, describes the module's RAS access time.

Table A–14. Byte 9 Definition

RAS ACCESS TIME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

A.2.10 Byte 10: CAS Access Time (t_{CAC})

This field, shown in Table A–15, describes the module's CAS access time.

Table A–15. Byte 10 Definition

CAS ACCESS TIME	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

A.2.11 Byte 11: DIMM Configuration Type

This field, shown in Table A–16, describes the module's error detection and/or correction schemes.

Table A–16. Byte 11 Definition

ERROR DET/COR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
None	0	0	0	0	0	0	0	0
Parity	0	0	0	0	0	0	0	1
ECC	0	0	0	0	0	0	1	0
TBD	0	0	0	0	0	0	1	1
TBD	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
TBD	1	1	1	1	1	1	1	1

A.2.12 Byte 12: Refresh Rate/Type

This field, shown in Table A–17, describes the module's refresh rate and type.

Table A–17. Byte 12 Definition

REFRESH PERIOD	BIT 7, SELF-REFRESH FLAG	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Normal (15.625us)	0	0	0	0	0	0	0	0
Reduced (.25x)…3.9us	0	0	0	0	0	0	0	1
Reduced (.5x)…7.8us	0	0	0	0	0	0	1	0
Extended (2x)…31.3us	0	0	0	0	0	0	1	1
Extended (4x)…62.5us	0	0	0	0	0	1	0	0
Extended (8x)…125us	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
TBD	0	0	0	0	0	1	1	1
TBD	0	0	0	0	1	0	0	0
TBD	0	0	0	0	1	0	0	1
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:

Table A–17. Byte 12 Definition (Continued)

REFRESH PERIOD	BIT 7, SELF-REFRESH FLAG	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SELF-REFRESH ENTRIES								
Normal (15.625us)	1	0	0	0	0	0	0	0
Reduced (.25x)…3.9us	1	0	0	0	0	0	0	1
Reduced (.5x)…7.8us	1	0	0	0	0	0	1	0
Extended (2x)…31.3us	1	0	0	0	0	0	1	1
Extended (4x)…62.5us	1	0	0	0	0	1	0	0
Extended (8x)…125us	1	0	0	0	0	1	0	1
TBD	1	0	0	0	0	1	1	0
TBD	:	:	:	:	:	:	:	:
TBD	:	:	:	:	:	:	:	:
TBD	1	1	1	1	1	1	1	0
TBD	1	1	1	1	1	1	1	1

A.2.13 Byte 13: DRAM Width (Base DRAM)

This field describes the width of the base DRAMs used on the module. Examples of base DRAMs widths are x4,x8, x9, x16, x18 and x32. DRAMs that provide extra bits for error checking are also included. Examples are shown in Table A–18. Table A–19 shows byte definition.

Table A–18. Byte 13 Examples

MODULE WIDTH	BASE DRAM WIDTH	ERROR CHECKING DRAM WIDTH	QTY OF BASE DRAMS	BYTE 13 (BINARY)
x72	x8	x8	9	0000 1000
x72	x9	–	8	0000 1001
x72	x16	x1	4	0001 0000

Table A–19. Byte 13 Definition

DRAM WIDTH, PRIMARY DRAM	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

A.2.14 Byte 14: Error-Checking DRAM Data Width

This field describes the width of error-checking DRAMs if they are present on the module. If the base DRAMs defined in byte 13 incorporate error checking, then this byte is left blank (00h). Examples are shown in Table A–20. Table A–21 shows byte definition.

Table A–20. Byte 14 Examples

MODULE WIDTH	BASE DRAM WIDTH	ERROR-CHECKING DRAM WIDTH	QTY OF ERROR-CHECKING DRAMS	BYTE 14 (BINARY)
x72	x8	x8	1	0000 1000
x72	x9	–	–	0000 0000
x72	x16	x1	8	0000 0001

Table A–21. Byte 14 Definition

DRAM WIDTH, ERROR CHECKING DRAM	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

A.2.15 Bytes 15–31: Reserved for Future Offerings

These bytes will be programmed with “0s” if not used.

A.2.16 Bytes 32–61: Superset Features (Possibly Used in the Future)

These bytes will be programmed with “0s” if not used.

A.2.17 Byte 62: Serial Presence Detect Revision

As the SPD definition is updated, it becomes necessary to identify the version of SPD that is being discussed. This TI specification follows JEDEC SPD specification revision 1. Table A–22 shows the definition of Byte 62.

Table A–22. Byte 62 SPD Revisions

SPD REVISION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Initial Release	0	0	0	0	0	0	0	0
Rev 1	0	0	0	0	0	0	0	1
Rev 2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:

A.2.18 Byte 63: Checksum for Bytes 0–62

The checksum calculation process is as follows:

1. Convert binary information, in byte locations 0–62, to decimal.
2. Add together (sum) all decimal values for byte locations 0–62.
3. Divide the ‘sum’ by 256.
4. Convert the remainder to binary (will be < 256).
5. Store the result (a single byte) in address 63 as the checksum.

Example A–1. Checksum Calculation Process

SPD BYTE ADDRESS	SERIAL PD			CONVERT TO DECIMAL	
0	0010 0100	——>		36	
1	1111 1110	——>	+	254	
2	0000 0000	——>	+	0	
3	0000 0000	——>	+	0	
.	. .	.		.	
.	. .	.		.	
60	0000 0000	——>	+	0	
61	0000 0000	——>	+	0	
62	0000 0000	——>	+	0	
				———	
				290	(Sum of all decimal values)
				290/256	(Divide by 256.)
				=1	With a remainder of 34
				34	(Keep remainder.)
				0010 0010	(Convert remainder to binary.)
63	0010 0010	<——		Store in byte location 63.	

A.2.19 Bytes 64–125: Manufacturer's Serial-Presence-Detect Format

See Appendix C.

A.2.20 Bytes 126–127: Reserved for Future Use

A.2.21 Bytes 128–255: System Integrator's SPD Format

See Appendix C.

Appendix B Serial-Presence-Detect Format for Synchronous DRAM Modules

This appendix describes the serial-presence-detect format for synchronous DRAM modules. All features follow the JEDEC standard on the serial presence detect and will be updated when changes or new features become available. Table B–1 outlines these features; each feature is defined in section B.2.

B.1 SPD Format for SDRAM Modules

Table B–1. SPD Format for SDRAM Modules

BYTE NUMBER	FUNCTION
0	Defines number of bytes written into serial memory at module mfg.†
1	Total number of bytes of the SPD memory device‡
2	Fundamental memory type (SDRAM)
3	Number of row addresses on this assembly
4	Number of column addresses on this assembly
5	Number of module rows on this assembly
6	Data width of this assembly…
7	… Data width continuation
8	Voltage interface standard of this assembly
9	SDRAM cycle time at maximum-supported CAS latency (CL), CL=X
10	SDRAM access from clock
11	DIMM configuration type (nonparity, parity, ECC)
12	Refresh rate/type
13	SDRAM width, primary SDRAM
14	Error-checking SDRAM data width
15	Minimum clock delay, back-to-back random column addresses
16	Burst lengths supported
17	Number of banks on each SDRAM device
18	CAS latencies supported
19	CS latencies supported
20	Write latencies supported
21	SDRAM module attributes
22	General SDRAM device attributes
23	Minimum clock cycle time at CL X–1
24	Maximum data access time from clock at CL X–1
25	Minimum clock cycle time at CL X–2

† This is typically programmed as 128 bytes.
‡ This is typically 256 bytes.

Table B–1. SPD Format for SDRAM Modules (Continued)

BYTE NUMBER	FUNCTION
26	Maximum data access time from clock at CL X–2
27	Minimum row precharge time
28	Minimum row-active-to-row-active delay
29	Minimum RAS-to-CAS delay
30	Minimum RAS pulse width
31	Module bank density
32	Command and address signal input setup time
33	Command and address signal input hold time
34	Data signal input setup time
35	Data signal input hold time
36–61	Superset features (may be used in the future)
62	SPD revision designator
63	Checksum for bytes 0–62
64–71	Manufacturer's JEDEC ID code per JEP–106E
72	Manufacturing location
73–90	Manufacturer's part number
91–92	Revision code
93–94	Manufacturing date
95–98	Assembly serial number
99–125	Manufacturer-specific data
126	Intel specification frequency
127	Intel specification details for PC100 support
128–135	System integrator's ID
136–150	System integrator's P/N
151–152	System integrator's D/C
153–165	System integrator's S/N
166	Checksum for bytes 128–165
167–189	Top-level system serial number
190–221	Open
222	Checksum for bytes 167–221
223–253	Open
254	Checksum for bytes 223–253
255	Checksum for bytes 0–128

B.2 SPD Bytes Defined

B.2.1 Byte 0: Number of Bytes Written Into Serial Memory by Module Manufacturer

This 8-bit field, shown in Table B–2, describes the total number of bytes used by the module manufacturer for the SPD data and any (optional) specific supplier information. The byte count includes the fields for all required and optional data. This byte is typically programmed as 128 bytes.

Table B–2. Byte 0 Definition

NUMBER OF SPD BYTES	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

B.2.2 Byte 1: Total Number of Bytes of SPD Serial Memory

This 8-bit field, shown in Table B–3, describes the total size of the serial memory used to hold the serial-presence-detect data.

Table B–3. Byte 1 Definition

SERIAL MEMORY	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
RFU	0	0	0	0	0	0	0	0
2 Bytes	0	0	0	0	0	0	0	1
4 Bytes	0	0	0	0	0	0	1	0
8 Bytes	0	0	0	0	0	0	1	1
16 Bytes	0	0	0	0	0	1	0	0
32 Bytes	0	0	0	0	0	1	0	1
64 Bytes	0	0	0	0	0	1	1	0
128 Bytes	0	0	0	0	0	1	1	1
256 Bytes	0	0	0	0	1	0	0	0
512 Bytes	0	0	0	0	1	0	0	1
1024 Bytes	0	0	0	0	1	0	1	0
2048 Bytes	0	0	0	0	1	0	1	1
4096 Bytes	0	0	0	0	1	1	0	0
8192 Bytes	0	0	0	0	1	1	0	1
16264 Bytes	0	0	0	0	1	1	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
:	1	1	1	1	1	1	1	0
:	1	1	1	1	1	1	1	1

B.2.3 Byte 2: Fundamental Memory Type

This byte, shown in Table B–4, defines the fundamental memory type of the module.

Table B–4. Byte 2 Definition

FUNDAMENTAL MEMORY TYPE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	SEE APPENDIX
Reserved	0	0	0	0	0	0	0	0	N/A
Standard FPM DRAM	0	0	0	0	0	0	0	1	A
EDO	0	0	0	0	0	0	1	0	A
PNEDO	0	0	0	0	0	0	1	1	TBD
Sync. DRAM	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	B
TBD	0	0	0	0	0	1	0	1	TBD
TBD	0	0	0	0	0	1	1	0	TBD
:	:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:	:
TBD	1	1	1	1	1	1	0	1	TBD
TBD	1	1	1	1	1	1	1	0	TBD
255	1	1	1	1	1	1	1	1	TBD

B.2.4 Byte 3: Number of Row Addresses on This Assembly

This field describes the row addressing on the module. If there is one physical bank on the module or if there are two physical banks of the same size and organization, then bits 0–3 are used to represent the number of row addresses for each physical bank. If the module has two physical banks of different sizes, then bits 0–3 represent the number of row addresses for physical bank 1 and bits 4–7 represent the number of row addresses for physical bank 2. These do not include the bank address (BA) pin, since physical bank selection on DIMM modules is asserted on dedicated BA pins. Note that if the module employs redundant addressing, then it is denoted in byte 21, bit 6. Examples of byte 3 are shown in Table B–5. Table B–6 shows the byte definition.

Table B–5. Byte 3 Examples

# BANKS	# ROW ADDR BANK 1	# ROW ADDR BANK 2	MODULE ORGANIZATION	DISCRETE USED	BYTE 3 CONTENTS
1	11, RA0–RA 10	N/A	2M x 64	2M x 8	0000 1011
2	11, RA0–RA 10	11, RA0–RA 10	2 x 2M x 64	2M x 8	0000 1011
2	11, RA0–RA 10	11, RA0–RA 10	2M x 64 & 1M x 64	2M x 8 & 1M x 16	1011 1011

Table B–6. Byte 3 Definition

# ROW ADDR		TABLE SUBFIELD A: Number of row addresses on Bank 1 –OR– Number of row addresses on Bank 1 or 2 if both banks are the same depth, bits 0–3			
		BIT 3	BIT 2	BIT 1	BIT 0
Undefined	See Subfield B	0	0	0	0
1/16		0	0	0	1
2/17		0	0	1	0
:		:	:	:	:
7		0	1	1	1
8		1	0	0	0
9		1	0	0	1
10		1	0	1	0
11		1	0	1	1
12		1	1	0	0
13		1	1	0	1
14		1	1	1	0
15		1	1	1	1

# ROW ADDR	TABLE SUBFIELD B: Number of row addresses on Bank 2 (if different from Bank 1), bits 4–7				
	BIT 7	BIT 6	BIT 5	BIT 4	
Undefined	0	0	0	0	See Subfield A
1/16	0	0	0	1	
2/17	0	0	1	0	
:	:	:	:	:	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

B.2.5 Byte 4: Number of Column Addresses on This Assembly

This field describes the column addressing on the module. If there is one physical bank on the module or if there are two physical banks of the same size, then bits 0–3 are used to represent the number of column addresses for each physical bank. If the module has two physical banks of asymmetric size, then bits 0–3 represent the number of column addresses for physical bank 1 and bits 4–7 represent the number of column addresses for physical bank 2. Examples are shown in Table B–7. Table B–8 shows the byte definition.

Table B–7. Byte 4 Examples

# BANKS	# COL ADDR BANK 1	# COL ADDR BANK 2	MODULE ORGANIZATION	DISCRETE USED	BYTE 3 CONTENTS
1	9, CA0–CA 8	N/A	2M x 64	2M x 8	0000 1001
2	9, CA0–CA 8	11, CA0–CA 10	2 x 2M x 64	2M x 8	0000 1001
2	9, CA0–CA 8	8, CA0–CA 7	2M x 64 & 1M x 64	2M x 8 & 1M x 16	1000 1001

Table B–8. Byte 4 Definition

# COLUMN ADDR		TABLE SUBFIELD A: Number of column addresses on Bank 1 –OR– Number of column addresses on Bank 1 or 2 if both banks are the same depth, bits 0–3			
		BIT 3	BIT 2	BIT 1	BIT 0
Undefined	See Subfield B	0	0	0	0
1/16		0	0	0	1
2/17		0	0	1	0
:		:	:	:	:
7		0	1	1	1
8		1	0	0	0
9		1	0	0	1
10		1	0	1	0
11		1	0	1	1
12		1	1	0	0
13		1	1	0	1
14		1	1	1	0
15		1	1	1	1

# COLUMN ADDR	TABLE SUBFIELD B: Number of column addresses on Bank 2 (if different from Bank 1), bits 4–7				
	BIT 7	BIT 6	BIT 5	BIT 4	
Undefined	0	0	0	0	See Subfield A
1/16	0	0	0	1	
2/17	0	0	1	0	
:	:	:	:	:	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	1	0	1	0	
11	1	0	1	1	
12	1	1	0	0	
13	1	1	0	1	
14	1	1	1	0	
15	1	1	1	1	

B.2.6 Byte 5: Number of Module Rows on This Assembly

This field, shown in Table B–9, indicates the number of physical rows on the module.

Table B–9. Byte 5 Definition

NUMBER OF BANKS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

B.2.7 Bytes 6 and 7: Module Data Width of This Assembly

This 16-bit field, divided between bytes 6 and 7, represents the data width of the module. Bit 0 of byte 6 represents the LSB of the 16-bit identifier, and bit 7 of byte 7 represents the MSB. If the width is less than 255 bits, then byte 7 becomes 00h. If the width is ≥ 256 bits, then bytes 6 and 7 are used to designate the total module width. Examples are shown in Table B–10. Table B–11 and Table B–12 show the byte definition.

Table B–10. Bytes 6 and 7 Examples

MODULE DATA WIDTH	BYTE 7	BYTE 6
64	0000 0000	0100 0000
72	0000 0000	0100 1000
780	0000 0011	0000 1100

Table B–11. Byte 6 (LSB Byte) Definition

DATA WIDTH	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
:	:	:	:	:	:	:	:	:
64	0	1	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
72	0	1	0	0	1	0	0	0
:	:	:	:	:	:	:	:	:
80	0	1	0	1	0	0	0	0
:	:	:	:	:	:	:	:	:
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

Table B–12. Byte 7 (MSB Byte) Definition

MODULE DATA WIDTH	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0(+)	0	0	0	0	0	0	0	0
256(+)	0	0	0	0	0	0	0	1
512(+)	0	0	0	0	0	0	1	0
1024(+)	0	0	0	0	0	0	1	1
2048(+)	0	0	0	0	0	1	0	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:

B.2.8 Byte 8: Module Interface Standard of This Assembly

This field, shown in Table B–13, describes the module's voltage interface.

Table B–13. Byte 8 Definition

VOLTAGE INTERFACE	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
5.0 Volt/TTL	0	0	0	0	0	0	0	0
LVTTL	0	0	0	0	0	0	0	1
HSTL 1.5	0	0	0	0	0	0	1	0
SSTL 3.3	0	0	0	0	0	0	1	1
SSTL 2.5	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
New Table	1	1	1	1	1	1	1	1

B.2.9 Byte 9: SDRAM Cycle Time at Maximum Supported CAS Latency (CL), CL=X

This byte, shown in Table B–14, defines the total minimum cycle time for the SDRAM module at the maximum CAS latency specified in byte 18. The byte is broken into two nibbles: the higher order nibble (bits 4–7) designates the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0–3) has a granularity of 1/10ns and is added to the value designated by the higher order nibble. For example, if:

Bits 7:4 are		and bits 3:0 are		then the cycle time is
1010		0101		
(10ns)	+	(0.5ns)	=	10.5ns

Table B–14. Byte 9 Definition

NANOSECONDS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SDRAM CYCLE TIME SUBFIELD A: Units of ns (bits 4 through 7)								
Undefined	0	0	0	0	See Subfield Table B			
1	0	0	0	1				
2	0	0	1	0				
3	0	0	1	1				
4	0	1	0	0				
5	0	1	0	1				
6	0	1	1	0				
7	0	1	1	1				
8	1	0	0	0				
9	1	0	0	1				
10	1	0	1	0				
11	1	0	1	1				
12	1	1	0	0				
13	1	1	0	1				
14	1	1	1	0				
15	1	1	1	1				
SDRAM CYCLE TIME SUBFIELD B: Tenths of ns (bits 0 through 3)								
+0ns	See Subfield Table A				0	0	0	0
+0.1					0	0	0	1
+0.2					0	0	1	0
+0.3					0	0	1	1
+0.4					0	1	0	0
+0.5					0	1	0	1
+0.6					0	1	1	0
+0.7					0	1	1	1
+0.8					1	0	0	0
+0.9					1	0	0	1
RFU					1	0	1	0
:	:	:	:	:	:	:	:	:
Undefined	1	1	1	1	1	1	1	1

B.2.10 Byte 10: SDRAM Access From Clock

This byte, shown in Table B–15, defines the maximum clock to data out for the SDRAM module. These are the clock-to-data out specifications at the maximum CAS latency specified in byte 18. The byte is broken into two nibbles: the higher order nibble (bits 4–7) designates the cycle time to a granularity of 1ns; the value presented by the lower order nibble (bits 0–3) has a granularity of 1/10ns and is added to the value designated by the higher order nibble. For example, if:

Bits 7:4 are		and bits 3:0 are		then the cycle time is
1010		0101		
(10ns)	+	(0.5ns)	=	10.5ns

Table B–15. Byte 10 Definition

NANOSECONDS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SDRAM CYCLE TIME SUBFIELD A: Units of ns (bits 4 through 7)								
Undefined	0	0	0	0	See Subfield Table B			
1	0	0	0	1				
2	0	0	1	0				
3	0	0	1	1				
4	0	1	0	0				
5	0	1	0	1				
6	0	1	1	0				
7	0	1	1	1				
8	1	0	0	0				
9	1	0	0	1				
10	1	0	1	0				
11	1	0	1	1				
12	1	1	0	0				
13	1	1	0	1				
14	1	1	1	0				
15	1	1	1	1				
SDRAM CYCLE TIME SUBFIELD B: Tenths of ns (bits 0 through 3)								
+0ns	See Subfield Table A				0	0	0	0
+0.1					0	0	0	1
+0.2					0	0	1	0
+0.3					0	0	1	1
+0.4					0	1	0	0
+0.5					0	1	0	1
+0.6					0	1	1	0
+0.7					0	1	1	1
+0.8					1	0	0	0
+0.9					1	0	0	1
RFU					1	0	1	0
:	:	:	:	:	:	:	:	:
Undefined	1	1	1	1	1	1	1	1

B.2.11 Byte 11: DIMM Configuration Type

This field, shown in Table B–16, describes the module's error-detection and/or correction schemes.

Table B–16. Byte 11 Definition

ERROR DET/COR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
None	0	0	0	0	0	0	0	0
Parity	0	0	0	0	0	0	0	1
ECC	0	0	0	0	0	0	1	0
TBD	0	0	0	0	0	0	1	1
TBD	0	0	0	0	0	1	0	0
TBD	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
TBD	1	1	1	1	1	1	1	1

B.2.12 Byte 12: Refresh Rate/Type

This field, shown in Table B–17, describes the module's refresh rate and type.

Table B–17. Byte 12 Definition

REFRESH PERIOD	BIT 7, SELF-REFRESH FLAG	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Normal (15.625us)	0	0	0	0	0	0	0	0
Reduced (.25x)…3.9us	0	0	0	0	0	0	0	1
Reduced (.5x)…7.8us	0	0	0	0	0	0	1	0
Extended (2x)…31.3us	0	0	0	0	0	0	1	1
Extended (4x)…62.5us	0	0	0	0	0	1	0	0
Extended (8x)…125us	0	0	0	0	0	1	0	1
TBD	0	0	0	0	0	1	1	0
TBD	0	0	0	0	0	1	1	1
TBD	0	0	0	0	1	0	0	0
TBD	0	0	0	0	1	0	0	1
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
Normal (15.625us)	1	0	0	0	0	0	0	0
Reduced (.25x)…3.9us	1	0	0	0	0	0	0	1
Reduced (.5x)…7.8us	1	0	0	0	0	0	1	0
Extended (2x)…31.3us	1	0	0	0	0	0	1	1
Extended (4x)…62.5us	1	0	0	0	0	1	0	0
Extended (8x)…125us	1	0	0	0	0	1	0	1

Table B–17. Byte 12 Definition (Continued)

REFRESH PERIOD	BIT 7, SELF-REFRESH FLAG	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TBD	1	0	0	0	0	1	1	0
TBD	:	:	:	:	:	:	:	:
TBD	:	:	:	:	:	:	:	:
TBD	1	1	1	1	1	1	1	0
TBD	1	1	1	1	1	1	1	1

B.2.13 Byte 13: SDRAM Width, Primary SDRAM

Bits 0–6 of this byte relate to the primary SDRAM's data width. Bit 7 is a flag that is set to 1 when there is a second physical bank on the module whose size differs from that of the first physical bank. A1 in bit 7 indicates that the second physical bank's data RAMs are twice the width of those on the first physical bank. If there is a second physical bank of the same size and organization as the first, then bit 7 remains 0 and bits 0–6 indicates the error-checking SDRAM width for both banks.

The primary SDRAM is the one that is used for data; examples of primary (data) SDRAM widths are x4, x8, x16, and x32. Note that if the module contains SDRAMs that provide for data and error checking (e.g. x9, x18, and x36), then it is also designated in this field. Table B–18 shows examples of SDRAM DIMMs using 1 and 2 banks of symmetrical and asymmetrical size. Table B–19 shows the byte definition.

Table B–18. Byte 13 Examples

MODULE WIDTH	PHYS. BANK 1 PRIMARY SDRAM WIDTH	PHYS. BANK 2 PRIMARY SDRAM WIDTH	PHYS. BANK 1 ERROR-CHECKING SDRAM WIDTH	PHYS. BANK 2 ERROR-CHECKING SDRAM WIDTH	POSSIBLE (16MB-BASED) MODULE DENSITY	BYTE 13 CONTENTS
x72	x9	N/A	—	N/A	16MB	0000 1001
x72	x8	N/A	x8	N/A	16MB	0000 1000
x72	x16	N/A	x4	N/A	8MB	0001 0000
x72	x8	x8	x8	x8	32MB	0000 1000
x64	x8	x16	N/A	N/A	24MB	1000 1000

Table B–19. Byte 13 Definition

SUBFIELD A: DATA SDRAM WIDTH								
DATA SDRAM WIDTH	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
N/A	See Subfield B	0	0	0	0	0	0	0
1		0	0	0	0	0	0	1
:		:	:	:	:	:	:	:
4		0	0	0	0	1		0
:		:	:	:	:	:	:	:
8		0	0	0	1	0	0	0
9		0	0	0	1	0	0	1
:		:	:	:	:	:	:	:
15		0	0	0	1	1	1	1
16		0	0	1	0	0	0	0
17		0	0	1	0	0	0	1
:		:	:	:	:	:	:	:
32		0	1	0	0	0	0	0
:		:	:	:	:	:	:	:
36		0	1	0	0	1	0	0
:		:	:	:	:	:	:	:
127		1	1	1	1	1	1	1
SUBFIELD B: BANK 2 DATA SDRAM WIDTH MULTIPLIER								
BANK 2 DATA SDRAM WIDTH MULTIPLIER	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
No Bank 2 –OR– Bank 2 uses same width SDRAM as bank 1	0	See Subfield A						
Bank 2's SDRAM is 2X the width of Bank 1's SDRAM	1							

B.2.14 Byte 14: Error-Checking SDRAM Data Width

If the module incorporates error checking and the primary SDRAM does not include these bits (i.e. there are separate error checking SDRAMs), then the error-checking SDRAM's width is expressed in bits 0–6 of byte 14. Bit 7 is a flag that is set to 1 when there is a second physical bank on the module whose size differs from the first physical bank A1 in bit 7 indicates that the error-checking RAMs in bank 2 are twice as wide as those on the first physical bank. If there is a second physical bank of same size and organization as the first, then bit 7 remains 0 and bits 0–6 indicate the error checking SDRAM width for both physical banks.

Table B–20 shows examples of error-checking SDRAM widths with physical banks of symmetric and asymmetric sizing. Table B–21 shows the byte definition.

Table B–20. Byte 14 Examples

MODULE WIDTH	PHYS. BANK 1 PRIMARY SDRAM WIDTH	PHYS. BANK 2 PRIMARY SDRAM WIDTH	PHYS. BANK 1 ERROR-CHECKING SDRAM WIDTH	PHYS. BANK 2 ERROR-CHECKING SDRAM WIDTH	POSSIBLE (16MB-BASED) MODULE DENSITY	BYTE 14 CONTENTS
x72	x9	N/A	—	N/A	8MB	0000 0000
x72	x8	N/A	x8	N/A	16MB	0000 1000
x72	x16	N/A	x4	N/A	8MB	0000 0100
x72	x8	x8	x8	x8	32MB	0000 1000
x72	x8	x16	x8	x16	24MB	1000 1000
x72	x8	x16	x8	x16	24MB	1000 1000

Table B–21. Byte 14 Definition

SUBFIELD A: ERROR-CHECKING SDRAM WIDTH								
DATA SDRAM WIDTH	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
N/A	See Subfield B	0	0	0	0	0	0	0
1		0	0	0	0	0	0	1
:		:	:	:	:	:	:	:
4		0	0	0	0	1		0
:		:	:	:	:	:	:	:
8		0	0	0	1	0	0	0
9		0	0	0	1	0	0	1
:		:	:	:	:	:	:	:
15		0	0	0	1	1	1	1
16		0	0	1	0	0	0	0
17		0	0	1	0	0	0	1
:		:	:	:	:	:	:	:
32		0	1	0	0	0	0	0
:		:	:	:	:	:	:	:
36		0	1	0	0	1	0	0
:		:	:	:	:	:	:	:
127		1	1	1	1	1	1	1
SUBFIELD B: BANK 2 ERROR-CHECKING SDRAM WIDTH MULTIPLIER								
BANK 2 ERROR-CHECKING SDRAM WIDTH MULTIPLIER	**BIT 7**	**BIT 6**	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BIT 1**	**BIT 0**
No Bank 2 –OR– Bank 2 uses same width SDRAM as bank 1	0	See Subfield A						
Bank 2's SDRAM is 2X the width of Bank 1's SDRAM	1							

B.2.15 Byte 15: Minimum Clock Delay, Back-to-Back Random Column Addresses (nCCD)

Table B–22 shows the definition for byte 15.

Table B–22. Byte 15 Definition

NUMBER OF CLOCKS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

B.2.16 Byte 16: Burst Lengths Supported

This byte, shown in Table B–23, defines which burst lengths are supported. If the burst length is supported, then the corresponding bit is 1.

Table B–23. Byte 16 Definition

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Burst Length = Page	TBD	TBD	TBD	Burst Length = 8	Burst Length = 4	Burst Length = 2	Burst Length = 1
1 or 0	0	0	0	1 or 0	1 or 0	1 or 0	1 or 0

B.2.17 Byte 17: Number of Banks on Each SDRAM Device

This byte, shown in Table B–24, defines the number of banks internal to each discrete SDRAM device on the module.

Table B–24. Byte 17 Definition

NUMBER OF BANKS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

B.2.18 Byte 18: CAS Latencies Supported

This byte, shown in Table B–25, defines which CAS latencies are supported. If the bit is 1, then that CAS latency is supported; otherwise, it is 0.

Table B–25. Byte 18 Definition

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TBD	CAS latency = 7	CAS latency = 6	CAS latency = 5	CAS latency = 4	CAS latency = 3	CAS latency = 2	CAS latency = 1
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

B.2.19 Byte 19: CS Latencies Supported

This byte, shown in Table B–26, defines which CS latencies are acceptable for the module. If the bit is 1, then that CS latency is supported; otherwise, it is 0.

Table B–26. Byte 19 Definition

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TBD	CS latency = 6	CS latency = 5	CS latency = 4	CS latency = 3	CS latency = 2	CS latency = 1	CS latency = 0
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

B.2.20 Byte 20: Write Latency

This byte, shown in Table B–27, defines which write latencies are acceptable for the module. If the bit is 1, then that WE latency is supported; otherwise, it is 0.

Table B–27. Byte 20 Definition

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TBD	WE latency = 6	WE latency = 5	WE latency = 4	WE latency = 3	WE latency = 2	WE latency = 1	WE Latency = 0
1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

B.2.21 Byte 21: SDRAM Module Attributes

This byte, shown in Table B–28, defines certain features of the module. If the feature is present, then the bit is 1. Conversely, if the feature is not present, then the bit is 0.

Table B–28. Byte 21 Definition

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TBD	Redundant addressing†	Differential clock input	Registered DQMB inputs	Buffered DQMB inputs	On-card PLL (clock)	Registered address and control inputs‡	Buffered address and control inputs‡
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

† Redundant Addressing implies the use of SDRAMs having the same address depth (e.g. 4Mx4 mixed with 4Mx16) in the same 8 byte quad word, but having different RAS/CAS addressing and/or different numbers of device banks. Actual implementation is not yet determined.

‡ Address, RAS, CAS, WE, CKE, CS

B.2.22 Byte 22: General SDRAM Device Attributes

This byte, shown in Table B–29, defines certain features of the SDRAMs on the module. Unless otherwise specified, if the feature is present, then the bit is 1. Conversely, if the feature is not present, then the designated bit is 0.

Table B–29. Byte 22 Definition

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
TBD	TBD	Upper Vcc tolerance§: 0=10% 1=5%	Lower Vcc tolerance§: 0=10% 1=5%	Supports Write1/Read Burst 0=false 1=true	Supports Precharge All 0=false 1=true	Supports auto Precharge 0=false 1=true	Supports Early RAS# Precharge 0=false 1=true
0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0	1 or 0

§ Tolerance refers to the voltage range under which the SDRAMs operate to the timings specified in SPD bytes 9, 10, 23–30.

B.2.23 Byte 23: Minimum Clock Cycle Time at CL of X–1

The highest CAS latency identified in byte 18 is X; bytes 9 and 10 identify the timing values associated with CAS latency X. Byte 23 identifies the minimum cycle time at CAS X–1. For example, if byte 18 indicates CAS latencies of 1–3, then X is 3 and X–1 is 2. Byte 23 then splits the minimum cycle time at CAS latency = 2.

Byte 23 is broken down into two nibbles designating cycle time. The value in the higher order nibble (bits 4–7) has a granularity of 1ns. The value in the lower order nibble (bits 0–3) has a granularity of 1/10ns and is added to the value in the higher order nibble.

For example, if:

Bits 7:4 are		and bits 3:0 are		then the cycle time is
1001		0101		
(9ns)	+	(0.5ns)	=	9.5ns

Table B–30 shows the definition for byte 23.

Table B–30. Byte 23 Definition

NANOSECONDS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SDRAM MINIMUM CYCLE TIME AT CL OF X–1: Subfield A: Units of ns (Bits 4 through 7)								
Undefined	0	0	0	0	See Subfield Table B			
1/16	0	0	0	1				
2/17	0	0	1	0				
3/18	0	0	1	1				
4	0	1	0	0				
5	0	1	0	1				
6	0	1	1	0				
7	0	1	1	1				
8	1	0	0	0				
9	1	0	0	1				
10	1	0	1	0				
11	1	0	1	1				
12	1	1	0	0				
13	1	1	0	1				
14	1	1	1	0				
15	1	1	1	1				
SDRAM MINIMUM CYCLE TIME AT CL OF X–1: Subfield B: Tenths of ns (Bits 0 through 3)								
+0ns	See Subfield Table A				0	0	0	0
+0.1					0	0	0	1
+0.2					0	0	1	0
+0.3					0	0	1	1
+0.4					0	1	0	0
+0.5					0	1	0	1
+0.6					0	1	1	0
+0.7					0	1	1	1
+0.8					1	0	0	0
+0.9					1	0	0	1
RFU					1	0	1	0
:	:	:	:	:	:	:	:	:
Undefined	1	1	1	1	1	1	1	1

B.2.24 Byte 24: Maximum Data Access Time from CLK at CAS Latency of X–1

The highest CAS latency identified in byte 18 is X. Byte 24 indicates the maximum access time from CLK at CAS latency of X–1. For example, if byte 18 indicates supported CAS latencies of 1–3, then X is 3 and X–1 is 2. Byte 24 then indicates the maximum data access time from CLK at CAS latency of 2.

The byte is split into two nibbles designating access time: the value in the higher order nibble (bits 4–7) has a granularity of 1ns; the value in the lower order nibble (bits 0–3) has a granularity of 1/10ns and is added to the value in the higher order nibble.

For example, if:

Bits 7:4 are		and bits 3:0 are		then the cycle time is
1001		0101		
(9ns)	+	(0.5ns)	=	9.5ns

Table B–31 shows the definition for byte 24.

Table B–31. Byte 24 Definition

NANOSECONDS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SDRAM ACCESS TIME FROM CLOCK AT CL OF X–1: Subfield A: Units of ns (bits 4 through 7)								
Undefined	0	0	0	0	See Subfield Table B			
1/16	0	0	0	1				
2/17	0	0	1	0				
3/18	0	0	1	1				
4	0	1	0	0				
5	0	1	0	1				
6	0	1	1	0				
7	0	1	1	1				
8	1	0	0	0				
9	1	0	0	1				
10	1	0	1	0				
11	1	0	1	1				
12	1	1	0	0				
13	1	1	0	1				
14	1	1	1	0				
15	1	1	1	1				
SDRAM ACCESS TIME FROM CLOCK AT CL OF X–1: Subfield B: Tenths of ns (bits 0 through 3)								
+0ns	See Subfield Table A				0	0	0	0
+0.1					0	0	0	1
+0.2					0	0	1	0
+0.3					0	0	1	1
+0.4					0	1	0	0
+0.5					0	1	0	1
+0.6					0	1	1	0
+0.7					0	1	1	1
+0.8					1	0	0	0
+0.9					1	0	0	1
RFU					1	0	1	0
:	:	:	:	:	:	:	:	:
Undefined	1	1	1	1	1	1	1	1

B.2.25 Byte 25: Minimum Clock Cycle Time at CAS Latency of X–2

The highest CAS latency identified in byte 18 is X. Byte 25 indicates the minimum cycle time at CAS Latency X–2. For example, if byte 18 indicates CAS latencies of 1–3, then X is 3 and X–2 is 1. Byte 25 then indicates the minimum cycle time at CAS Latency 1.

Byte 25 is split into two orders of bits (high and low) designating cycle time: the higher order bits (bits 2–7) designate the cycle time to a granularity of 1ns; the value presented by the lower order bits (0–1) has a granularity of 1/4ns and is added to the value in the higher order bits.

For example, if:

Bits 7:2 are		and bits 1:0 are		then the cycle time is
011001		00		
(25ns)	+	(0.0ns)	=	25.0ns

Bits 7:2 are		and bits 1:0 are		then the cycle time is
100001		11		
(9ns)	+	(0.75ns)	=	9.75ns

Table B–32 shows the definition for byte 25.

Table B–32. Byte 25 Definition

NANOSECONDS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	SDRAM MINIMUM CYCLE TIME AT CL OF X–2: Subfield A: Units of ns (bits 2 through 7)							
Undefined	0	0	0	0	0	0	See Subfield Table B	
1	0	0	0	0	0	1		
2	0	0	0	0	1	0		
3	0	0	0	0	1	1		
4	0	0	0	1	0	0		
5	0	0	0	1	0	1		
6	0	0	0	1	1	0		
7	0	0	0	1	1	1		
8	0	0	1	0	0	0		
9	0	0	1	0	0	1		
10	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61	1	1	1	1	0	1		
62	1	1	1	1	1	0		
63	1	1	1	1	1	1		
							SDRAM MINIMUM CYCLE TIME AT CL = X–2: Subfield B: Quarters of ns (bits 0 through 1)	
+0ns	See Subfield Table A						0	0
+0.25							0	1
+0.5							1	0
+0.75							1	1

B.2.26 Byte 26: Maximum Data Access Time From CLK at CAS Latency of X–2

The highest CAS latency identified in byte 18 is X. Byte 26 indicates the maximum access time from the CLK at CAS latencies X–2. For example, if byte 18 indicates CAS latencies of 1–3, then X is 3 and X–2 is 1. Byte 26 then indicates the maximum data access time from CLK at CAS latency of 1.

The byte is split into two orders (high and low) of bits designating a data access time: the higher order bits (bits 2–7) have a granularity of 1ns; the value in the lower order bits (bits 0–1) has a granularity of 1/4ns, and is added to the value in the higher order bits.

For example, if:

Bits 7:2 are		and bits 1:0 are		then the maximum access time is
001001		01		
(9ns)	+	(0.25ns)	=	9.25ns

Table B–33 shows the definition of byte 26.

Table B–33. Byte 26 Definition

NANOSECONDS	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	SDRAM MINIMUM CYCLE TIME AT CL X–2: Subfield A: Units of ns (bits 2 through 7)							
Undefined	0	0	0	0	0	0	See Subfield Table B	
1	0	0	0	0	0	1		
2	0	0	0	0	1	0		
3	0	0	0	0	1	1		
4	0	0	0	1	0	0		
5	0	0	0	1	0	1		
6	0	0	0	1	1	0		
7	0	0	0	1	1	1		
8	0	0	1	0	0	0		
9	0	0	1	0	0	1		
10	0	0	1	0	1	0		
:	:	:	:	:	:	:		
:	:	:	:	:	:	:		
61	1	1	1	1	0	1		
62	1	1	1	1	1	0		
63	1	1	1	1	1	1		
							SDRAM MINIMUM CYCLE TIME AT CL = X–2: Subfield B: Quarters of ns (Bits 0 through 1)	
+0ns	See Subfield Table A						0	0
+0.25							0	1
+0.5							1	0
+0.75							1	1

B.2.27 Byte 27: Minimum Row Precharge Time (t_{RP})

Byte 27, shown in Table B–34, indicates the module's minimum row precharge time.

Table B–34. Byte 27 Definition

MINIMUM ROW PRECHARGE TIME (NANOSECONDS)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	0
31	0	0	0	1	1	1	1	1
32	0	0	1	0	0	0	0	0
33	0	0	1	0	0	0	0	1
34	0	0	1	0	0	0	1	0
35	0	0	1	0	0	0	1	1
36	0	0	1	0	0	1	0	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

B.2.28 Byte 28: Minimum Row-Active-to-Row-Active Delay (t_{RRD})

This field, shown in Table B–35, indicates the minimum required delay between row activations.

Table B–35. Byte 28 Definition

MINIMUM ROW-ACTIVE-TO-ROW-ACTIVE DELAY (NANOSECONDS)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
20	0	0	0	1	0	1	0	0
21	0	0	0	1	0	1	0	1
22	0	0	0	1	0	1	1	0
23	0	0	0	1	0	1	1	1
24	0		0	1	1	0	0	0
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	1
:	:	:	:	:	:	:	:	:
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

B.2.29 Byte 29: Minimum RAS-to-CAS Delay (t_{RCD})

Byte 29, shown in Table B–36, indicates the minimum delay required between assertions of RAS and CAS.

Table B–36. Byte 29 Definition

MINIMUM RAS TO CAS DELAY (NANOSECONDS)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	1
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

B.2.30 Byte 30: Minimum RAS Pulse Width (t_{RAS})

Byte 30, shown in Table B–37, defines the minimum RAS pulse width.

Table B–37. Byte 30 Definition

MINIMUM RAS PULSE WIDTH (NANOSECONDS)	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Undefined	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
25	0	0	0	1	1	0	0	1
26	0	0	0	1	1	0	1	0
27	0	0	0	1	1	0	1	1
28	0	0	0	1	1	1	0	0
29	0	0	0	1	1	1	0	1
30	0	0	0	1	1	1	1	1
:	:	:	:	:	:	:	:	:
50	0	0	1	1	0	0	1	0
:	:	:	:	:	:	:	:	:
60	0	0	1	1	1	1	0	0
:	:	:	:	:	:	:	:	:
70	0	1	0	0	0	1	1	0
:	:	:	:	:	:	:	:	:
127	0	1	1	1	1	1	1	1
128	1	0	0	0	0	0	0	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
254	1	1	1	1	1	1	1	0
255	1	1	1	1	1	1	1	1

B.2.31 Byte 31: Module Bank Density

This byte indicates the density of each physical bank on the SDRAM DIMM. This byte will have at least one bit set to 1 to represent the density of at least one bank. If there is more than one physical bank on the module (indicated by byte 5) and all banks have the same density, then only one bit in this field is set. If the module has more than one physical bank of different sizes, then more than one bit will be set; each bit set for each density represented. Examples are shown in Table B–38. Table B–39 shows byte definition.

Table B–38. Byte-31 Examples

# BANKS	DENSITY OF PHYSICAL BANK 1	DENSITY OF PHYSICAL BANK 2	BYTE 31 CONTENTS
1	32M byte	N/A	0000 1000
2	32M byte	32M byte	0000 1000
2	32M byte	16M byte	0000 1100

Table B–39. Byte-31 Definition

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DENSITY	512M byte	256M byte	128M byte	64M byte	32M byte	16M byte	8M byte	4M byte
N/Y	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

B.2.32 Byte 32: Command and Address Signal Input Setup Time

This byte describes the command and address signal input setup time with respect to the rising edge of the clock input. Both positive and negative setup times are supported. If bit 7 is equal to 0, then the signal input setup time is positive with respect to the clock. If bit 7 is equal to 1, then, the signal input setup time is negative with repect to the clock. Bit 4 through bit 6 define the setup time in nanoseconds (ns) and bit 0 through bit 3 define the signal input setup time in a tenth of a nanosecond.

Table B–40. Byte-32 Definition

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
POSITIVE/ NEGATIVE	Setup time in ns			Setup time in tenths of a ns			
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

For example if:

Bit 7 is	and bits 6:4 are		and bits 3:0 are		then the signal input setup time is
0	010		0101		
+	2 ns	+	0.05 ns	=	2.5 ns

For example if:

Bit 7 is	and bits 6:4 are		and bits 3:0 are		then the signal input setup time is
1	000		0101		
–	(0 ns)	=	0.05 ns	=	–0.5ns

B.2.33 Byte 33: Command and Address Signal Input Hold Time

This byte describes the command and address signal input hold time with respect to the rising edge of the clock input. Both positive and negative hold times are supported. If bit 7 is equal to 0, then the signal input hold time is positive with respect to the clock. If bit 7 is equal to 1, then the signal input hold time is negative with respect to the clock. Bits 6 through bit 4 define the hold time in nanoseconds (ns) and bits 3 through 0 define the signal input hold time in a tenth of a nanosecond.

Table B–41. Byte-33 Definition

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
POSITIVE/ NEGATIVE	Setup time in ns			Setup time in tenths of a ns			
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

For example if:

Bit 7 is	and bits 6:4 are		and bits 3:0 are		then the signal input hold time is
0	010		0101		
+	2 ns	+	0.05 ns	=	2.5 ns

For example if:

Bit 7 is	and bits 6:4 are		and bits 3:0 are		then the signal input hold time is
1	000		0101		
–	(0 ns)	=	0.05 ns	=	–0.5ns

B.2.34 Byte 34: Data Signal Input Setup Time

This byte describes the data signal input setup time with respect to the rising edge of the clock input. Both positive and negative setup times are supported. If bit 7 is equal to 0, then the signal input setup time is positive with respect to the clock. If bit 7 is equal to 1, then the signal input setup time is negative with respect to the clock. Bit 6 through bit 4 define the setup time in nanoseconds (ns) and bits 3 through 0 define the signal input setup time in a tenth of a nanosecond.

For example if:

Bit 7 is	and bits 6:4 are		and bits 3:0 are		then the signal input setup time is
0	010		0101		
+	2 ns	+	0.05 ns	=	2.5 ns

For example if:

Bit 7 is	and bits 6:4 are		and bits 3:0 are		then the signal input setup time is
1	000		0101		
–	(0 ns)	=	0.05 ns	=	–0.5ns

B.2.35 Byte 35: Data Signal Input Hold Time

This byte describes the input hold time with respect to the rising edge of the clock input. Both positive and negative hold times are supported. If bit 7 is equal to 0, then the signal input hold time is positive with respect to the clock. If bit 7 is equal to 1, then the signal input hold time is negative with respect to the clock. Bit 6 through bit 4 define the hold time in nanoseconds (ns) and bits 3 through 0 define the signal input hold time in a tenth of a nanosecond.

B.2.36 Bytes 36 – 61: Superset Features (May be Used in the Future)

These bytes will be programmed with “zeroes” if not used.

B.2.37 Byte 62: Serial-Presence-Detect Revision

As the SPD definition is updated, it becomes necessary to identify the version of SPD that is being referred to. This TI specification follows JEDEC SPD specification revision 1. Table B–42 shows the definition for byte 62.

Table B–42. Byte-62 Definition

SPD REVISION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Initial release	0	0	0	0	0	0	0	0
Rev 1	0	0	0	0	0	0	0	1
Rev 2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:

B.2.38 Byte 63: Checksum for Bytes 0 – 62

The checksum calculation is as follows:

1. Convert binary information in byte locations 0 – 62 to decimal.
2. Add together (sum) all decimal values for byte locations 0 – 62.
3. Divide the sum by 256.
4. Convert the ramainder to binary (it will be < 256).
5. Store the single-byte result in address 63 as the checksum.

Example B–1. Checksum for Bytes 0–62

SPD BYTE ADDRESS	SERIAL PD			CONVERT TO DECIMAL	
0	0010 0100	——>		36	
1	1111 1110	——>	+	254	
2	0000 0000	——>	+	0	
3	0000 0000	——>	+	0	
.	. .	.		.	
.	. .	.		.	
60	0000 0000	——>	+	0	
61	0000 0000	——>	+	0	
62	0000 0000	——>	+	0	
				———	
				290	(Sum of all decimal values)
				290/256	(Divide by 256.)
				=1	With a remainder of 34
				34	(Keep remainder.)
				0010 0010	(Convert remainder to binary.)
63	0010 0010	<——		Store in byte location 63.	

B.2.39 Bytes 64–125: Manufacturer's Serial-Presence-Detect Format

See Appendix C.

B.2.40 Byte 126: Intel Specification Frequency

This byte, shown in Table B–43, defines the clock frequency of the Intel SDRAM DIMM.

Table B–43. Byte-126 Definition

INTEL SPECIFICATION FREQUENCY	HEX VALUE
66 MHz	66
100 MHz	64

B.2.41 Byte 127: Intel Specification Details for 100 MHz Support

This byte defines the SDRAM component and clock interconnection details for the DIMMs as defined:

Table B–44. Byte-127 Definition

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CLK0	CLK1	CLK2	CLK3	Junction Temp	CAS latency = 3	CAS latency = 2	Intel “Concurrent AP”
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

bit 7 = 1: CLK0 is connected on the DIMM
bit7 = 0: CLK0 is not connected on the DIMM
bit 6 = 1: CLK1 is connected on the DIMM
bit6 = 0: CLK1 is not connected on the DIMM
bit 5 = 1: CLK2 is connected on the DIMM
bit5 = 0: CLK2 is not connected on the DIMM
bit 4 = 1: CLK3 is connected on the DIMM
bit4 = 0: CLK3 is not connected on the DIMM
bit 3 = 1: 100° C junction temp
bit3 = 0: 90° C junction temp
bit2 and bit 1 = CL3 and CL2 support as shown:

PERFORMANCE GRADE	HEX VALUE (BITS 2 – 1)
CAS Latency 3	04
CAS Latency 3	06

bit 0 = 1: It supports Intel defined concurrent auto-precharge
bit0 = 0: It does not support Intel defined concurrent auto-precharge

Example B–2.

Byte 127 with the following encoding will imply:

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CLK0	CLK1	CLK2	CLK3	Junction Temp	CAS latency = 3	CAS latency = 2	Intel AP
1	0	1	0	0	1	1	1

This example defines a single-sided DIMM. CLK0 and CLK2 are connceted on the DIMM and there is a 90° C junction temp. The SDRAMs support CL = 2 and the Intel-defined concurrent auto-precharge.

Example B–3.

Byte 127 with the following encoding will imply:

BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
CLK0	CLK1	CLK2	CLK3	Junction Temp	CAS latency = 3	CAS latency = 2	Intel AP
1	1	1	1	1	1	1	1

This example defines a double-sided DIMM. CLK0, CLK1, CLK2, and CLK3 are all connected on the DIMM and there is a 100° C junction temp. The SDRAMs support CL = 2 and the Intel-defined concurrent auto-precharge.

B.2.42 Bytes 128–255: System Integrator's SPD Format

See Appendix C.

Appendix C Manufacturer's and System Integrator's Serial-Presence-Detect Format

C.1 Bytes 64–71 : Manufacturer's JEDEC ID Code (see W.E.G.7.2 per JEP-106-E)

The manufacturer's JEDEC ID code for Texas Instruments is 97h. The JEDEC ID code is entered first, and the remainer of the assigned bytes are filled with 0s, as shown in Table C–1.

Table C–1. Bytes 64–71 Definition

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Byte 64	1	0	0	1	0	1	1	1
Byte 65	0	0	0	0	0	0	0	0
Byte 66	0	0	0	0	0	0	0	0
Byte 67	0	0	0	0	0	0	0	0
Byte 68	0	0	0	0	0	0	0	0
Byte 69	0	0	0	0	0	0	0	0
Byte 70	0	0	0	0	0	0	0	0
Byte 71	0	0	0	0	0	0	0	0

C.2 Byte 72: Manufacturing Location

This byte, shown in Table C–2, is defined by the manufacturer.

Table C–2. Byte 72 Definition

MFG LOCATION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
SCI–SGP	0	0	0	0	0	0	0	1
EEMS	0	0	0	0	0	0	1	0
TBD	0	0	0	0	0	0	1	1

C.3 Bytes 73–90: Manufacturer's Part Number

The manufacturer's device part number must be coded in 8-bit ASCII. Unused spaces will be filled in with 20h (the hex number equivalent of "space"), as shown in Table C–3 and Table C–4.

Example: For TM2SR64EPU–12A, bytes 73–90 are programmed as:

544D32535236344550552D3132412020202

Table C–3. Bytes 73–81 Definition

	BYTE 73	BYTE 74	BYTE 75	BYTE 76	BYTE 77	BYTE 78	BYTE 79	BYTE 80	BYTE 81
ASCII	T	M	2	S	R	6	4	E	P
HEX	54	4D	32	53	52	36	34	45	50

Table C–4. Bytes 82–90 Definition

	BYTE 82	BYTE 83	BYTE 84	BYTE 85	BYTE 86	BYTE 87	BYTE 88	BYTE 89	BYTE 90
ASCII	U	–	1	2	A				
HEX	55	2D	31	32	41	20	20	20	20

C.4 Bytes 91–92: Revision Code

Byte 91, as shown in Table C–5, is for die (chip) revision code.

Table C–5. Byte-91 Definition

REVISION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
A	0	0	0	0	0	0	0	1
B	0	0	0	0	0	0	1	0
C	0	0	0	0	0	0	1	1

Byte 92, as shown in Table C–6, is for board revision code.

Table C–6. Byte-92 Definition

REVISION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
A	0	0	0	0	0	0	0	1
B	0	0	0	0	0	0	1	0
C	0	0	0	0	0	0	1	1

C.5 Bytes 93–94: Manufacturing Date

Bytes 93 and 94 are for the manufacturing date.

Byte 93, shown in Table C–7, is for the week.

Table C–7. Byte-93 Definition

WEEK	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
N/A	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:
:	:	:	:	:	:	:	:	:

Byte 94, shown in Table C–8, is for the year.

Table C–8. Byte-94 Definition

YEAR	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
N/A	0	0	0	0	0	0	0	0
1901	0	0	0	0	0	0	0	1
1902	0	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:	:
1996	0	1	1	0	0	0	0	0
1997	0	1	1	0	0	0	0	1
1998	0	1	1	0	0	0	1	0
:	:	:	:	:	:	:	:	:

C.6 Bytes 95–98: Assembly Serial Number

Each module has a unique number regardless of the module type.

- Byte 95 is a tester number (SCI = 64, TIS= 1–31, EEMS=32–63).
- Bytes 96–98 are a 24-bit serial number that starts at 0. The MSB of this serial number is bit 1 of Byte 96, and the LSB is bit 8 of Byte 98.

C.7 Bytes 99–125: Manufacturer's Specific Data (for Future Use)

These bytes are FF.

C.8 Bytes 128–255: System Integrator's Specific Data

These bytes are FF.

Appendix D EEPROM Component Specifications

The serial presence detect (SPD) device is contained in a 2K-bit serial EEPROM located on the module. The SPD nonvolatile EEPROM contains data such as module configuration, SDRAM organization, and timing parameters. Only the first 128 bytes are programmed by Texas Instruments; the remaining 128 bytes are available for customer use. Programming is performed through an IIC bus using the clock (SCL) and data (SDA) signals. All Texas Instruments modules comply with the current JEDEC SPD standard.

D.1 EEPROM Component Definition

Table D–1, Table D–2, Table D–3, and Table D–4 define various components of the SPD EEPROM.

Table D–1. EEPROM Component Absolute Maximum Ratings

PARAMETER	RANGE
All input or output Voltages with respect to ground	+4.6V to –0.3V
Ambient Storage Temperature	–40 ^{O}C to +100 ^{O}C

Table D–2. EEPROM Component Operating Conditions

PARAMETER	RANGE
Ambient Operating Temperature	0 ^{O}C to +70 ^{O}C
Positive Power Supply	3.0V to 3.6V

Table D–3. EEPROM Component A.C. and D.C. Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNITS
I_{CCA}	Active power supply current	f_{SCL} = 100 kHz		5.0	mA
I_{SB}	Standby current	V_{IN} = GND or V_{CC}		100	uA
I_{LI}	Input leakage current	V_{IN} = GND or V_{CC}		10	uA
I_{LO}	Output leakage current	V_{OUT} = GND to V_{CC}		10	uA
V_{IL}	Input low voltage		–0.3	V_{CC} X 0.3	V
V_{IH}	Input high voltage		V_{CC} X 0.7		V
V_{OL}	Output low voltage	I_{OL} = 3 ma		0.4	V

Table D–4. EEPROM Component A.C. Timing Parameters

SYMBOL	PARAMETER	MIN	MAX	UNITS
f_{SCL}	SCL clock frequency		80	kHz
T_I	Noise suppression time constant at SCL, SDA inputs		100	ns
t_{AA}	SCL low to SDA data out valid	0.3	7.0	us
t_{BUF}	Time the bus must be free before a new transmission can start	6.7		us
$t_{HD:STA}$	Start condition hold time	4.5		us
t_{LOW}	Clock low time	6.7		us
t_{HIGH}	Clock high time	4.5		us
$t_{SU:STA}$	Start condition setup time (for a repeated start condition)	6.7		us
$t_{HD:DAT}$	Data in hold time	0		us
$t_{SU:DAT}$	Data in setup time	500		ns
t_R	SDA and SCL rise time		1	us
t_F	SDA and SCL fall time		300	ns
$t_{SU:STO}$	Stop condition setup time	6.7		us
t_{DH}	Data out hold time	300		ns
t_{WR}	Write cycle time		15	ms

NOTE: Note: The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal erase/program cycle. During the write cycle, the EEPROM bus interface circuits are disabled, SDA remains high due to a pull-up resistor, and the EEPROM does not respond to its slave address.

D.2 EEPROM Component Illustration

The following drawings illustrate the EEPROM components.

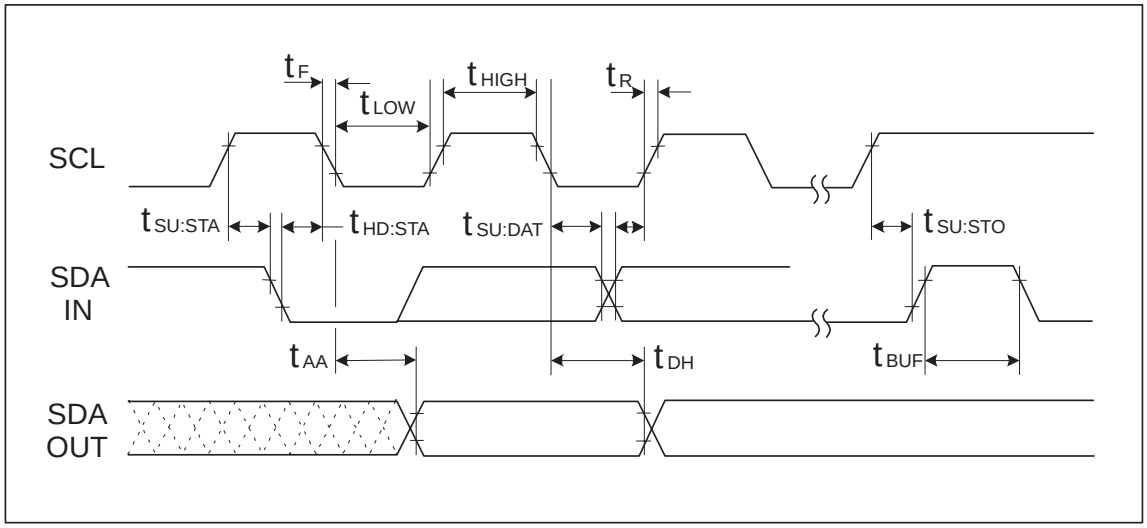

Figure D–1. EEPROM Component A.C. Timing Parameters

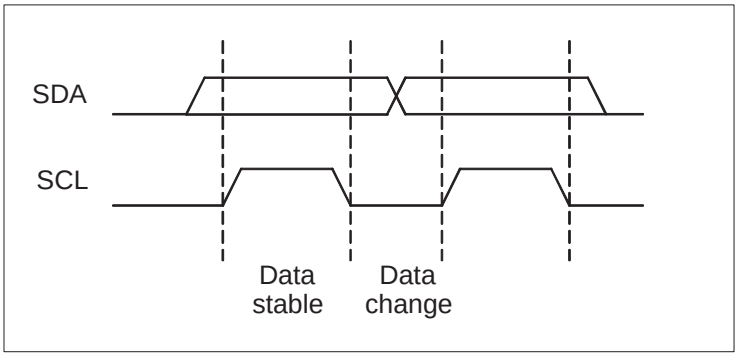

Figure D–2. EEPROM Data Validity

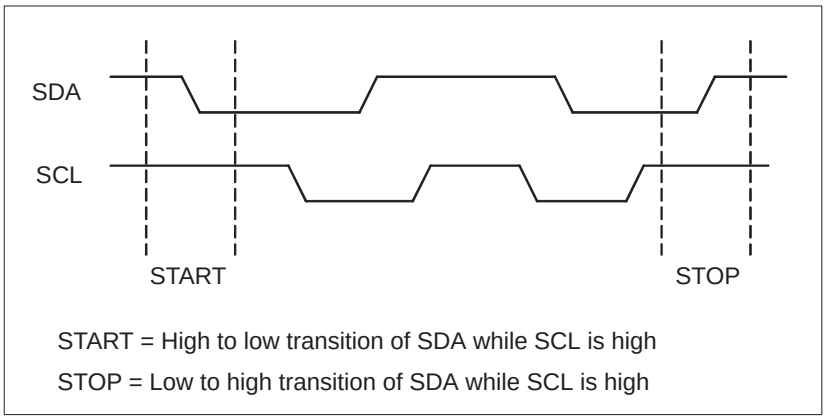

Figure D–3. EEPROM Start and Stop Conditions

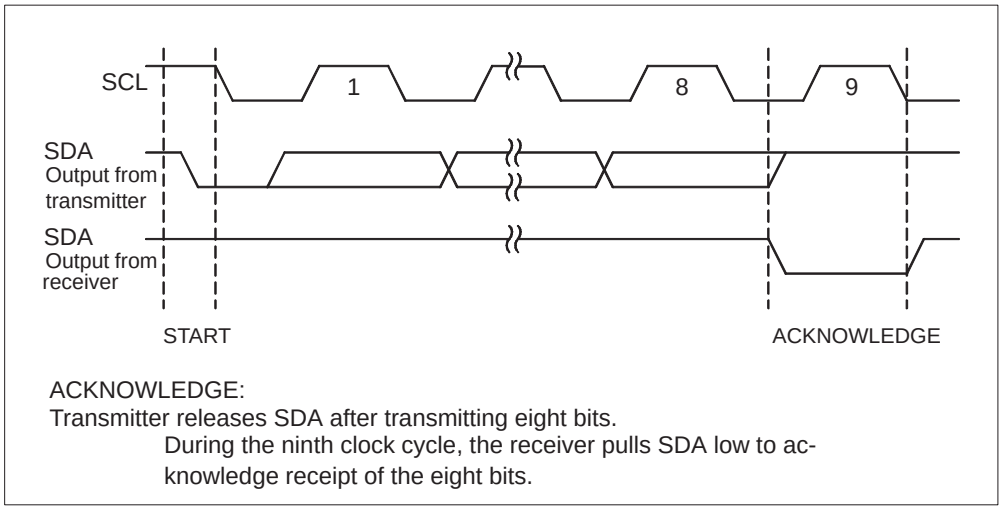

Figure D–4. EEPROM Acknowledge

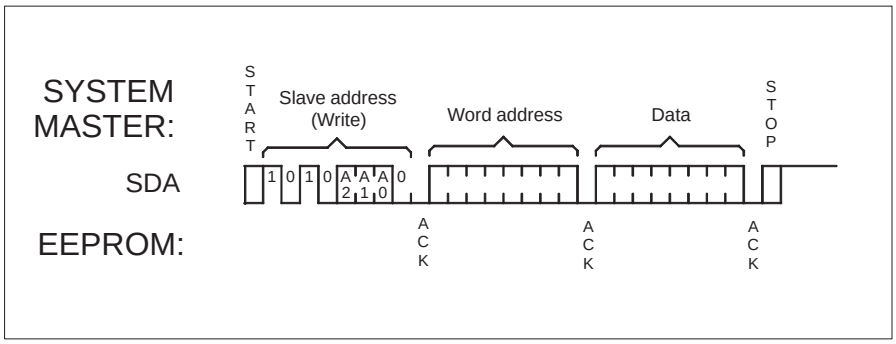

Figure D–5. EEPROM Byte Write Operation

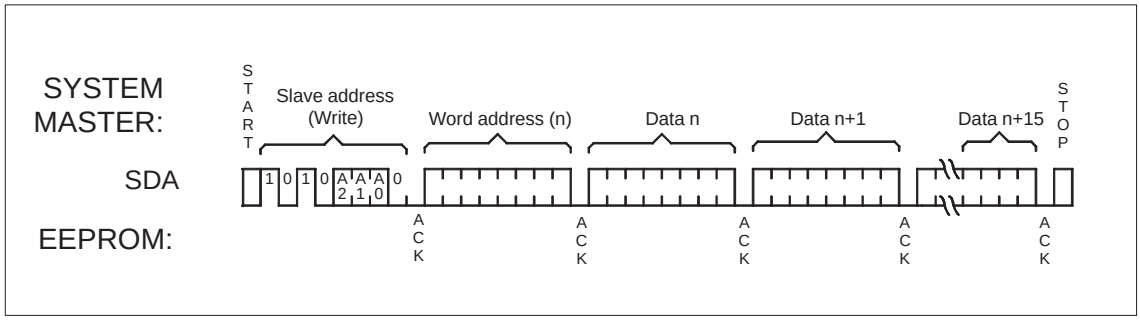

Figure D–6. EEPROM Page Write Operation

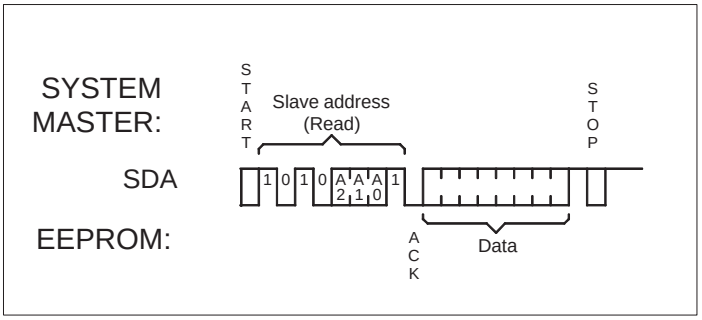

Figure D–7. EEPROM Current Address Read Operation

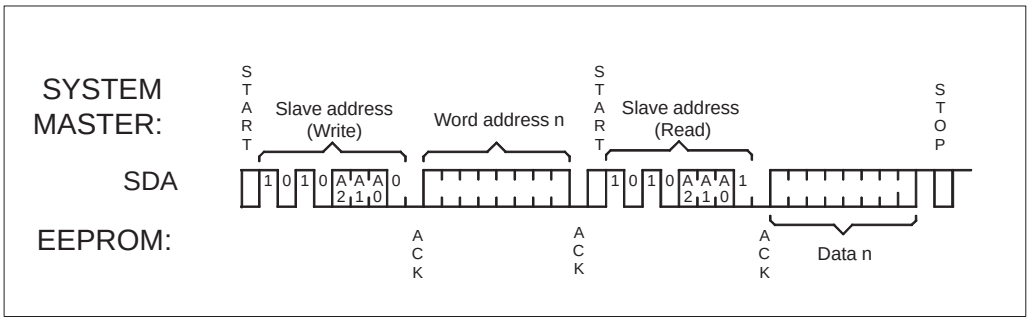

Figure D–8. EEPROM Random Read Operation

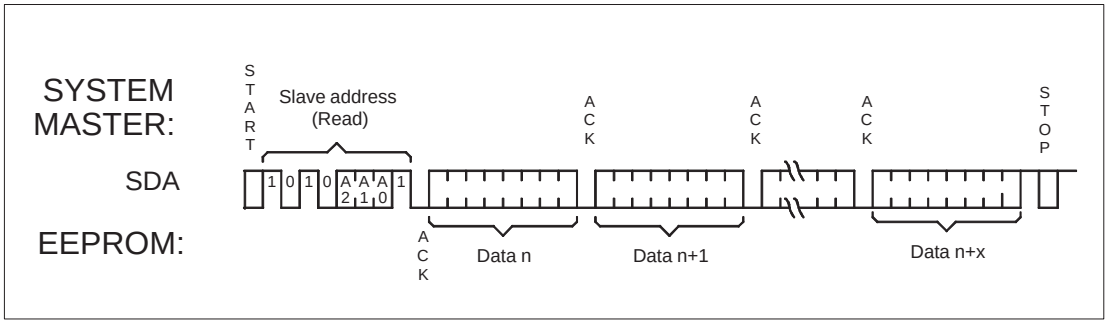

Figure D–9. EEPROM Sequential Read Operation

D.3 Example of SPD

Table D–5 shows an example of serial presence detect.

Table D–5. SDRAM DIMM Module TM2SR64EPU–12A

BYTE NUMBER	FUNCTION	VALUE	EEPROM CONTENTS
0	Defines number of bytes written into serial memory at module mfg.	128 bytes	80h
1	Total number of bytes of SPD memory device	256 bytes	08h
2	Fundamental memory type SDRAM	SDRAM	04h
3	Number of row addresses on this assembly	11	0Bh
4	Number of column addresses on this assembly	9	09h
5	Number of module banks on this assembly	1 bank	01h
6	Data width of this assembly…	64 bits	40h
7	… Data width continuation		00h
8	Voltage interface standard of this assembly	LVTTL	01h
9	SDRAM cycle time at maximum supported CAS latency (CL), CL=X (CL=3)	t_{CK}=12ns	C0h
10	SDRAM access from clock (CL=3)	t_{AC}=9ns	90h
11	Module configuration type (nonparity, parity, error-correcting code [ECC])	Nonparity	0h
12	Refresh rate/type	15.6us/self-refresh	80h
13	SDRAM width, primary SDRAM	x8	08h
14	Error-checking SDRAM data width	n/a	00h
15	Minimum clock delay, back-to-back random column addresses	1 clk cycle	01h
16	Burst lengths supported	1,2,4,8	0Fh
17	Number of banks on each SDRAM device	2 banks	02h
18	CAS number latency†	2,3	06h
19	CS number latency	0	01h
20	Write latency	0	01h
21	SDRAM module attributes	Nonbuffered/ nonregistered	00h
22	General SDRAM device attributes	Vcc tol. =(+10%)/(–5%), burst read, single-bit write, precharge all, autoprecharge	1Eh

† Read latency = 1 is not supported.

Table D–5. SDRAM DIMM Module TM2SR64EPU–12A (Continued)

BYTE NUMBER	FUNCTION	VALUE	EEPROM CONTENTS
23	Minimum clock cycle time at CL X–1 (CL=2)	t_{CK}=15ns	F0h
24	Maximum data access time from clock at CL X–1 (CL=2)	t_{AC}=9ns	90h
25	Minimum clock cycle time at CL X–2 (CL=1)†	–	00h
26	Maximum data access time from clock at CL X–2 (CL=1)†	–	00h
27	Minimum row precharge time	t_{RP}=30ns	1Eh
28	Minimum row-active-to-row-active delay	t_{RRD}=24ns	18h
29	Minimum RAS-to-CAS delay	t_{RCD}=30ns	1Eh
30	Minimum RAS pulse width	t_{RAS}=60ns	3Ch
31	Module bank density	16MB	04h
32–61	Superset features (may be used in the future)	N/A	00h
62	SPD revision designator	1	01h
63	Checksum for bytes 0–62	7	07h
64–71	Manufacturer’s JEDEC ID code per JEP–106E	97h	9700...00h
72	Manufacturing location	SCI–SGP	01h
73–90	Manufacturer’s part number	TM2SR64EPU–12A	544D3253523 6344550552D 31324120202 020
91	Die revision code	Rev A	01h
92	PCB revision code	Rev A	01h
93	Manufacturing week of the year	Example: fifth week of the year	05h
94	Manufacturing year	1997	61h
95–98	Assembly serial number	Unique number	MFG Data
99–125	Manufacturer-specific data	N/A	FFh
126–127	Vender specific	N/A	FFh

† Read latency = 1 is not supported.