LM48580 Evaluation Module

This user's guide describes the characteristics, operation, and use of the LM48580 Evaluation Module (EVM). A complete schematic diagram, printed-circuit board layouts, and bill of materials (BOM) are included in this document.

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Trademarks

1 Introduction

To help the user investigate and evaluate the LM48580 performance and capabilities, a fully-populated demonstration board was created. Figure 1 shows the board.

Connected to an external power supply (2.5 V ≤ V_{DD} ≤ 5.5 V) and a signal source, the LM48580 demonstration board easily exercises features of the amplifier.

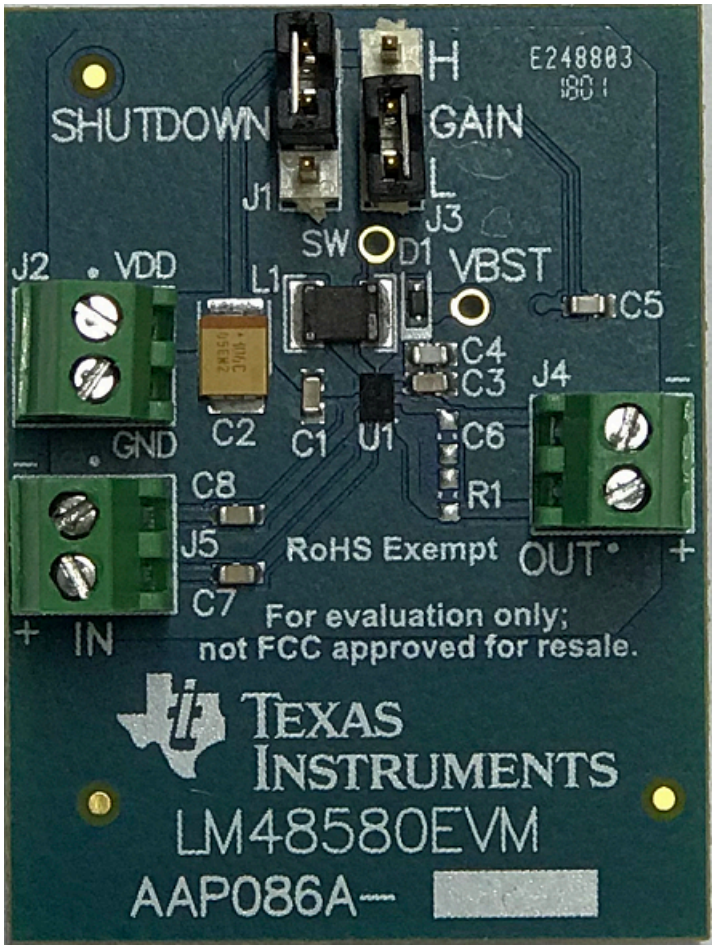

Figure 1. LM48580 Demonstration Board

2 Quick Start Guide

Use the following steps to set up the EVM board in hardware mode:

1. Short pins 1 (VDD) and 2 of J1 for normal operation.
2. Short pins 1 (VDD) and 2 on J3 to set the GAIN to 30 dB.
3. Connect the load across OUT+ and OUT–.
4. Connect a power supply (2.5 V to 5.5 V) and ground reference, respectively, to the VDD and GND headers on the demo board.
5. Connect a differential audio input to IN+ and IN–.
6. Power on the board and observe the output on OUT+ and OUT–.

3 General Description

The LM48580 is a high-voltage, high-efficiency, Class H driver for ceramic speakers and piezo actuators. The Class H architecture of the LM48580 offers significant power savings compared to traditional Class AB amplifiers. The device provides 30 V_{PP} output drive while consuming only 2.7 mA of quiescent current from a 3.6-V supply.

The LM48580 features one fully-differential input, a programmable gain pin, and a shutdown pin. The gain pin has three settings for 18 dB, 24 dB, and 30 dB. The LM48580 has a low power shutdown mode that reduces quiescent current consumption to 0.5 μA.

4 Operating Conditions

Table 1 lists the temperature range and supply voltage conditions for the EVM.

Table 1. Operating Conditions

Temperature Range: $T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le 85°C$
Supply Voltage (V_{DD})	$2.5\ V \le V_{DD} \le 5.5\ V$

5 Application Circuit Schematic

Figure 2 shows the demonstration board schematic.

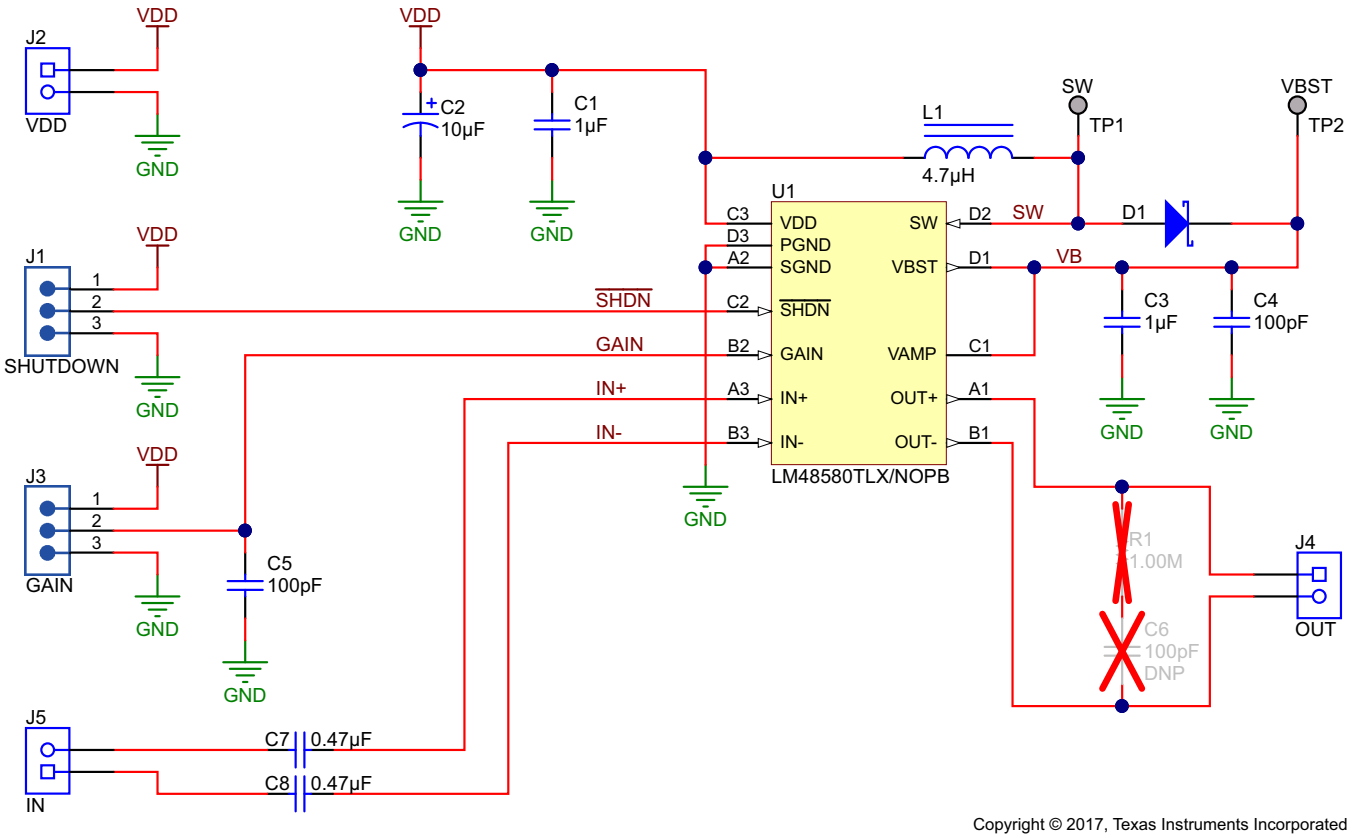

Figure 2. Demonstration Board Schematic

6 Connections

Table 2 lists the connections on the EVM board.

Table 2. Connections

Designator	Function	Notes
J1	Shutdown	Active Low Shutdown. Drive SHDN low to disable the device. Connect SHDN to VDD for normal operation.
J2	VDD/GND	Power supply and ground reference.
J3	GAIN	Gain select: GAIN = float: AV = 18 dB GAIN = GND: AV = 24 dB GAIN = VDD: AV = 30 dB
J4	OUT±	Positive and negative output terminals.
J5	IN±	Positive and negative input terminals.

7 PCB Layout Guidelines

Minimize trace impedance of the power, ground and all output traces for optimum performance. Voltage loss due to trace resistance between the LM48580 and the load results in decreased output power and efficiency. Trace resistance between the power supply and ground has the same effect as a poorly regulated supply: increased ripple and reduced peak output power. Use wide traces for power supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as route heat away from the device. Proper grounding improves audio performance, minimizes crosstalk between channels and prevents switching noise from interfering with the audio signal. Use of power and ground planes is recommended.

8 Bill Of Materials

Table 3 lists the bill of materials for the EVM.

Table 3. LM48580 Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer	Alternate Part Number	Alternate Manufacturer
PCB	1		Printed Circuit Board		AAP086	Any	–	–
C1, C3	2	1 µF	Capacitor, ceramic, 1 µF, 16 V, ±10%, X7R, 0603	0603	GRM188R71C105KE15D	MuRata		
C2	1	10 µF	Capacitor, TA, 10 µF, 16 V, ±10%, 0.8 Ω, SMD	3528-21	TPSB106K016R0800	AVX		
C4, C5	2	100 pF	Capacitor, ceramic, 100 pF, 50 V, ±5%, C0G/NP0, 0603	0603	GRM1885C1H101JA01D	MuRata		
C7, C8	2	0.47 µF	Capacitor, ceramic, 0.47 µF, 10 V, ±10%, X5R, 0603	0603	GRM188R61A474KA61D	MuRata		
D1	1	20 V	Diode, Schottky, 20 V, 0.5 A, AEC-Q101, SOD-523	SOD-523	NSR0520V2T1G	ON Semiconductor		
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 × 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M		
J1, J3	2		Header, 100 mil, 3 × 1, Gold, TH	PBC03SAAN	PBC03SAAN	Sullins Connector Solutions		
J2, J4, J5	3		Terminal Block, 2 × 1, 2.54 mm, TH	Terminal Block, 2 × 1, 2.54 mm, TH	282834-2	TE Connectivity		
L1	1	4.7 µH	Inductor, Wirewound, 4.7 µH, 1 A, 0.216 Ω, SMD	1210	BRL3225T4R7M	Taiyo Yuden		
SH1, SH2	2	1 × 2	Shunt, 100 mil, Gold plated, Black	Shunt	969102-0000-DA	3M	SNT-100-BK-G	Samtec
U1	1		High Efficiency Class H, High Voltage, Haptic Piezo Actuator / Ceramic Speaker Driver, 12-pin Micro SMD, Pb-Free	TLA12Z1A	LM48580TLX/NOPB	Texas Instruments		
C6	0	100 pF	Capacitor, ceramic, 100 pF, 50 V, ±5%, C0G/NP0, 0603	0603	GRM1885C1H101JA01D	MuRata		
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A		
R1	0	1.00 Meg	RES, 1.00 M, 1%, 0.1 W, 0603	0603	RC0603FR-071ML	Yageo America		

9 Demonstration Board PCB Layout

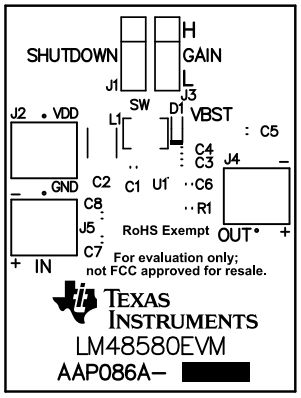

Figure 3. Top Overlay

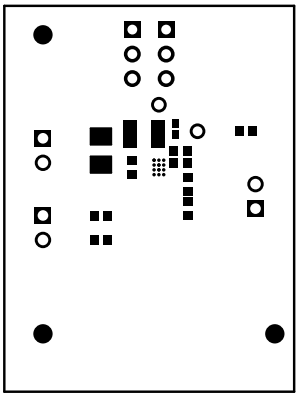

Figure 4. Top Solder Mask

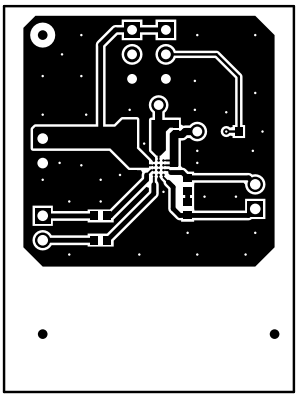

Figure 5. Top Layer

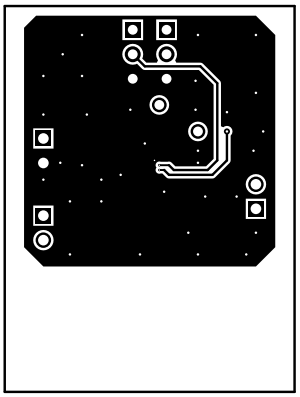

Figure 6. Bottom Layer

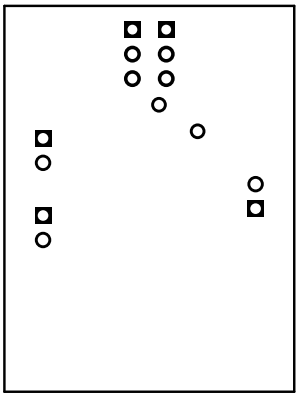

Figure 7. Bottom Solder Mask

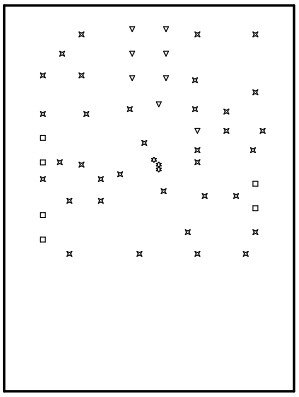

Figure 8. Drill Drawing

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Date	Revision	Description
February 2018	*	Initial Release

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