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3.125 Gbps 1:4 LVDS Buffer/Repeater with Transmit Pre-emphasis and Receive Equalization

DS25BR204 Evaluation Kit

USER MANUAL

Part Number: DS25BR204EVK NOPB

For the latest documents concerning these products and evaluation kit, visit lvds.national.com.
Schematics and gerber files are also available at lvds.national.com.

December 2007
Rev. 0.1

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Overview

The DS25BR204EVK is an evaluation kit designed for demonstrating performance of the DS25BR204, a 3.125 Gbps 1:4 LVDS Buffer/Repeater with transmit pre-emphasis and receive equalization. The evaluation kit is comprised of the DS25BR204 with its associated input and output SMA connectors and jumpers to manually configure the switch. In addition, the EVK features three FR4 striplines (15 (~38), 30 (~76) and 60 (~152) inches (cm) in length) for exercising device's signal conditioning features (pre-emphasis and equalization).

The purpose of this document is to familiarize the user with the DS25BR204EVK, to suggest test setup procedures and instrumentation to test the device optimally, and to guide the user through some typical measurements that demonstrate the performance of the DS25BR204 in typical applications.

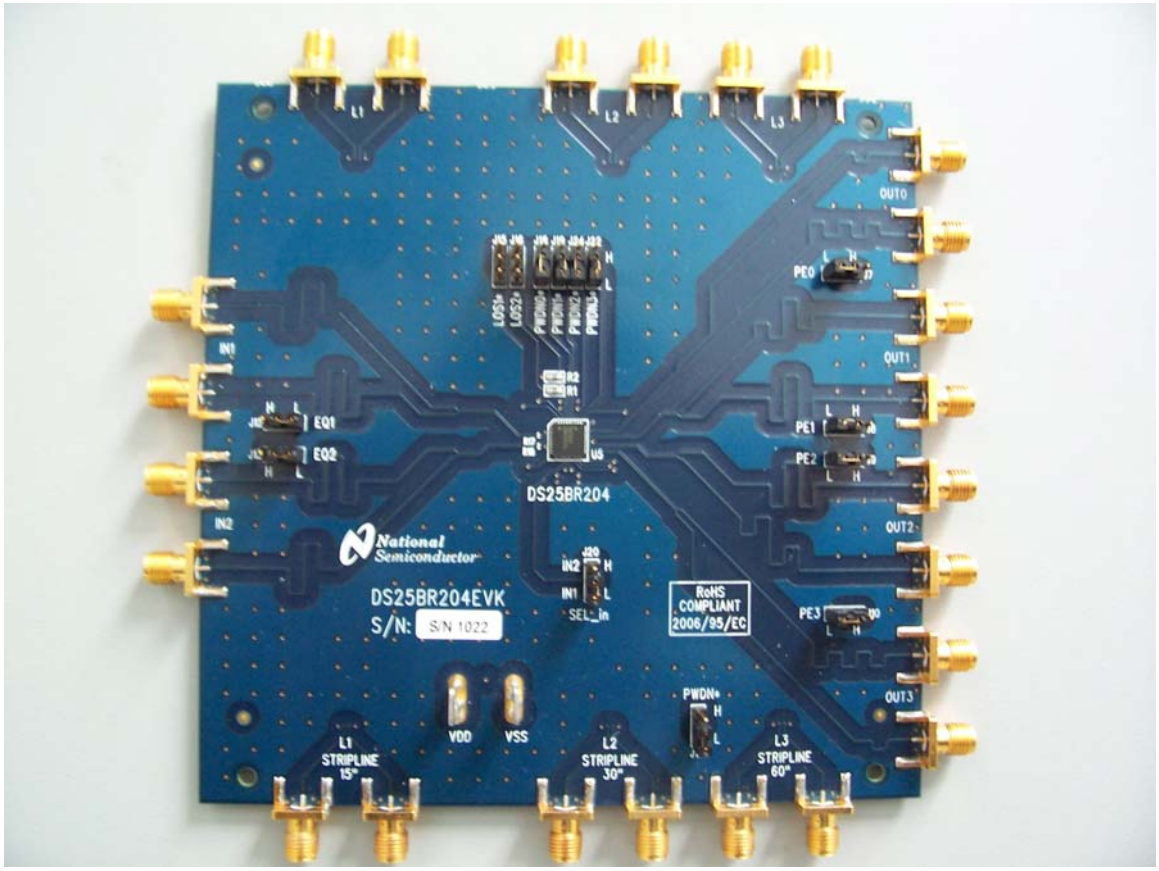


Figure 1. Photo of the DS25BR204EVK

Description

Figure 2 shows the top layer drawing of the PCB with the silkscreen annotations. The 5.25 by 5.25 inch, eight-layer PCB is designed to evaluate the functions of the DS25BR204.

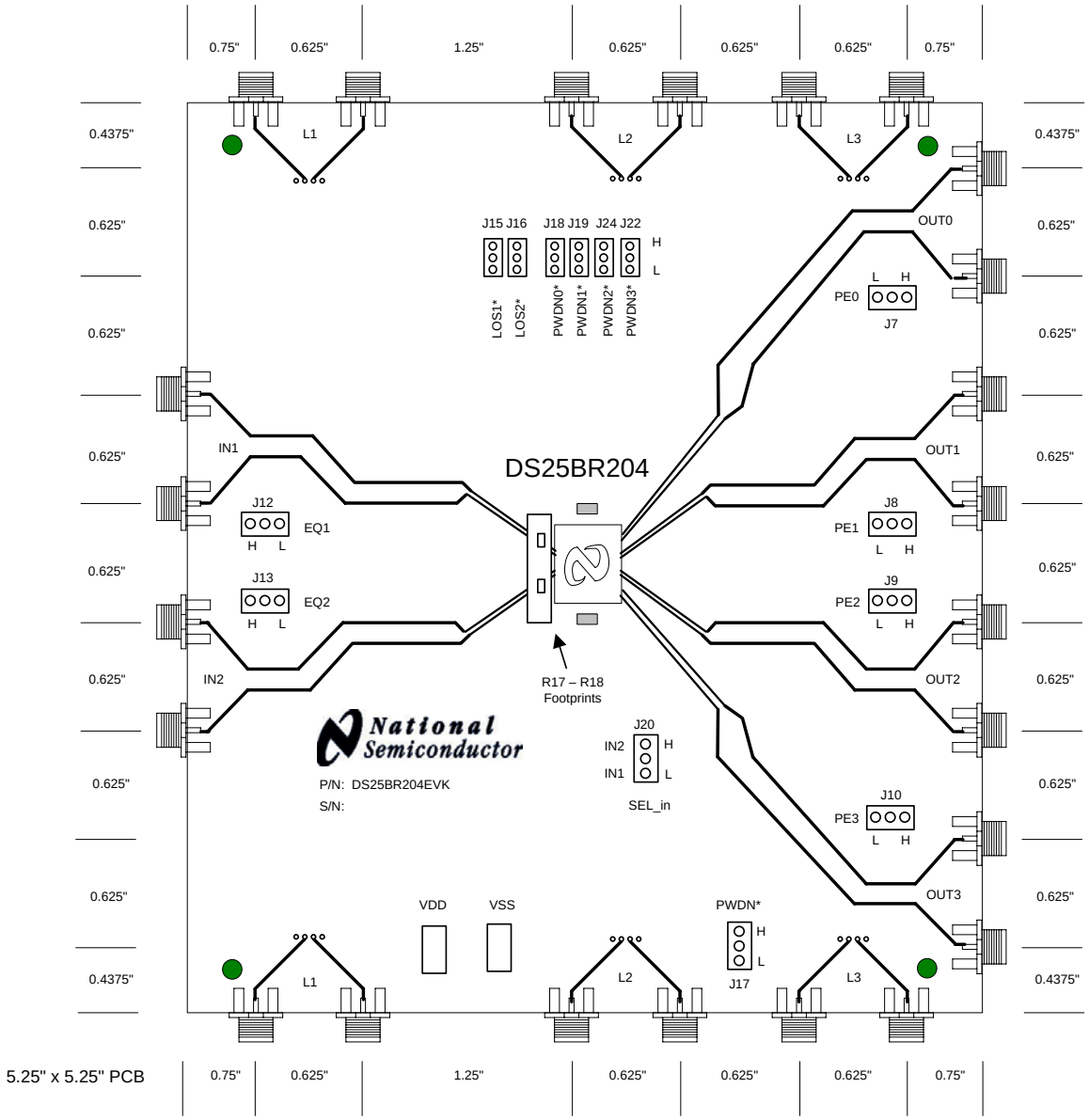


Figure 2. Top Layer DS25BR204EVK

Evaluation

This section provides recommended test setup procedure for the device evaluation. Figure 3 depicts a typical setup and instrumentation you may use for the device evaluation.

1. Configure the test setup as shown in Figure 3.
2. Select a desired input using J20.
3. Power up the device and desired output(s) using the J18, J19, J20, J22 and J24.
4. Apply + supply (3.3V typical) to the VDD and – supply (ground) to the VSS connectors.
5. Set desired pre-emphasis and/or equalization levels according to Tables 1 and 2.
6. Connect a signal source (signal generator, data source, or an LVDS driver) to the desired INn inputs on the board and adjust the signal parameters (VOH, VOL, VCM) so that they comply with the device input recommendations.
7. Connect an oscilloscope to the selected OUTn outputs and view the output signals with an oscilloscope with the analog bandwidth of at least 5 GHz.

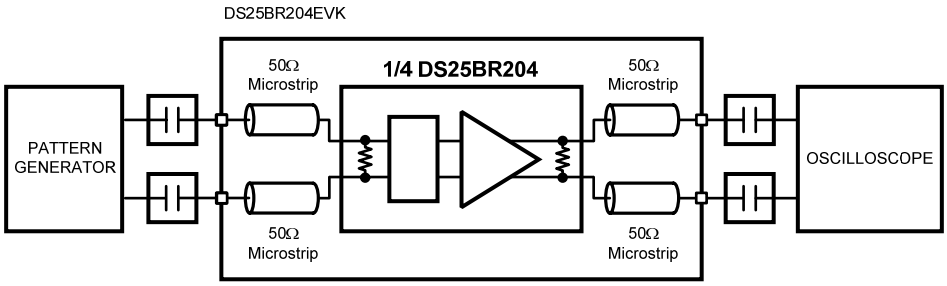


Figure 3. DS25BR204 Test Setup Example

Truth Tables

OUTPUT OUTn, n = {0, 1, 2, 3}	
CONTROL Pin PEn (J7, J8, J9, J10) State	**Pre-emphasis Level**
L	OFF
H	ON

Table 1. Transmit Pre-emphasis Truth Table

INPUT INn, n = {1, 2}	
CONTROL Pin EQn (J12, J13) State	**Pre-emphasis Level**
L	OFF
H	ON

Table 2. Receive Equalization Truth Table

Typical Performance

This section of the User Manual shows a typical eye diagram you can expect to see when evaluating the DS25BR204EVK.

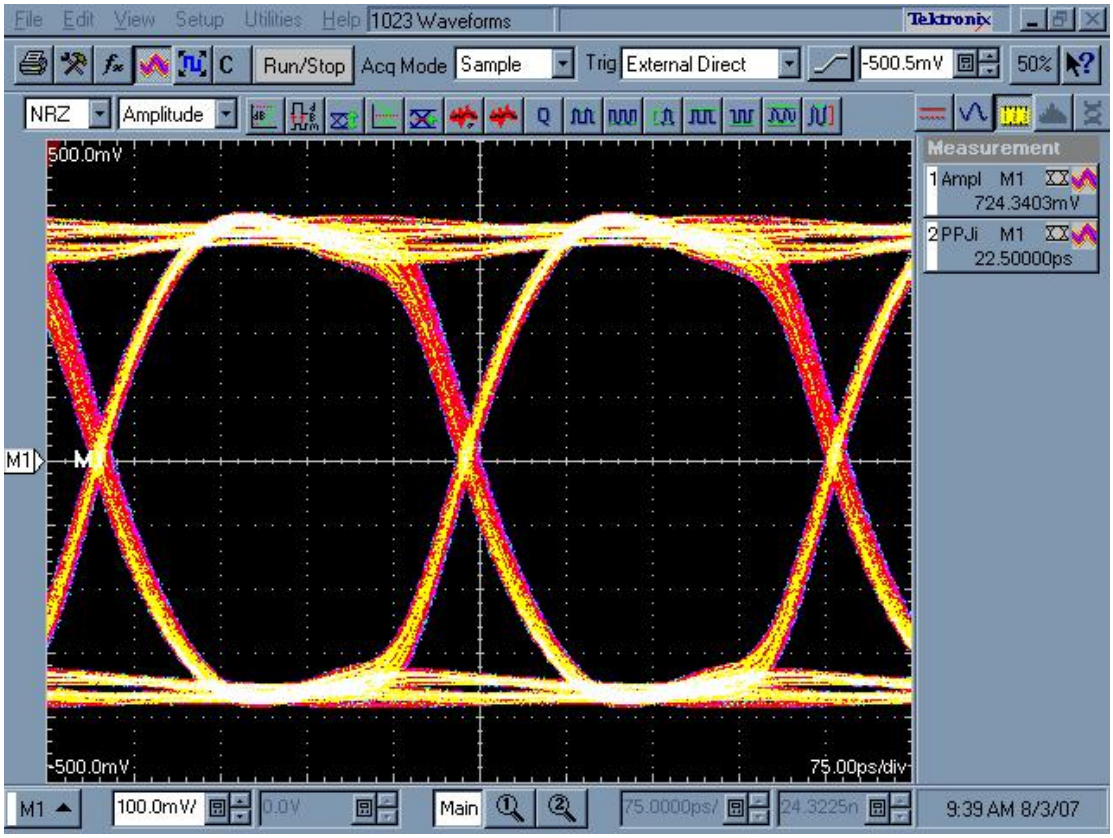
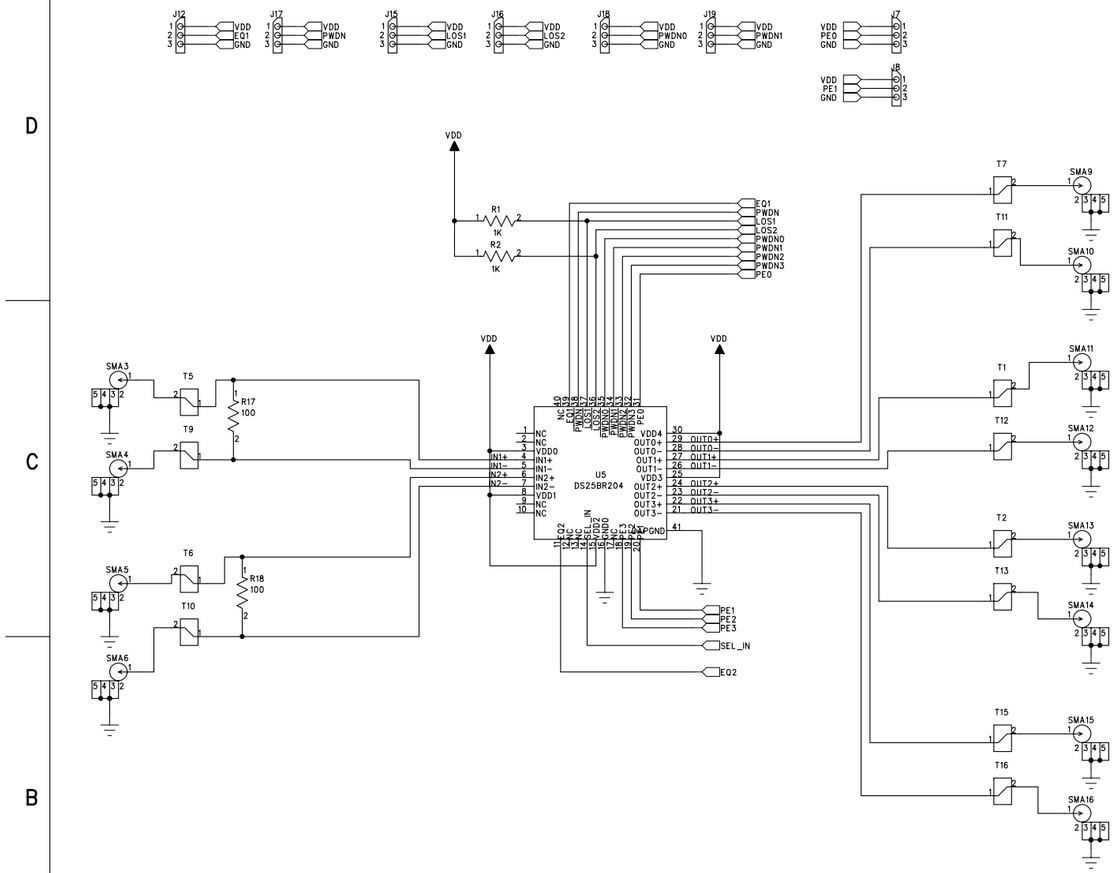
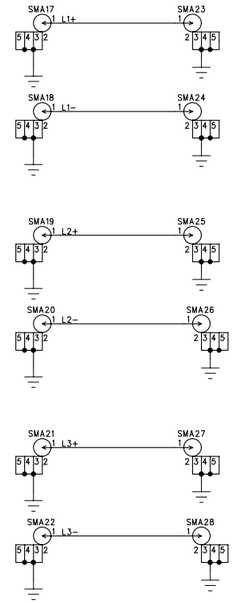
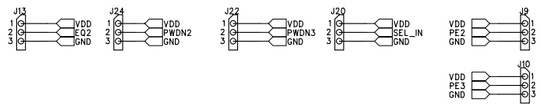


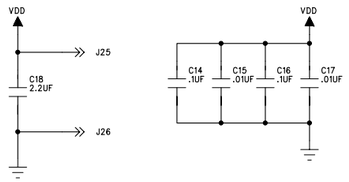
Figure 4. DS25BR204 3.125 Gbps NRZ PRBS-7 Output Eye Diagram

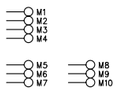
REVISION RECORD			
LTR:	ECO NO:	APPROVED:	DATE:
0	INITIAL RELEASE		











COMPANY:	NATIONAL SEMICONDUCTOR		
TITLE:	SCHEMATIC DS25BR204EVK		
CODE:	SIZE: C	DRAWING NO: S-06298	REV: 0
DRAWN: ACF	DATED: 10/3/07	SCALE:	

Enercon Technologies
25 NorthBrook Drive
Gray, Maine 04039
U.S.A.

ENERCON - BILL OF MATERIALS

TITLE: **NATIONAL SEMICONDUCTOR PCBA, DS25BR204EVK, ROHS DS25BR204EVK**

Main Product: PCBA, DS25BR204 EVK, ROHS

PL Number:	Rev:	Rev By:	Rev Date:	PL Status:
Z3199-01	1	BJ	10/18/2007	Released

Responsible Eng/Mgr:	Creator:	Creation Date:
	Arlene Fox	10/5/2007

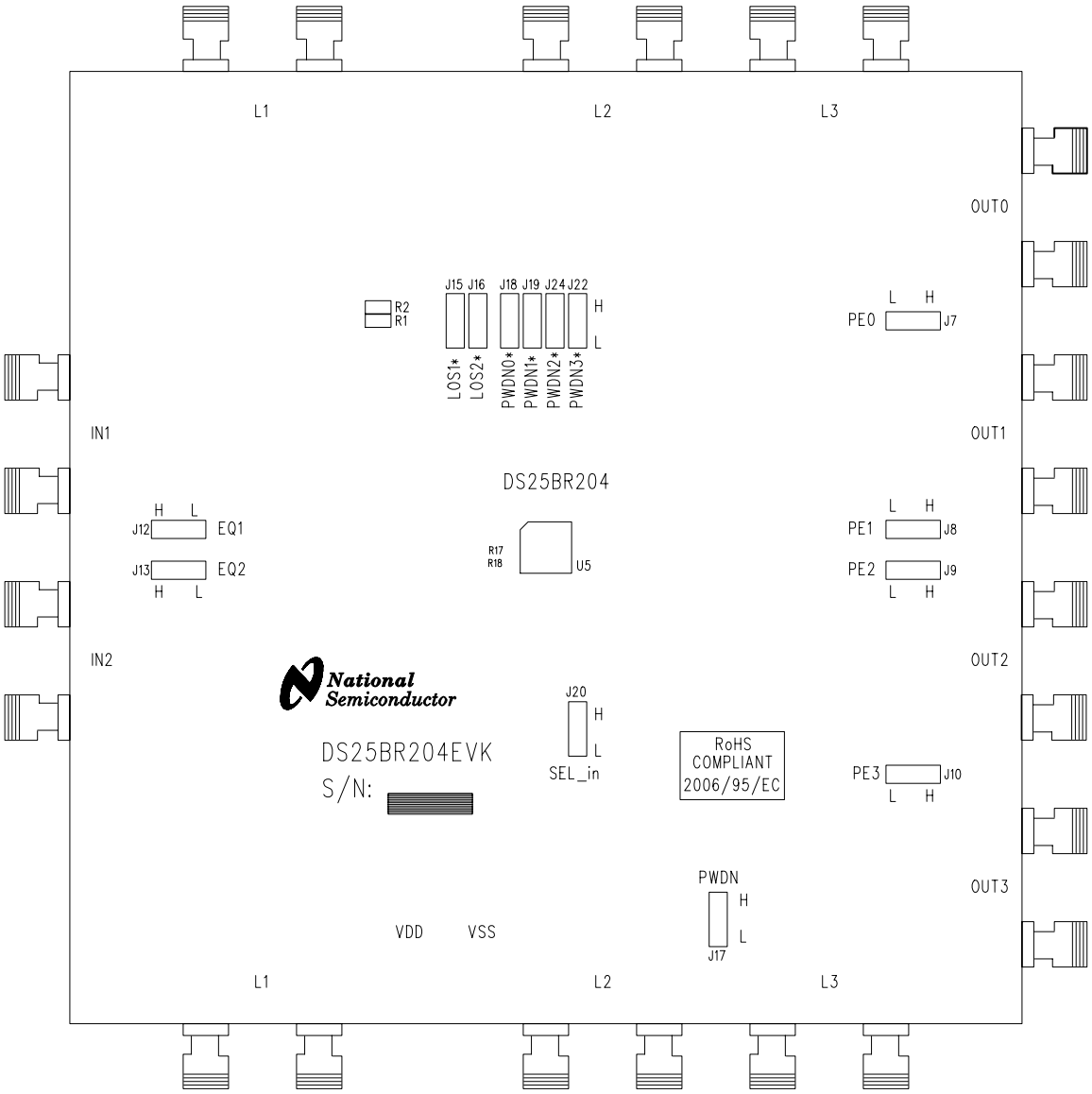
Item	Part Type	Part Number/Value	Mfg	NoSub	Description	Qty	SMT	Ref Des	Notes	Rev
1	PCB	P-06299R0	ENERCON		DS25BR204: 5.25x5.25x.060in, 8 layer	1			Bd: (133.35x 133.35mm) Panel: (10.60x5.25in) (269.24x 133.35mm) 2 bds/panel	0
2										
3	IC	DS25BR204TSQ/NOPB	NAT		LVDS Repeater, LLP40, Pb-Free	1	X	U5	Customer Supplied	0
4										
5	RES	ERJ-3GEYJ102	PANA		1K 1/10W ±5% 0603 200ppm, Pb-Free	2	X	R1-2		0
	<ALT>	CRCW06031K00JNEA	VISHAY		1K 1/10W ±5% 0603 200ppm, Pb-Free					
	<ALT>	RK73B1JTTD102J	KOA		1K 1/10W ±5% 0603 200ppm, Pb-Free					
6										
7	CAP	0402YC103KAT	AVX		.01µF, 16V, ±10%, 0402, Ceramic, X7R, Pb-Free	2	X	C15,17		0
	<ALT>	C0402C103K4RAC	KEMET		.01µF, 16V, ±10%, 0402, Ceramic, X7R, Pb-Free					
	<ALT>	ECJ-0EB1C103K	PANA		.01µF, 16V, ±10%, 0402, Ceramic, X7R, Pb-Free					
8	CAP	C0402C104K8RAC	KEMET		.1µF, 10V, ±10%, 0402, Ceramic, X7R, Pb-Free	2	X	C14,16		0
9	CAP	C1206C225K4RAC	KEMET		2.2µF, 16V, ±10%, 1206, Ceramic, X7R, Pb-Free	1	X	C18		0
	<ALT>	ECJ-3YB1C225K	PANA		2.2µF, 16V, ±10%, 1206, Ceramic, X7R, Pb-Free					
10										
11	CONN	1287-ST	KEYSTONE		Faston, Male, .250x.032, Pb-Free	2		J25-26		0
12	CONN	142-0701-851	EMERSON		SMA, Jack Receptacle, 50 OHM, Pb-Free	24		SMA3-6,9-28		0
13	CONN	SNT-100-BK-G	SAMTEC		Shunt, .100"sp, Gold, Pb-Free	14			Use with J7-10,12-13,15-20,22,24 Pins 2&3	0
	<ALT>	SNT-100-BK-H	SAMTEC		Shunt, .100"sp, Gold, Pb-Free					

ENERCON - BILL OF MATERIALS	TITLE:	PL Number:	Rev:	Rev By:	Rev Date:	PL Status:
Main Product: PCBA, DS25BR204 EVK, ROHS	NATIONAL SEMICONDUCTOR PCBA, DS25BR204EVK, ROHS DS25BR204EVK	Z3199-01	1	BJ	10/18/2007	Released
		Responsible Eng/Mgr:	Creator: Arlene Fox		Creation Date: 10/5/2007	

Item	Part Type	Part Number/Value	Mfg	NoSub	Description	Qty	SMT	Ref Des	Notes	Rev
14	CONN	TSW-103-07-G-S	SAMTEC		Header, 3p, Male, .100"sp, Gold, Pb-Free	14		J7-10,12-13,15-20,22,24		0
15										
16	STENCL	T-06302R0	ENERCON		STENCIL FABRICATION TOP, DS25BR204EVK	1				0
17	STENCL	T-06303R0	ENERCON		STENCIL FABRICATION BOTTOM, DS25BR204EVK	1				0
18										
19	REF	C-06300R0	ENERCON		FABRICATION DWG, DS25BR204EVK					0
20	REF	C-06301R0	ENERCON		PALLET DWG, DS25BR204EVK					0
21	REF	S-06298R0	ENERCON		SCHEMATIC, DS25BR204EVK					0
22										
23										
24										

Notes:

DO NOT STUFF
R17,18


L1
L2
L3
OUT0
OUT1
OUT2
OUT3
IN1
IN2
R2
R1
J15 J16 J18 J19 J24 J22
H
L
LOS1*
LOS2*
PWDN0*
PWDN1*
PWDN2*
PWDN3*
L H
PE0 J7
DS25BR204
H L
J12 EQ1
J13 EQ2
H L
R17
R18
U5
L H
PE1 J8
PE2 J9
L H
National Semiconductor
DS25BR204EVK
S/N:
J20
H
L
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COMPLIANT
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L H
PWDN
H
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J17
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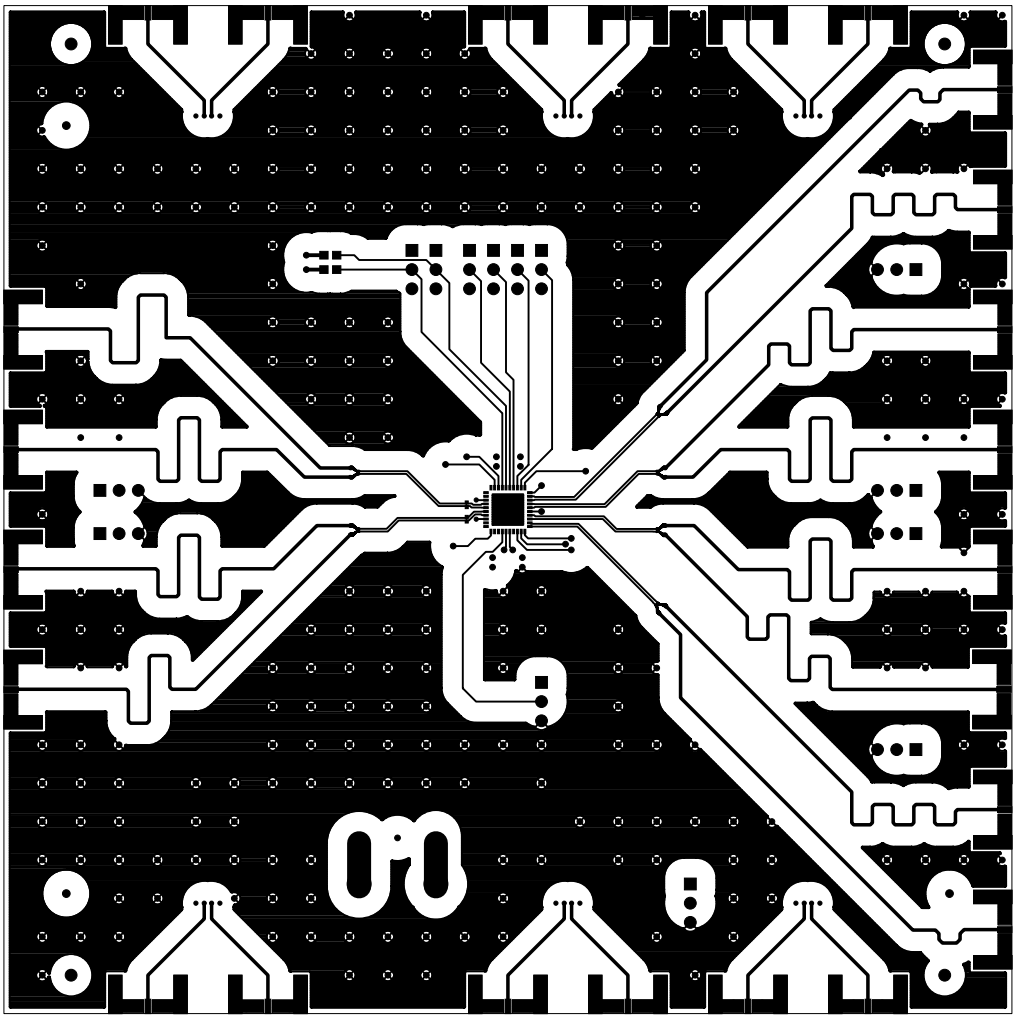
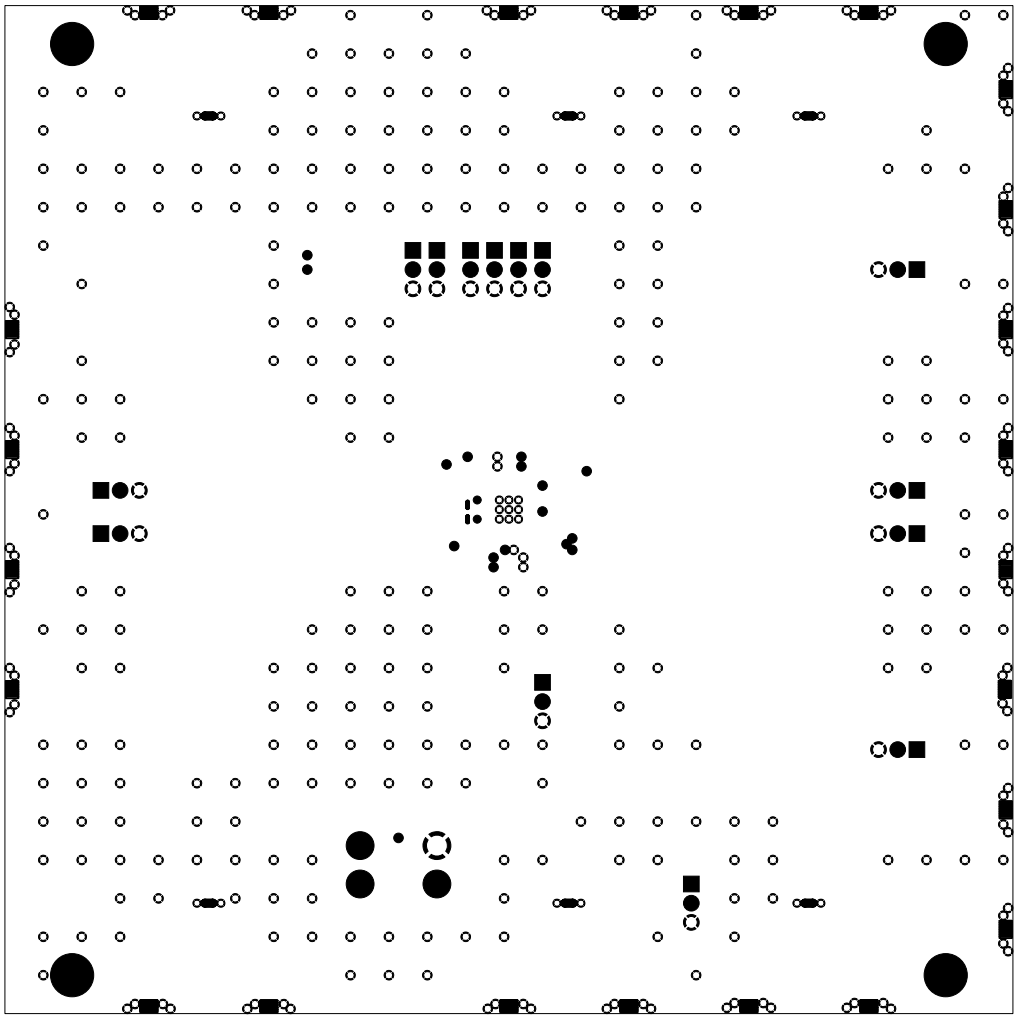
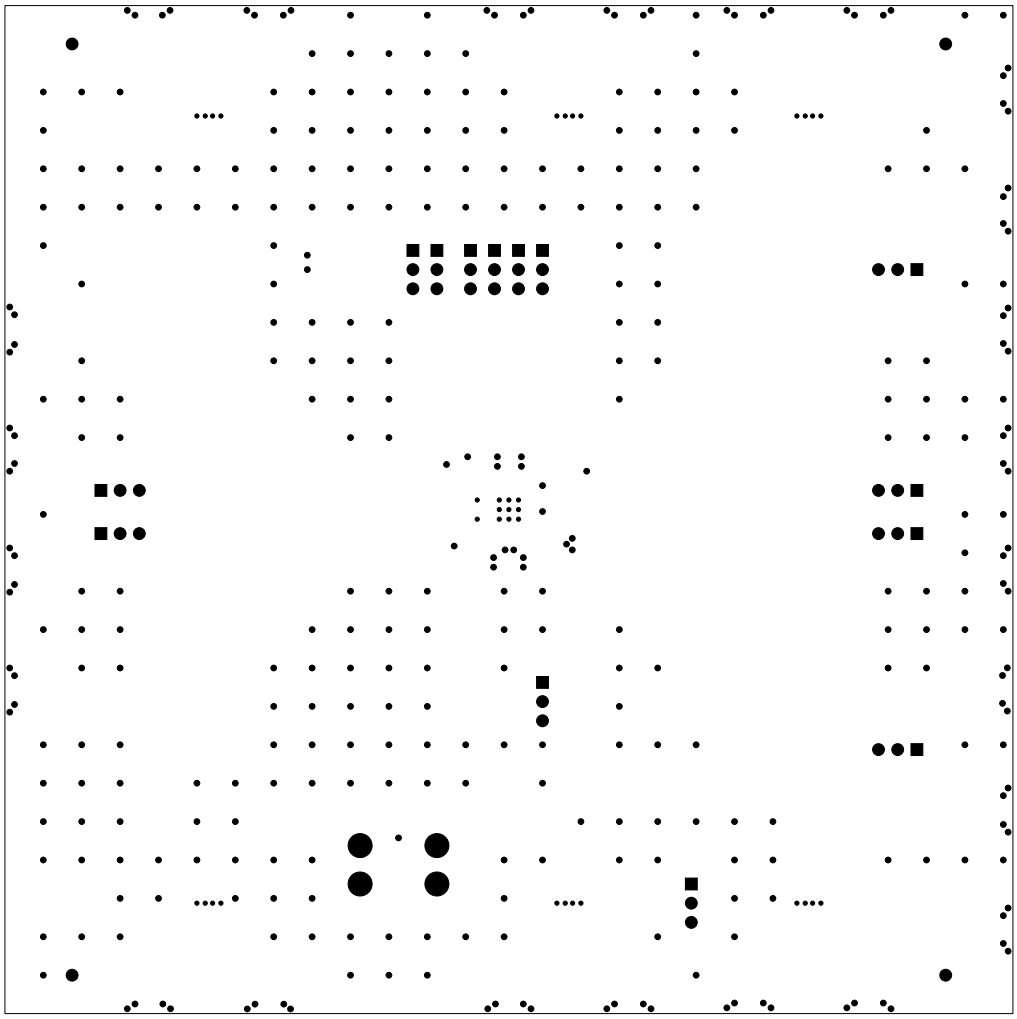
VSS

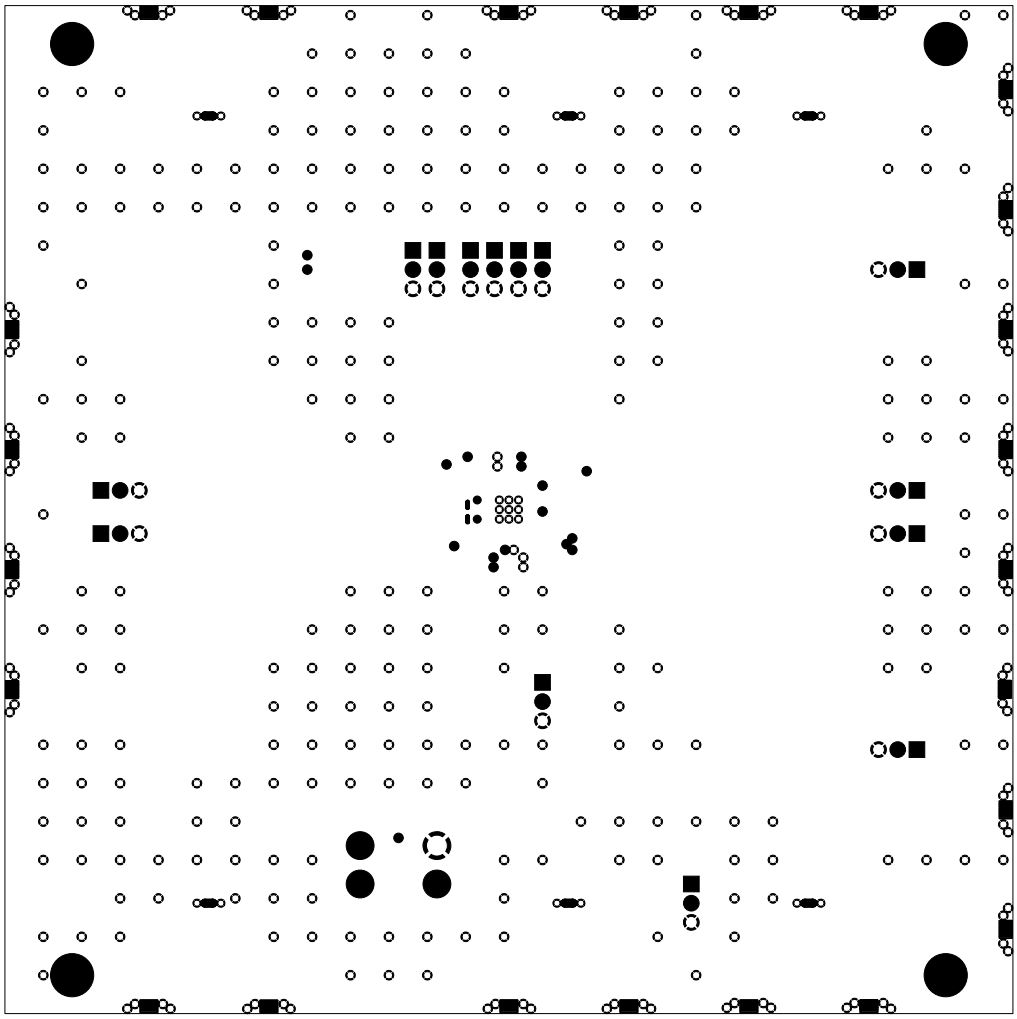




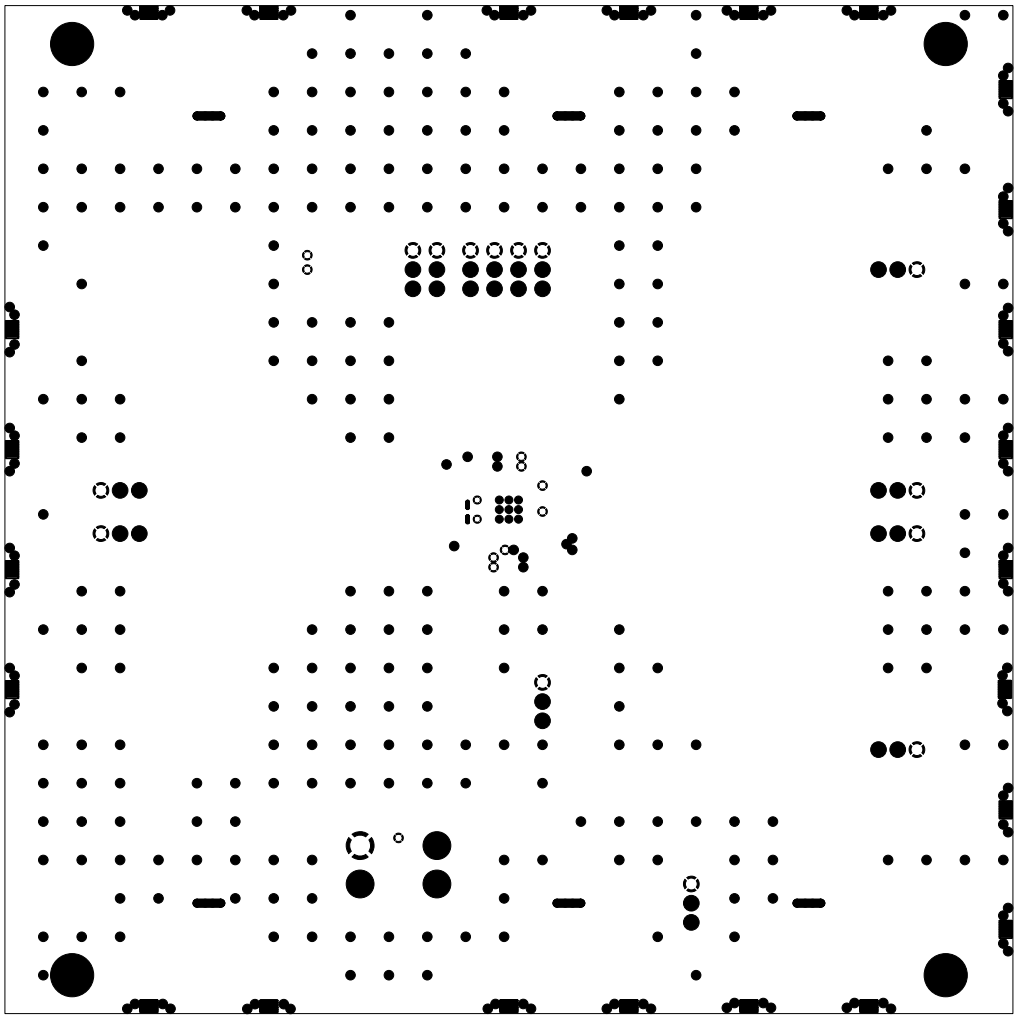
LAYER 2 GND PLANE



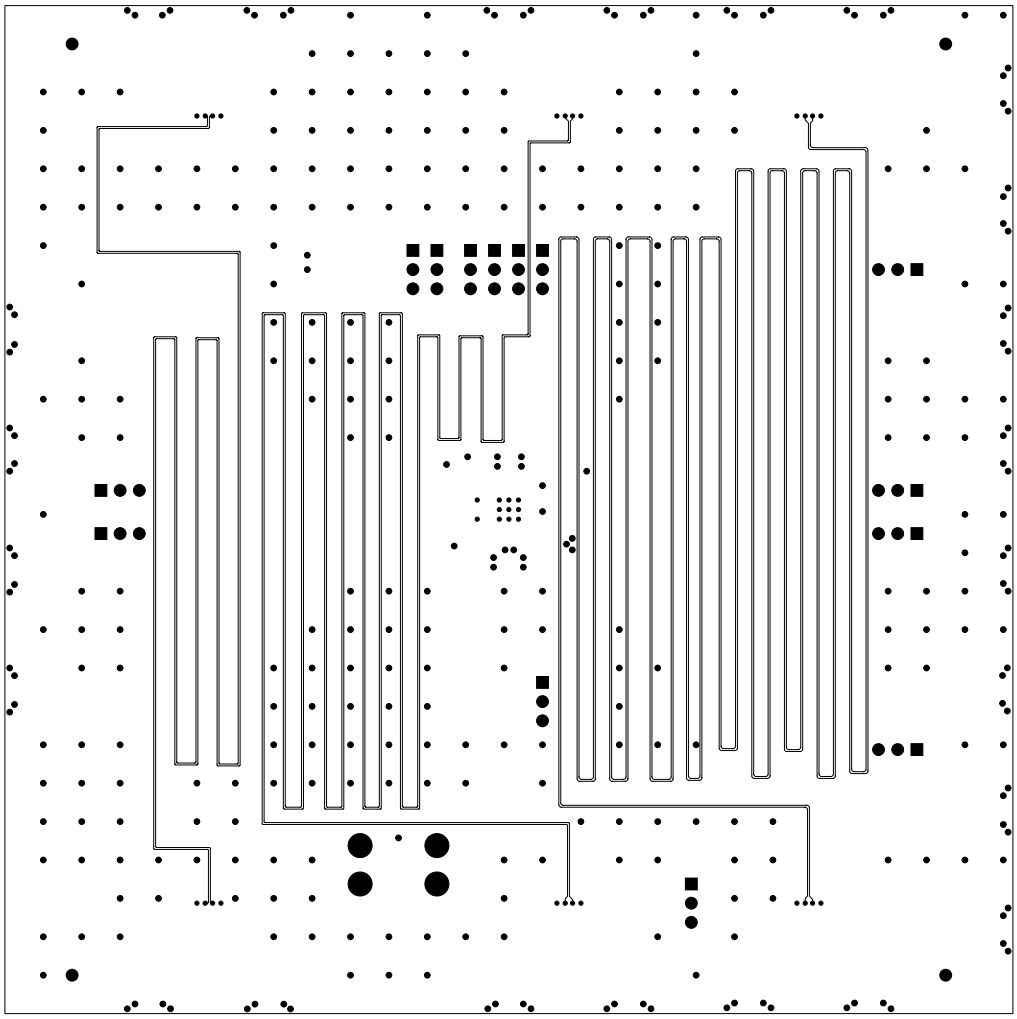
LAYER 3 SIGNAL



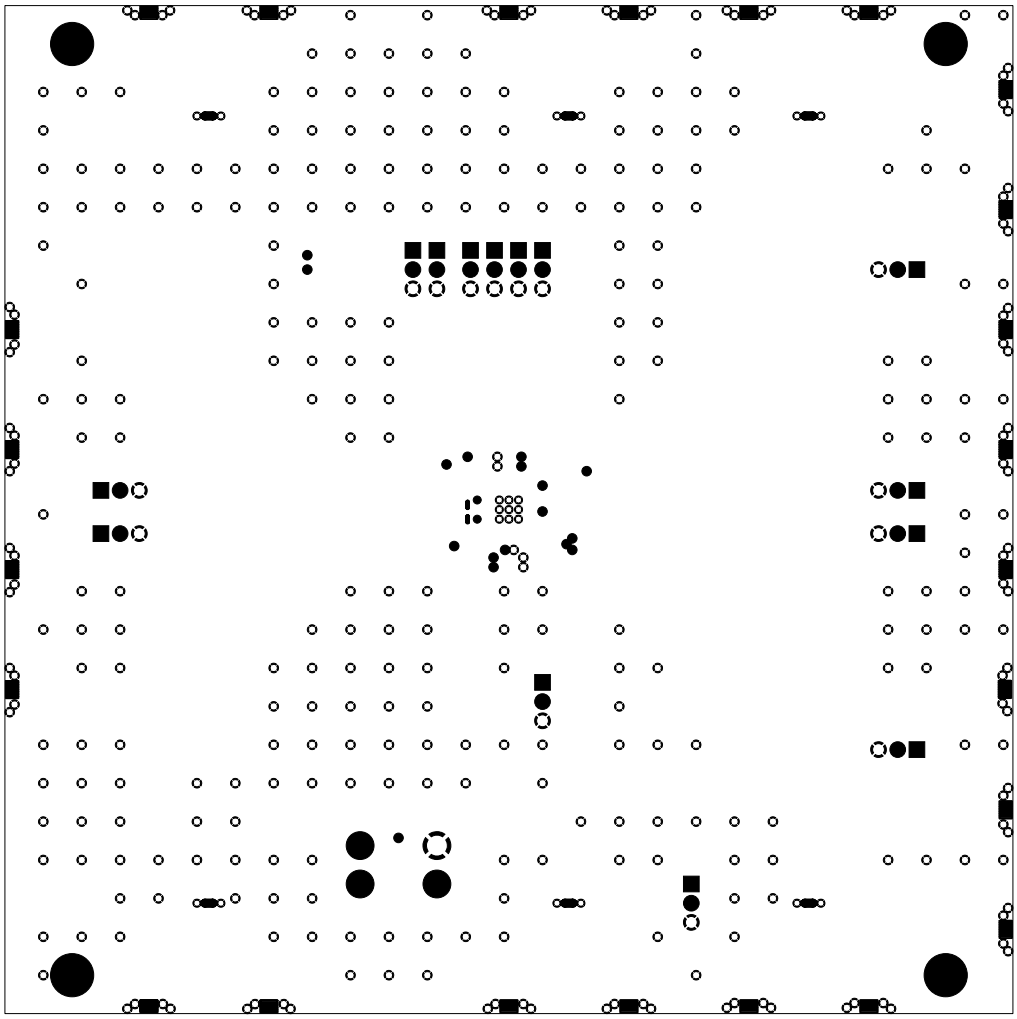
LAYER 4 GND PLANE



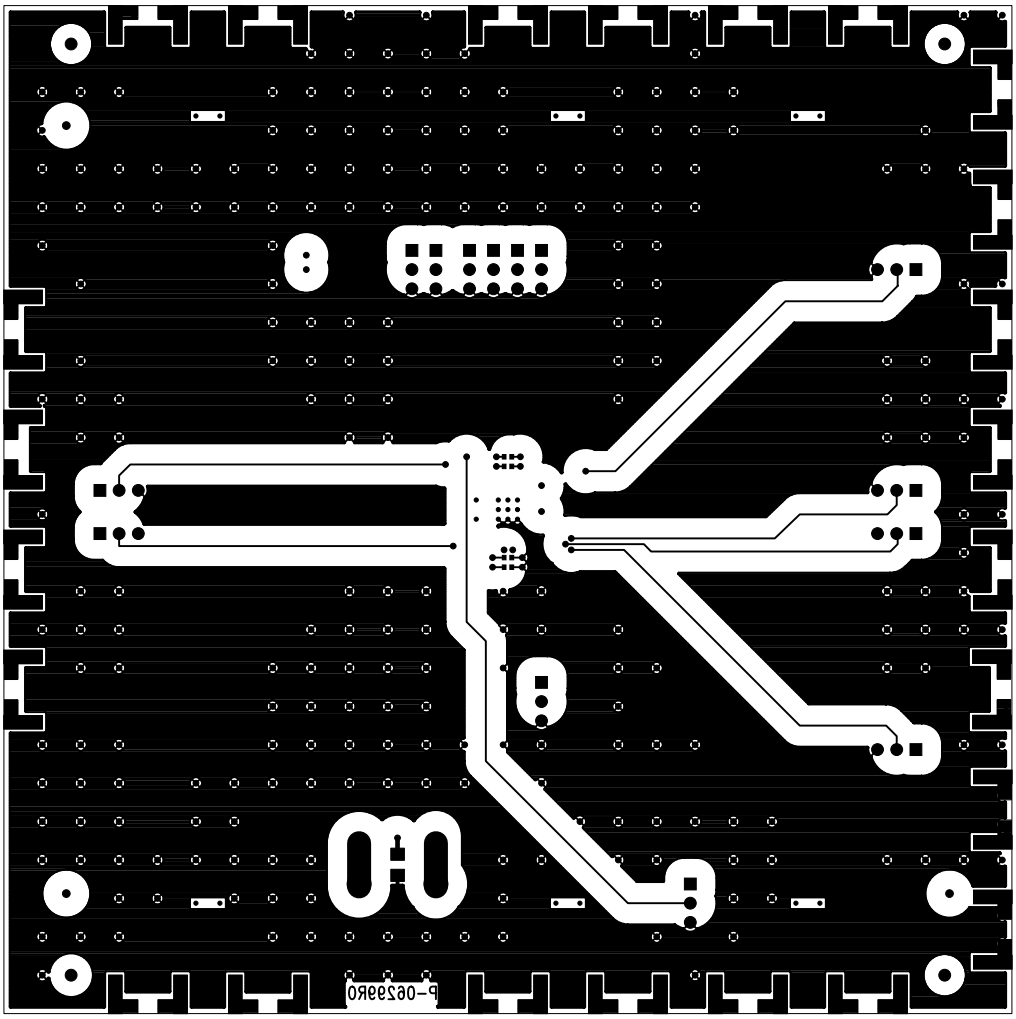
LAYER 5 VCC PLANE



LAYER 6 SIGNAL



LAYER 7 GND PLANE



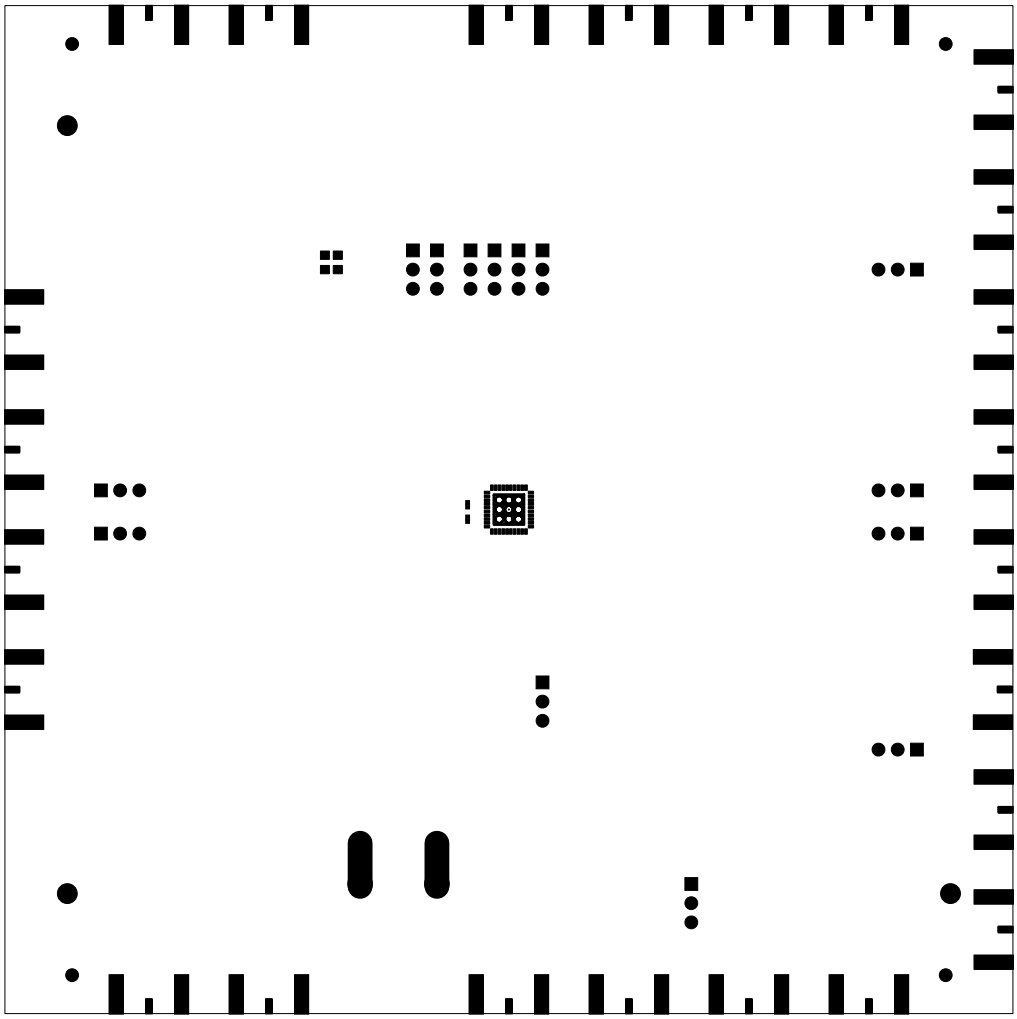
C17

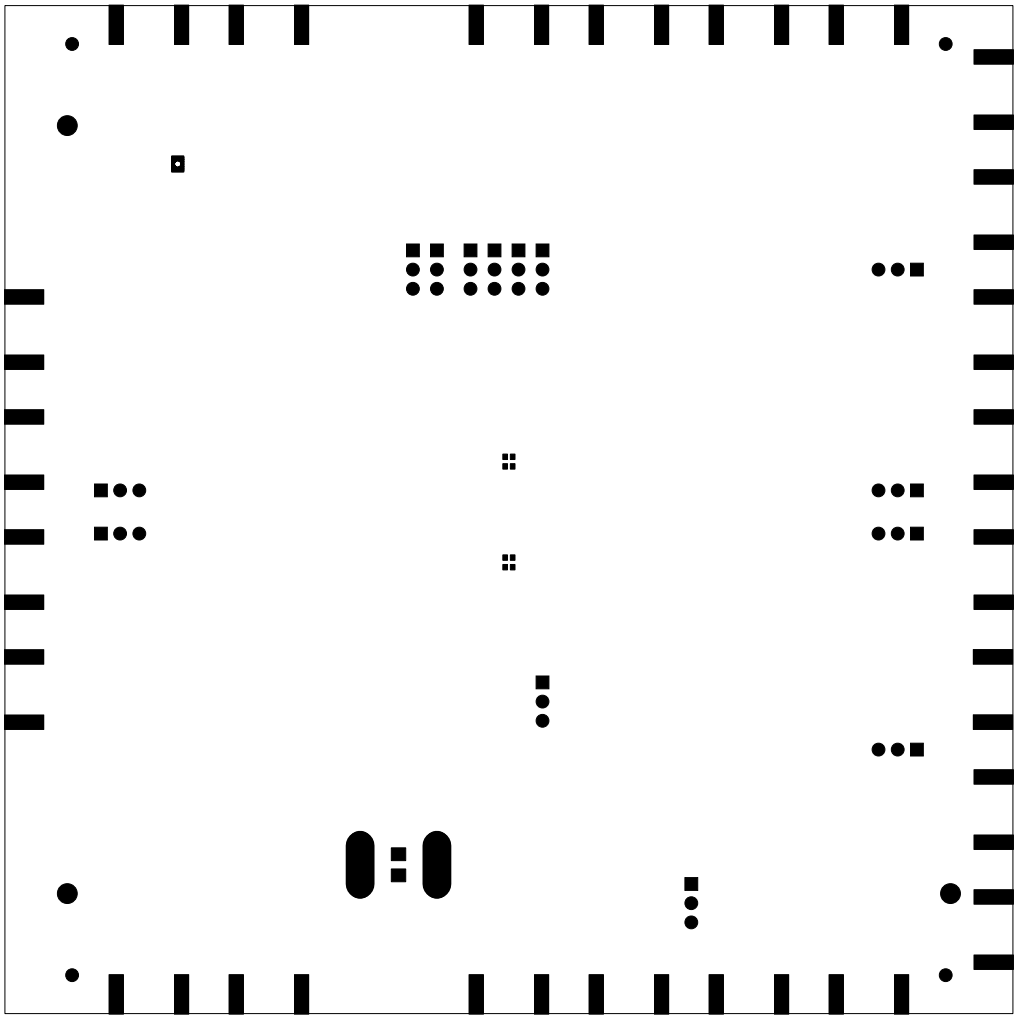
C16

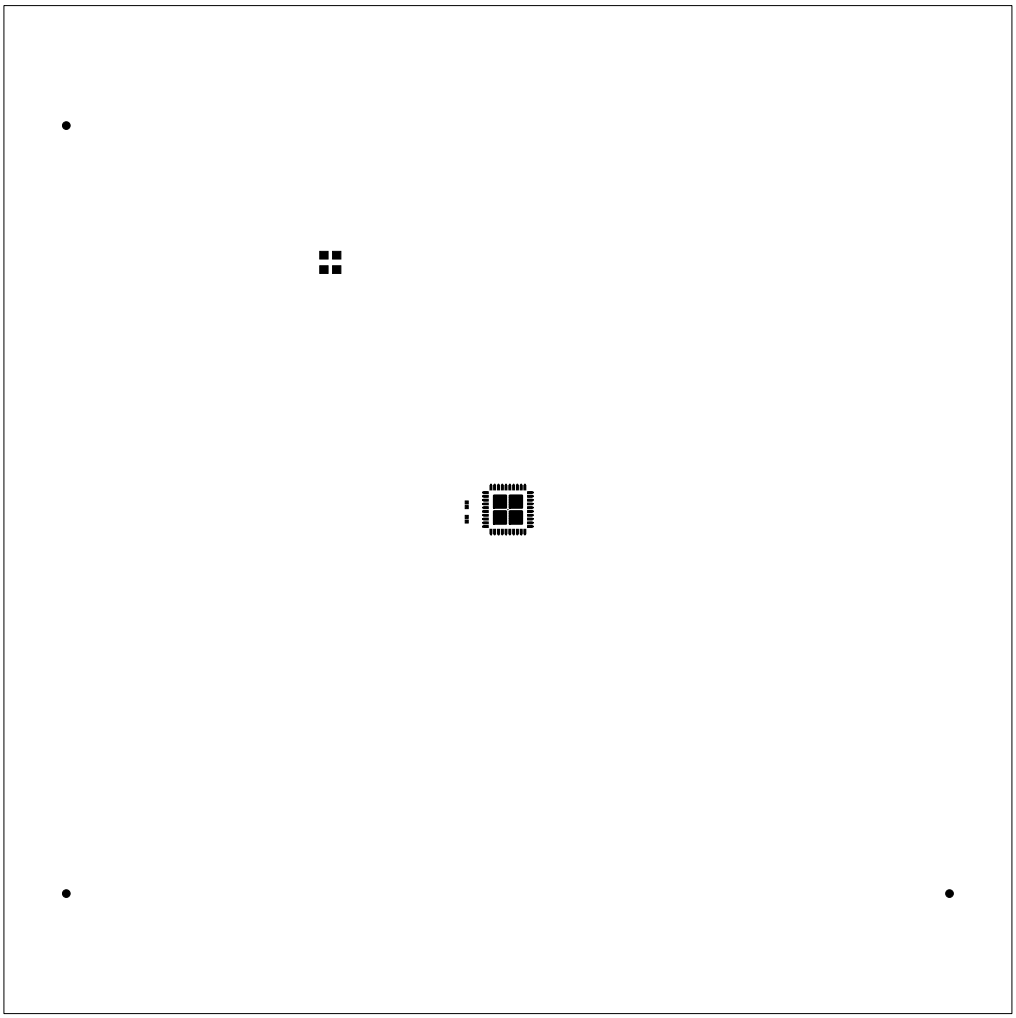
C14

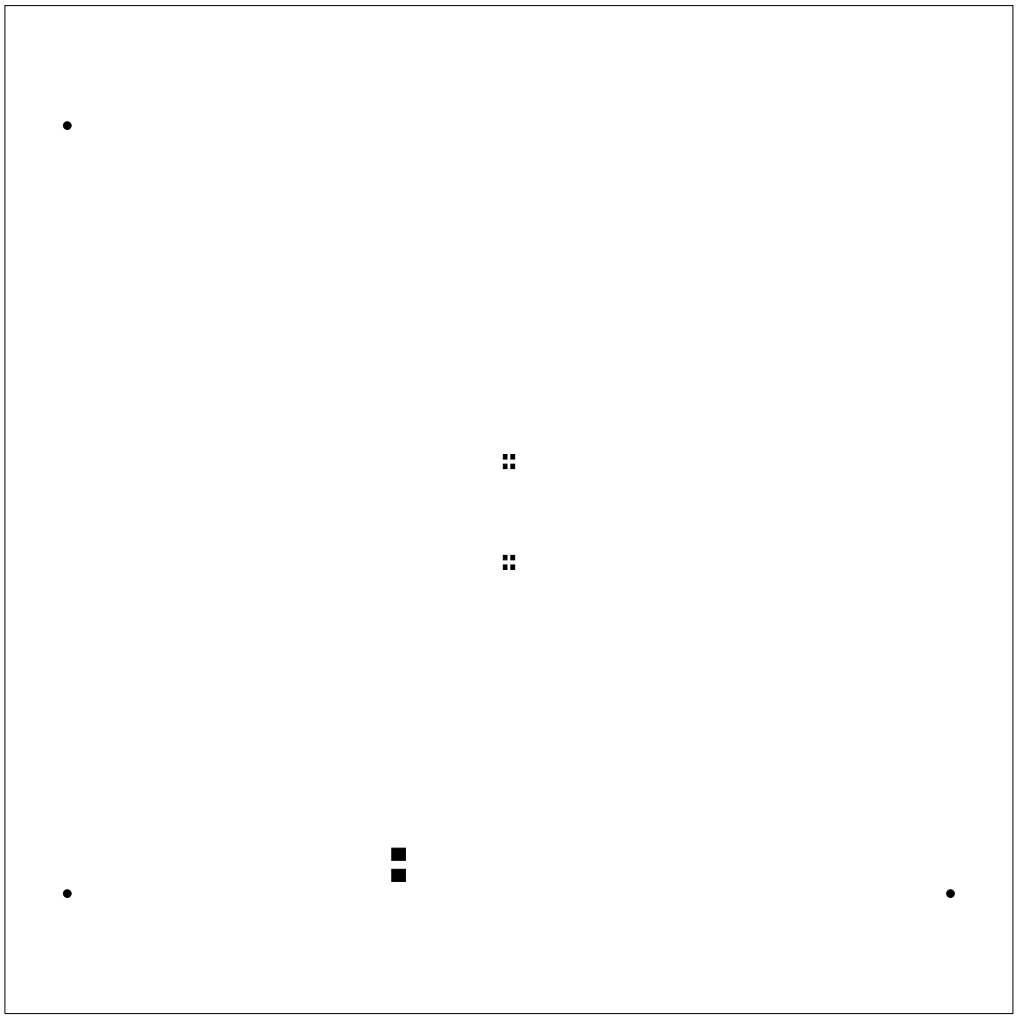
C15

C18









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