AN–1208 LM2633 Evaluation Board

1 Specifications

Input Voltage: 5 V to 24 V (don't go above 24 V because input capacitors are rated for 25 V only)

Continuous Load Current:

Ch1 = 16A

Ch2 = 5A

Ch3 = 300 mA

Output Voltage:

Ch1 = DAC-Programmable (0.9 V ~ 2.0 V)

Ch2 = 1.5 V

Ch3 = 2.5 V

Minimum Steady-State Duty Cycle:

8% (steady-state duty cycle lower than this may cause subharmonic oscillations)

DIP Switch-Changeable Settings:

VID0 to VID4 logic levels

ON/SS1 and ON/SS2 pins (either grounded or connected to a capacitor)

FPWM pin (either grounded or pulled up to 5 V)

UV_Delay pin (either grounded or connected to a capacitor).

NOTE:

1. When a DIP switch slide is ON, the signal whose label appears beside that slide is grounded.
2. Much flexibility is built into the board. For example, it is possible to use a dual SO-8 FET in Ch2, it is possible to use leaded capacitors at the switching outputs, and VDDX voltage (5 V) can be supplied externally, and so forth.

2 Troubleshooting Guide

- Board would not start; try one or all of the following:
  - Check the DIP switch (S1) setting and make sure ON1 and ON2 are not grounded at the same time
  - Check the current limit setting on the input power supply and make sure it is more than 2A during start up
  - Disconnect all loads
  - Make sure input voltage is between 5 V and 24 V
- Power good flag does not go high
  - Make sure the 3.3 V is connected
  - If a scope probe is used to measure the voltage, make sure the scope is not set to 50 Ω termination impedance
  - Make sure all three channels are presenting the correct voltage
- Under-voltage shutdown does not activate
  - Make sure the UVD bit is not grounded at the DIP switch
  - Channel 3 will recover after the fault condition disappears
- The board shuts down after a VID bit is toggled on the DIP switch;
  - Do not change the Ch1 voltage setting on the fly using the DIP switch. Instead, set the corresponding DIP VID bits to float, and then use a signal generator to toggle the corresponding VID terminal(s).
- Output voltage is too noisy
  - If you see large voltage spikes in the output voltage waveform, with a 2 µs/div time base, it is most probably noise picked up by your probe. You can greatly reduce the sensitivity of your probe to the radiated noise by shortening its ground lead.

3 Using an External 5 V to Supply the FET Drivers

Using the internal VLIN5 to power the VDDX pins has an efficiency penalty at light loads, especially when the input voltage is high. If there happens to be an external 5 V available, it may make sense to use the external one. However, there may be a timing issue. Namely, if the external 5 V comes up too late so that at the end of the soft start process the output voltages are still too low, then UVP will activate and cause the system to shut down. To work around this potential issue, it is recommended to DIODE OR the two 5 V rails. Of course, the external 5 V needs to be slightly higher than VLIN5 so that the latter will not be supplying VDDX current. To do this, remove R16 on the evaluation board, and connect the external 5 V to terminal “ext5v”.

4 Speedstep™ Setup

There are five VID terminals on the board. Determine which VID pins you need to toggle, and set the corresponding DIP switch slides to OFF. Set the signal generator to square wave, with a frequency below 1 kHz, and voltage levels between 0 V and 5 V. Connect the signal generator to the corresponding VID terminal(s) and to the “sgnd” terminal. Enable the signal generator after soft start.

5 Adaptive Voltage Positioning

Adaptive voltage positioning (AVP) is a technique that lowers the output voltage when the load is heavier and raises it when the load is lighter. The technique creates more room for fast load transients and thus saves output capacitors. To do AVP, cut open the wide trace that is shorting the two pads of R17, and install a current sense resistor. Then use R15 and R18 to adjust the amount of current feedback needed.

6 Using NFET wWth Channel 3

While G3 pin of Channel 3 can go up to 4 V maximum, if the output voltage is low enough, it is still possible to use an NFET as the pass transistor. With this evaluation board, a TSOP-6 FET can be installed as Q8. Check the “Current Sourcing Capability of Pin G3 vs. Its Voltage” curve in the device-specific data sheet and determine if an NFET can be used for your application.

7 Connection Diagram

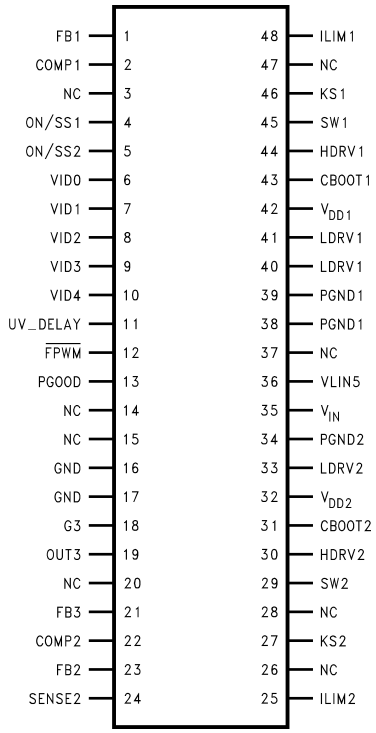

Figure 1. 48-Lead TSSOP (MTD) - TOP VIEW

8 Pin Descriptions

FB1 (Pin 1): The feedback input for Channel 1. Connect to the load directly.

COMP1 (Pin 2): Channel 1 compensation network connection (connected to the output of the voltage error amplifier).

NC (Pins 3, 14, 15, 20, 26, 28, 37 and 47): No internal connection.

ON/SS1 (Pin 4): Adding a capacitor to this pin provides a soft-start function that minimizes inrush current and output voltage overshoot; A lower than 0.8 V input (open-collector type) at this pin turns off Channel 1; also if both ON/SS1 and ON/SS2 pins are below 0.8 V, the whole chip goes into *shut down mode*.

ON/SS2 (Pin 5): Adding a capacitor to this pin provides a soft-start function that minimizes inrush current and output voltage overshoot; A lower than 0.8 V input (open-collector type) at this pin turns off Channel 2; also if both ON/SS1 and ON/SS2 pins are below 0.8 V, the whole chip goes into *shut down mode*.

VID4-0 (Pins 6-10): Voltage identification code. Each pin has an internal pull-up. They can accept open collector compatible 5-bit binary code from the CPU. The code table is shown in Table 2.

UV_DELAY (Pin 11): A capacitor from this pin to ground adjusts the delay for the output under-voltage lockout.

$\overline{\text{FPWM}}$ (Pin 12): When $\overline{\text{FPWM}}$ is low, pulse-skip mode operation at light load is disabled. The regulator is forced to operate in constant frequency mode.

PGOOD (Pin 13): A constant monitor on the output voltages. It indicates the general health of the regulators. For more information, see Power Good Truth Table and Power Good Function in Operation Descriptions.

GND (Pin 16-17): Low-noise analog ground.

G3 (Pin 18): Connect to the base of the linear regulator transistor.

OUT3 (Pin 19): Connect to the output of the linear regulator.

FB3 (Pin 21): The feedback input for the linear regulator, connected to the center of the external resistor divider.

COMP2 (Pin 22): Channel 2 compensation network connection (it is the output of the voltage error amplifier).

FB2 (Pin 23): The feedback input for Channel 2. Connect to the center of the output resistor divider.

SENSE2 (Pin 24): Remote sense pin of Channel 2. This pin is used for skip-mode operation.

ILIM2 (Pin 25): Current limit threshold setting for Channel 2. It sinks at a constant current. A resistor is connected between this pin and the top MOSFET drain. The voltage across this resistor is compared with the V_{DS} of the top MOSFET to determine if an over-current condition has occurred in Channel 2.

KS2 (Pin 27): The Kelvin sense for the drain of the top MOSFET of Channel 2.

SW2 (Pin 29): Switch-node connection for Channel 2 that is connected to the source of the top MOSFET.

HDRV2 (Pin 30): Top gate-drive output for Channel 2. HDR is a floating drive output that rides on SW voltage. MOSFET of Channel 2.

CBOOT2 (Pin 31): Bootstrap capacitor connection for Channel 2 top gate drive.

VDD2 (Pin 32): The input voltage supply for the LDRV2 gate driver.

LDRV2 (Pin 33): Low-side gate-drive output for Channel 2.

PGND2 (Pin 34): The analog input voltage supply.

VIN (Pin 35): The Kelvin sense for the drain of the top MOSFET of Channel 2.

VLIN5 (Pin 36): The output of the internal 5 V linear regulator. Connect to the ground with a 1UF ceramic capacitor. This pin can be connected to a 5 V supply (if available) to improve efficiency.

PGND1 (Pin 38-39): Power ground for Channel 1.

LDRV1 (Pin 40-41): Bottom gate-drive output for Channel 1.

VDD1 (Pin 42): The input voltage supply for the LDRV1 gate driver.

CBOOT1 (Pin 43): Bootstrap capacitor connection for Channel 1 top gate drive.

HDRV1 (Pin 44): Top gate-drive output for Channel 1. HDRV is a floating drive output that rides on SW voltage.

SW1 (Pin 45): Switch-node connection for Channel 1 that is connected to the source of the top MOSFET.

KS1 (Pin 46): The Kelvin sense for the drain of the top MOSFET of Channel 1.

ILIM1 (Pin 48): Current limit threshold setting for Channel 1. It sinks a constant current. A resistor is connected between this pin and the top MOSFET drain. The voltage across this resistor is compared with the V_{DS} of the top MOSFET to determine if an over-current condition has occurred in Channel 1.

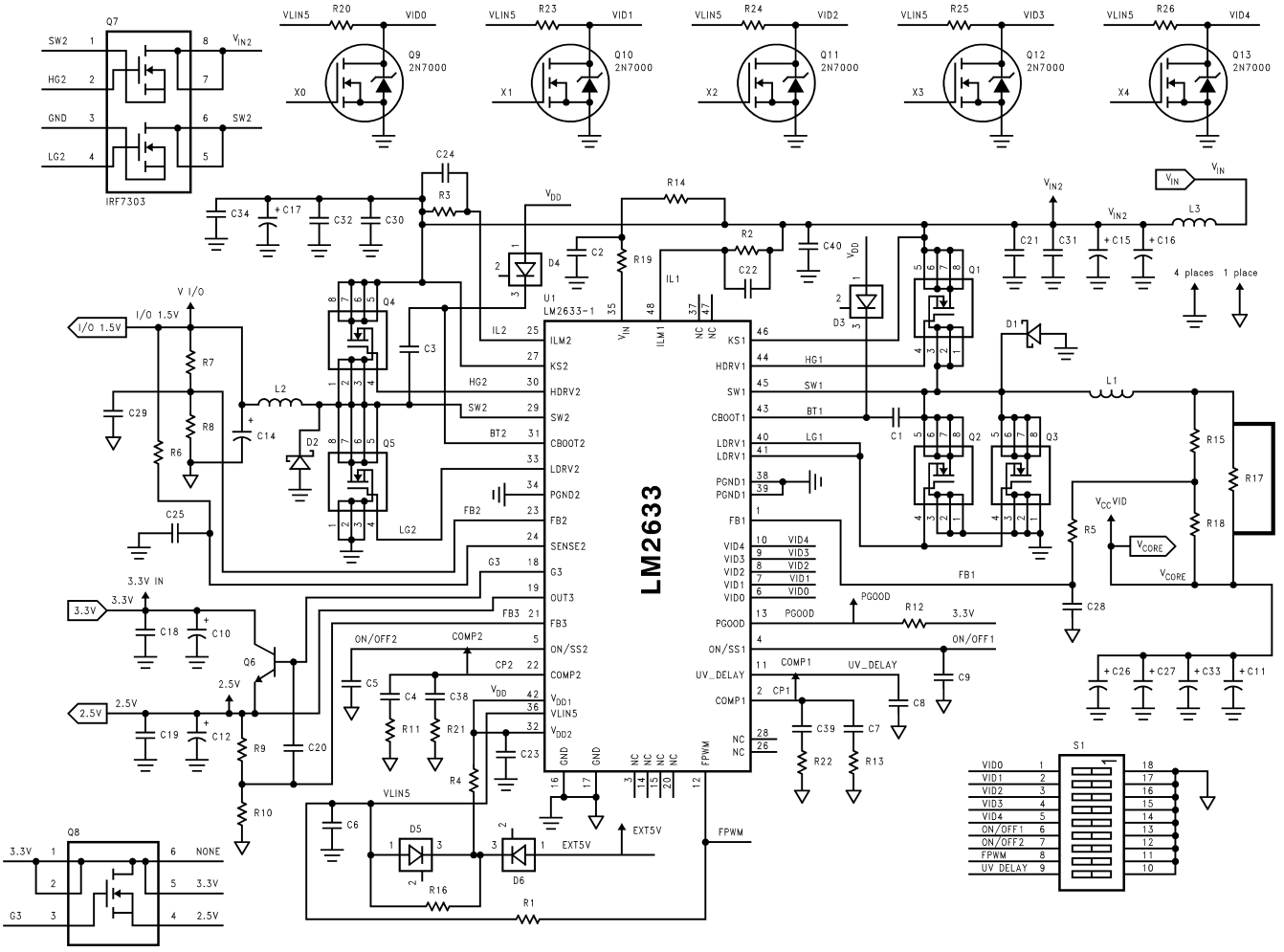

Figure 2. LM2633 Evaluation Board

Table 1. Bill of Materials (BOM) (Parts not listed are not installed)

Designator	Part Specification	Size	Part Type	Part Number	Manufacturer	Qty. Per Board
C15, C16, C17	56UF, 25 V, OSCON	RADIAL, 10.3 mm x 10.3 mm	CAPACITOR, OSCON	**25SP56M**	Sanyo	3
C14, C26, C27, C33	1 mF, 4 V, 18 mΩ	E Case	CAPACITOR, TANTALUM	**T510E108M004AS**	Kemet	4
C39	150 pF, 16 V, X7R, 20%	805	CAPACITOR, CERAMIC	**VJ0805Y151MXJAB**	Vishay	1
C38	680 pF, 16 V, X7R, 20%	805	CAPACITOR, CERAMIC	**VJ0805Y681MXJAB**	Vishay	1
C5, C9	4700 pF, 16 V, X7R, 20%	805	CAPACITOR, CERAMIC	**VJ0805Y472MXJAB**	Vishay	2
C22, C24	0.01 µF, 50 V, X7R, 20%	805	CAPACITOR, CERAMIC	**VJ0805Y103MXJAB**	Vishay	2
C4, C7	0.015 µF, 16 V, X7R, 20%	805	CAPACITOR, CERAMIC	**VJ0805Y153MXJAB**	Vishay	2
C1, C2, C3, C8	0.1 µF, 50 V, X7R, 20%	805	CAPACITOR, CERAMIC	**VJ0805Y104MXJAB**	Vishay	4
C21, C30, C31, C32, C34, C40	0.33 µF, 50 V, X7R, 20%	1206	CAPACITOR, CERAMIC	**VJ1206Y334MXAAB**	Vishay	6
C18, C19, C23	0.47 µF, 16 V, X7S, 20%	805	CAPACITOR, CERAMIC	**VJ0805S474MXJAB**	Vishay	3

Table 1. Bill of Materials (BOM) (Parts not listed are not installed) (continued)

Designator	Part Specification	Size	Part Type	Part Number	Manufacturer	Qty. Per Board
C6	1 µF, 16 V, X7S, 20%	1206	CAPACITOR, CERAMIC	**VJ1206S105MXJAC**	Vishay	1
D3, D4, D5, D6	30 V, 200 mA	SOT-23	DIODE, SCHOTTKY	**BAT54**	Vishay	4
L1	1.6 µH, 15.5A, 1.5 mΩ	14.6 mm x 14.6 mm	INDUCTOR	**CEPH149-1R6MC**	Sumida	1
L2	10 µH, 5.4A, 21.6 mΩ	12 mm x 12 mm	INDUCTOR	**CDRH127-100MC**	Sumida	1
L3	1.5 µH, 6.4A, 10 mΩ	13 mm x 9.4 mm	INDUCTOR	**DO3316P-152**	Coilcraft	1
Q9, Q10, Q11, Q12, Q13	60 V, 115 mA	SOT-23	N-FET	**2N7002LT1**	ON	5
Q6	40 V, 600 mA	SOT-23	BJT, NPN	**MMBT2222ALT1**	ON	1
Q1, Q2, Q3	30 V, 10 mΩ @ 4.5 V, 16 nC	SO-8	N-FET	**IRF7805**	IR	3
Q4, Q5	30 V, 25 mΩ @ 4.5 V, 14 nC	SO-8	N-FET	**IRF7807**	IR	2
R11	22k, 5%	805	RESISTOR	**CRCW0805223J**	Vishay	1
R21	2.2k, 5%	805	RESISTOR	**CRCW0805222J**	Vishay	1
R5, R6, R18, R19	0 Ω	805	RESISTOR		Vishay	4
R4, R14	10 Ω, 20%	805	RESISTOR	**CRCW0805100J**	Vishay	2
R7, R9, R10, R22	10.0k, 1%	805	RESISTOR	**CRCW08051002F**	Vishay	4
R3	16.2k, 1%	805	RESISTOR	**CRCW08051622F**	Vishay	1
R2	26.1k, 1%	805	RESISTOR	**CRCW08052612F**	Vishay	1
R8	47.5k, 1%	805	RESISTOR	**CRCW08054752F**	Vishay	1
R1, R12, R13, R20, R23, R24, R25, R26	100k, 20%	805	RESISTOR	**CRCW0805104J**	Vishay	8
S1	9 POSITION DIP SWITCH	DIP-9	SWITCH, DIP	**435640-6**	AMP	1
TP1–TP23	0.094″	94 mils	TERMINAL	**160-1026-02-01-00**	IPI CAMBION	23
U1	Triple Controller	TSSOP-48	IC	**LM2633**	TI	1

Table 2. VID Code and DAC Output

VID4	VID3	VID2	VID1	VID0	DAC Voltage (V)
1	1	1	1	1	No CPU[(1)]
1	1	1	1	0	0.925
1	1	1	0	1	0.950
1	1	1	0	0	0.975
1	1	0	1	1	1.000
1	1	0	1	0	1.025
1	1	0	0	1	1.050
1	1	0	0	0	1.075
1	0	1	1	1	1.100
1	0	1	1	0	1.125
1	0	1	0	1	1.150
1	0	1	0	0	1.175
1	0	0	1	1	1.200
1	0	0	1	0	1.225
1	0	0	0	1	1.250
1	0	0	0	0	1.275

(1) This code is set to 0.900 V for convenience.

Table 2. VID Code and DAC Output (continued)

VID4	VID3	VID2	VID1	VID0	DAC Voltage (V)
0	1	1	1	1	1.25
0	1	1	1	0	1.30
0	1	1	0	1	1.35
0	1	1	0	0	1.40
0	1	0	1	1	1.45
0	1	0	1	0	1.50
0	1	0	0	1	1.55
0	1	0	0	0	1.60
0	0	1	1	1	1.65
0	0	1	1	0	1.70
0	0	1	0	1	1.75
0	0	1	0	0	1.80
0	0	0	1	1	1.85
0	0	0	1	0	1.90
0	0	0	0	1	1.95
0	0	0	0	0	2.00

9 PCB Layout

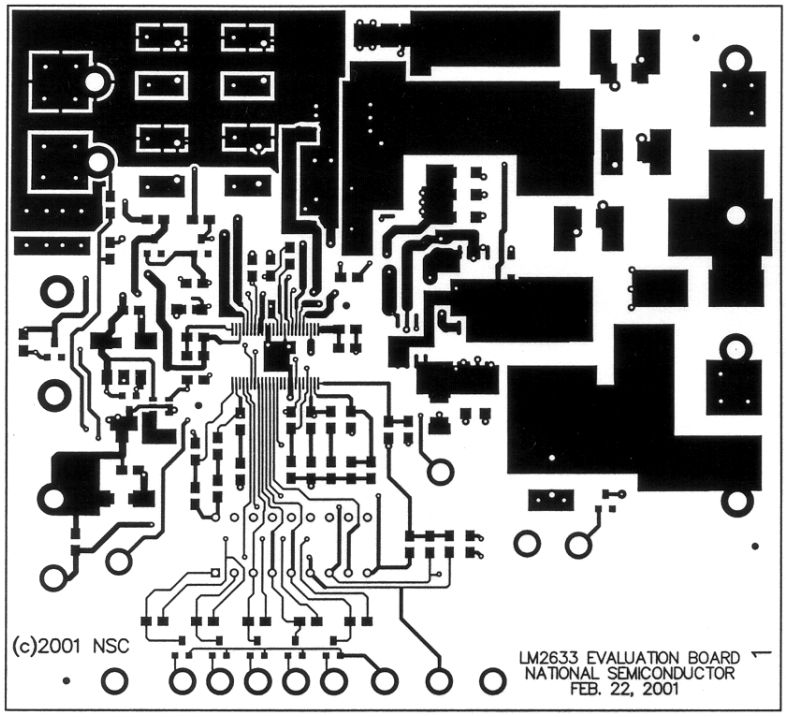

Figure 3. TOP LAYER

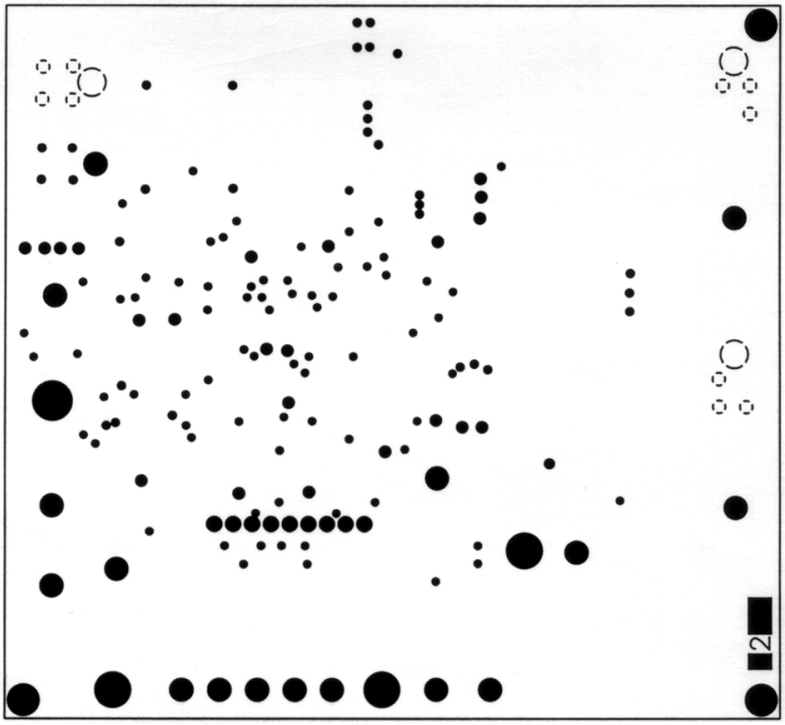

Figure 4. INTERNAL 1

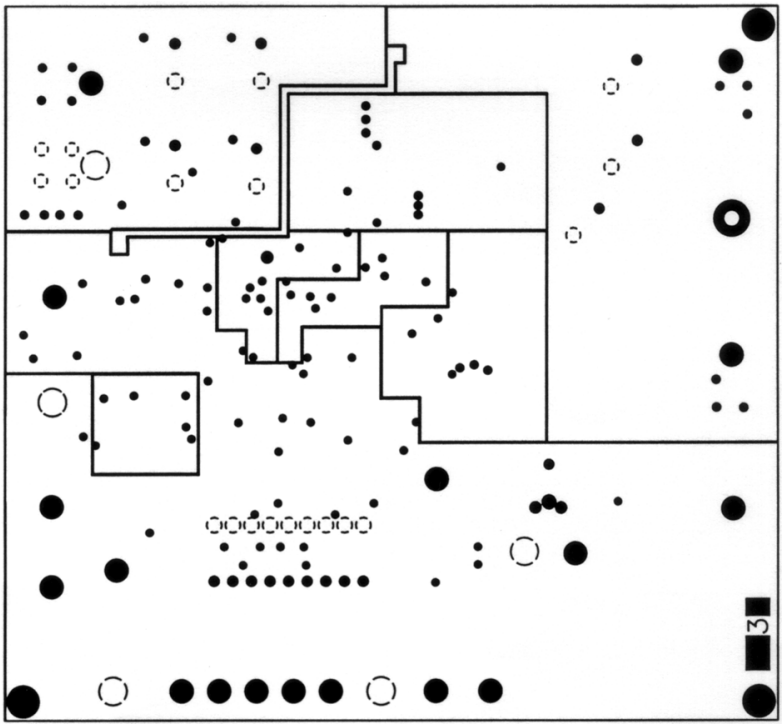

Figure 5. INTERNAL 2

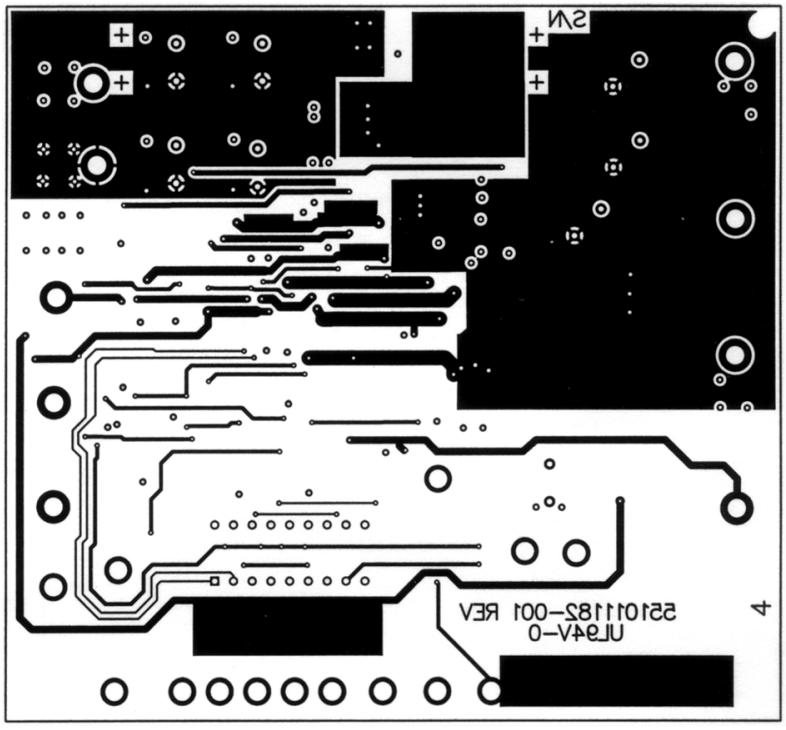

Figure 6. BOTTOM LAYER

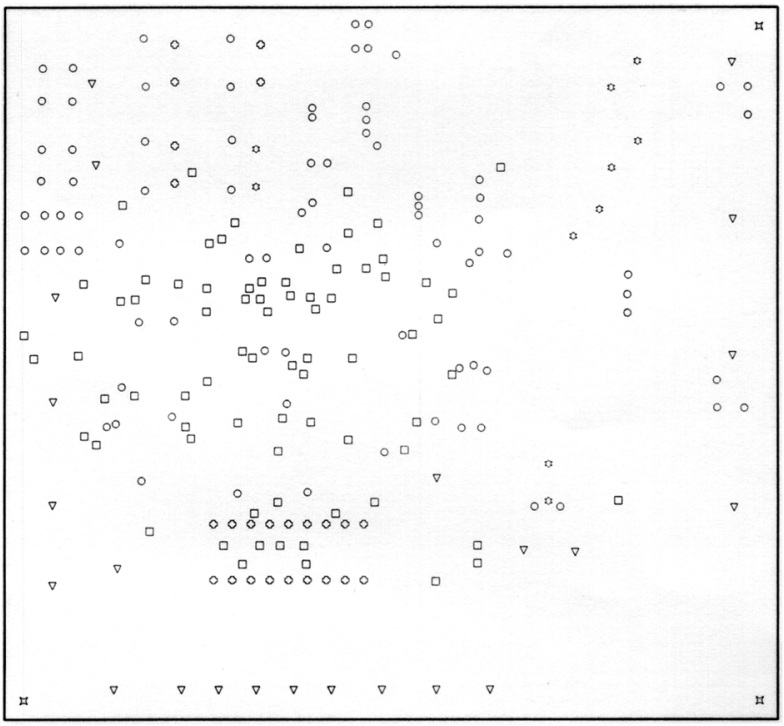

Figure 7. DRILL DRAWING

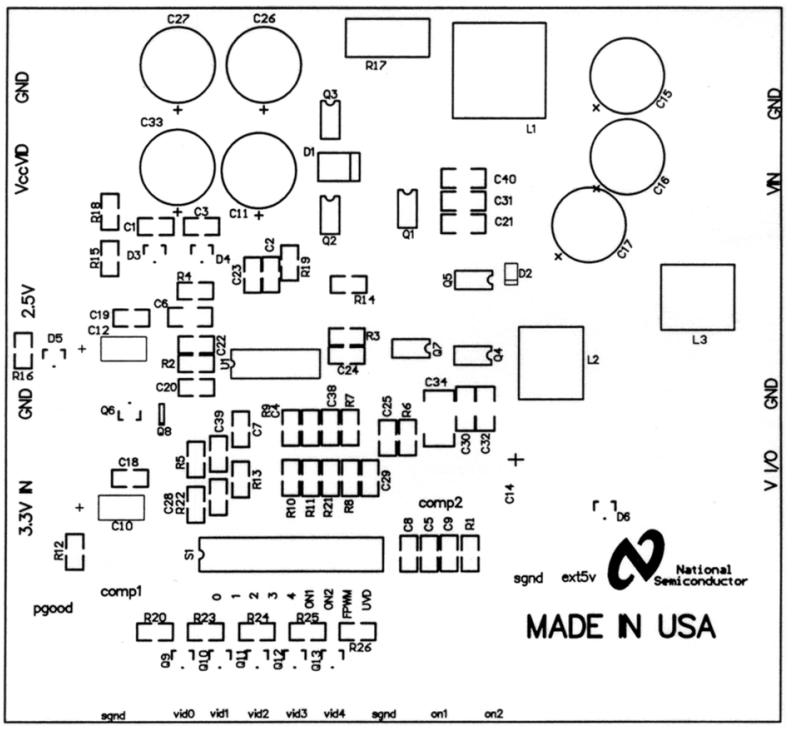

Figure 8. TOP SILKSCREEN

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