AN-1480 LP38859S-1.2 Evaluation Board

1 Introduction

This board is designed to enable the evaluation of the LP38859 voltage regulator. Each board is assembled and tested in the factory. This evaluation board has the TO-263 5–lead package mounted.

2 General Description

The LP38859 is a dual-rail LDO linear regulator capable of supplying up to 3A of output current, and incorporates a Soft-Start feature.

The device has been designed to work with 10 µF input and output ceramic capacitors, and 1µF bias capacitors. Footprints areas for C_{IN} and C_{OUT} will allow for a variety of sizes.

3 Operation

The input voltage, applied between V_{IN} and GND, should be at least 1.0 V greater than V_{OUT}, and no higher than the applied V_{BIAS} voltage.

The bias voltage, applied between V_{BIAS} and GND should be above the minimum bias voltage of 3.0 V, and no higher than the maximum of 5.5 V.

Loads can be connected to V_{OUT} with reference to GND.

V_{OUT} and V_{IN} test points are provided on the board to allow accurate measurements directly on the evaluation board, eliminating any voltage drop on the PCB traces or connecting wires to the load.

The Soft-Start time for V_{OUT} is an exponential function, and is adjusted by changing the Soft-Start capacitor (C_{SS}) on device pin one. An internal resistor (r_{SS}) and the external capacitor (C_{SS}) form an RC circuit. Five RC time constants is considered to be the Soft-Start time.

$$\text{Soft-Start Time} = 5 \times r_{SS} \times C_{SS} \quad (1)$$

The installed soft-start capacitor (C_{SS}) is 10 nF (0.01 µF), and the internal r_{SS} is typically 16 kΩ.

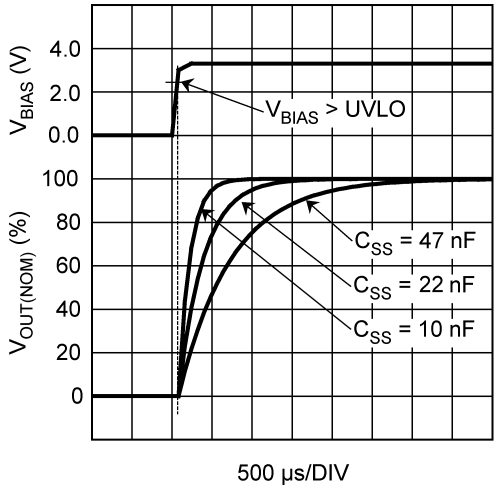

Figure 1. V_{OUT} vs C_{SS}

4 Hardware

The schematic is shown in Figure 2 and the layout of the evaluation board is shown in Figure 3.

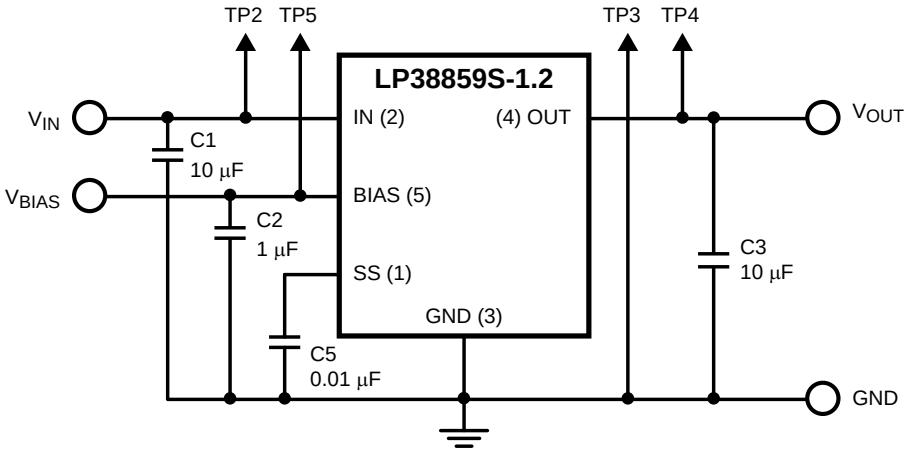

Figure 2. Evaluation Board Schematic

5 PCB Layout

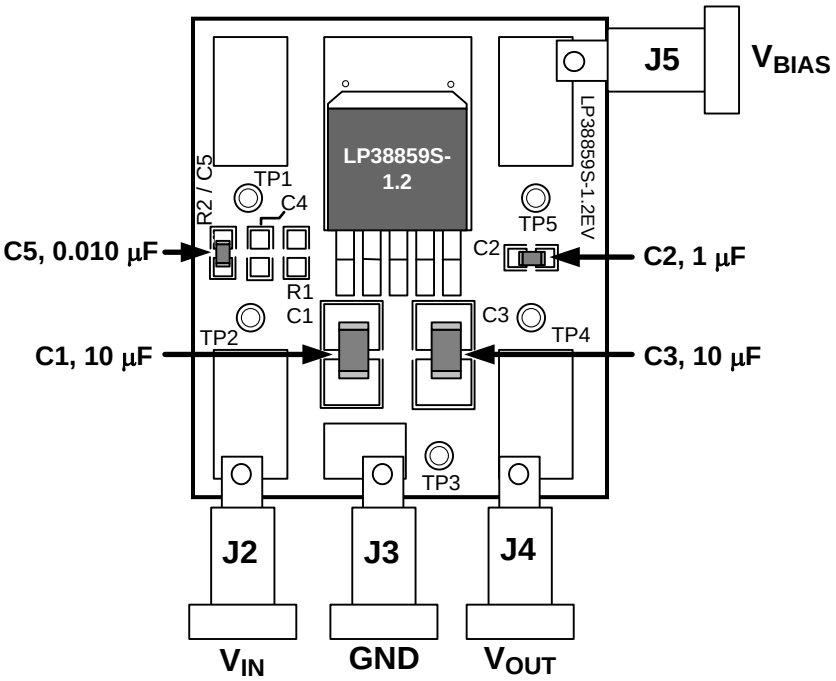

Figure 3. Evaluation Board Component and Pin Layout

6 Power Dissipation

The TO-263 package alone has a junction to ambient thermal resistance (θ_{JA}) rating of 60°C/W. When mounted on the LP38859S evaluation board the θ_{JA} rating is approximately 37°C/W.

Although there is only approximately 0.28 square inches of copper area immediately under the tab, the top copper surface area is extended to additional copper area on the bottom of the board by five thermal vias.

With the 37°C/W thermal rating the LP38859S evaluation board will dissipate a maximum of 2.75W with T_A = 25°C.

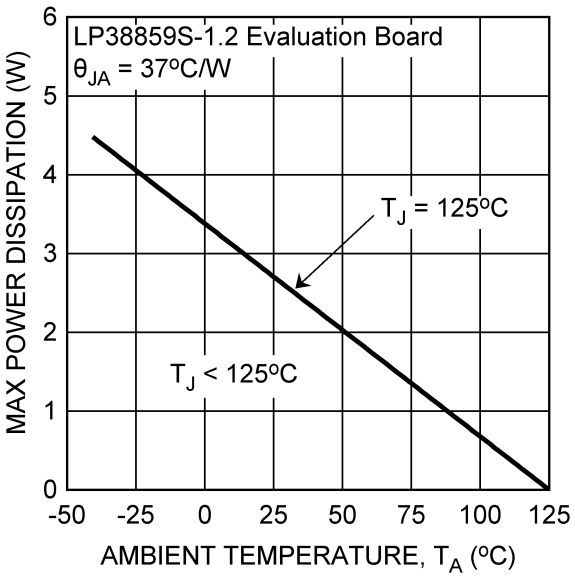

Figure 4. Maximum Power Dissipation vs Ambient Temperature

7 Bill of Materials (BOM)

Table 1. Bill of Materials (BOM)

ID	Name	Description	Manufacturer	Part Number
U1	U1	LP38859	Texas Instruments	LP38859
C1	C_{IN}	10 µF, 10%, MLCC, 10V, X7R, 1210	AVX	1210ZC106KAT2A
C2	C_{BIAS}	1 µF, 10%, MLCC, 10V, X7R, 0805	AXV	0805ZC105KAT2A
C3	C_{OUT}	10 µF, 10%, MLCC, 10V, X7R, 1210	AVX	1210ZC106KAT2A
C4	—	Not Installed	—	—
C5	C_{SS}	0.010 µF, 10%, MLCC, 16 V, X7R, 0805	AVX	0805YC103KAT2A
J1	—	Not Installed	Johnson Components	—
J2	V_{IN}	Banana Jack : Insulated Solder Terminal - RED		108–0902–001
J3	GND	Banana Jack : Insulated Solder Terminal - BLACK		108–0903–001
J4	V_{OUT}	Banana Jack : Insulated Solder Terminal - ORANGE		108–0906–001
J5	V_{BIAS}	Banana Jack : Insulated Solder Terminal - BLUE		108–0910–001
R1	—	Not Installed	—	—
R2	—	Not Installed	—	—
TP1	—	Not Installed	—	—
TP2	TP_{IN}	Turret Terminal : Mounting Hole Diameter = 0.062”	Keystone	1593-2
TP3	TP_{GND}			
TP4	TP_{OUT}			
TP5	TP_{BIAS}			

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