AN-1532 LP3906 Evaluation Kit

1 LP3906 Overview

The LP3906 is a multi-function, programmable Power Management Unit, optimized for low power FPGAs, microprocessors and DSPs. This device integrates two highly efficient 1.5A Step-Down DC/DC converters with dynamic voltage management (DVM), two 300mA Linear Regulators and a 400kHz I2C compatible interface to allow a host controller access to the internal control registers of the LP3906. The LP3906 additionally features programmable power-on sequencing and is offered in a tiny 5 × 4 × 0.8mm WQFN-24 pin package.

2 Evaluation Kit Overview

The LP3906 Evaluation Kit is based on a modular system, where the actual evaluation board is connected to the PC via a USB – I^2C interface board. The kit supports complete functional evaluation of the LP3906 circuit. The evaluation kit consists of

LP3906 evaluation board with USB interface

USB Interface cable

Evaluation software for PC

LP3906 datasheet

Evaluation Manual

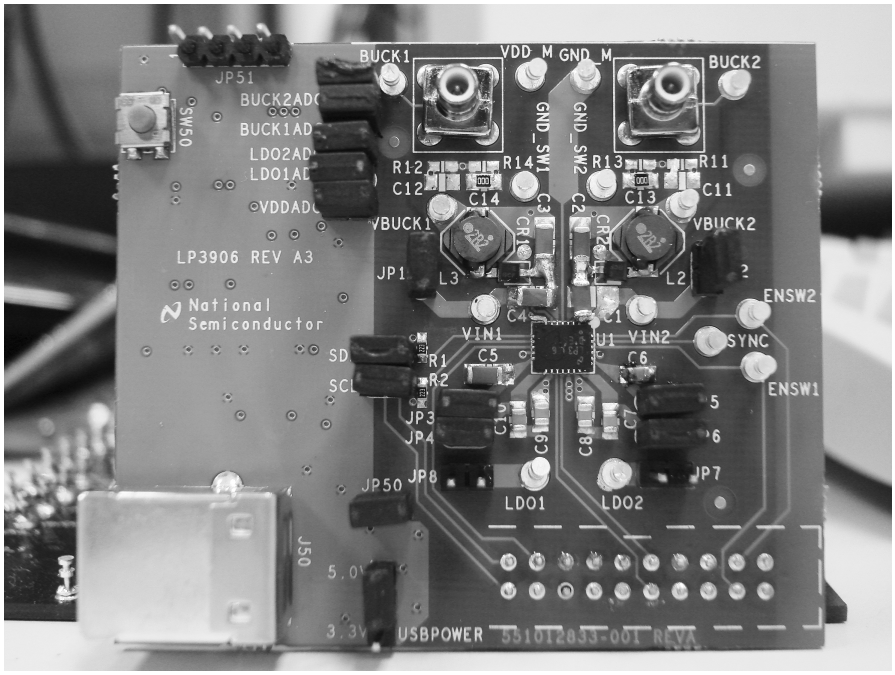


Figure 1. Evaluation Board

3 Evaluation Kit Setup

Please use ESD protection to prevent any unwanted damaging ESD events!

The LP3906 Evaluation Board should contain a USB interface to the left, as shown in Figure 1.

Connect this setup to the USB port of a PC using the included USB cable. When the USB board is plugged in for the first time, the operating system prompts for “New hardware found” and installs the USB driver. If this does not happen, try unplugging and plugging in the cable again.

LP3906 evaluation software can run directly from the delivered CD by double clicking its icon. However, we recommend that it be copied to the PC’s hard disk and run from there.

The software runs on WinXP and Windows 2000. Please note that Win XP OS administrator rights may be required to run the software.

4 Cautionary Notes

Always disconnect the USB cable from the board when changing the supply jumper setting (USB Power Jumper described in Section 7.1). Failure to do so may stop the USB board from responding.

If the USB interface is not responding or the software hangs up, press the reset button shown in Figure 2, or disconnect the USB cable for 5 seconds. Details of the operation of the USB interface board can be found in the accompanying USB interface manual.

The evaluation software allows control of all registers necessary to control the device through sliders and buttons. Direct Register Programming (described in Section 6.1) should only be used for debugging purposes.

The GUI can be used in conjunction with an external supply, as long as the USB cable is plugged into the board, and the USB Power Jumper is removed.

If the user is using an external supply and the cable is NOT plugged into the board, be sure to remove the jumpers connecting the USB interface to the chip – USBPOWER, GND plane, SDA, SCL, and all of the ADC jumpers.

5 Getting Started

Because of internal pullups, the LP3906 should become active as soon as the USB cable is plugged in. To avoid damaging any parts, be sure to read how to power the board in Section 7.1.

For a quick start, make sure to short (connect) all jumpers except for JP8 and JP7 on the LP3906 Evaluation board, see Figure 3. Those jumpers short circuit the LDO output to GND for internal test purposes. Also please disregard the 4 pin USB programming interface.

For a quick verification of a clean power up, start up the GUI (Figure 4), and the interface control at the bottom should read “OK”. For more information on powering up the LP3906 through a charger adapter, please refer to Section 7.1 or the LP3906 datasheet provided in the LP3906 Evaluation Kit CD.

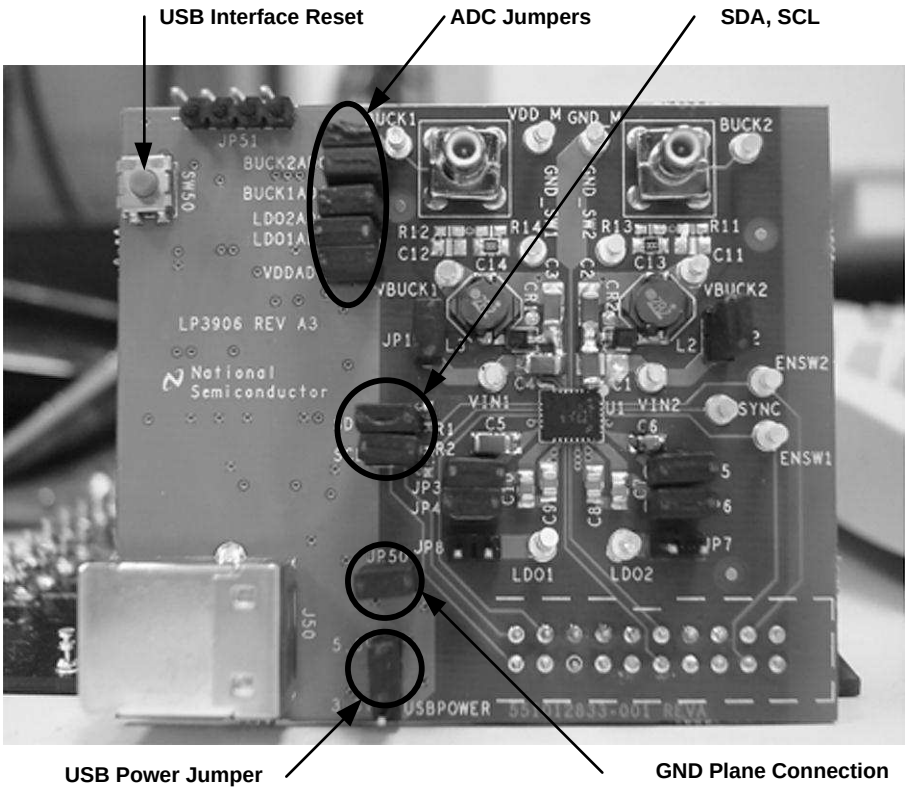


Figure 2. USB Interface Settings

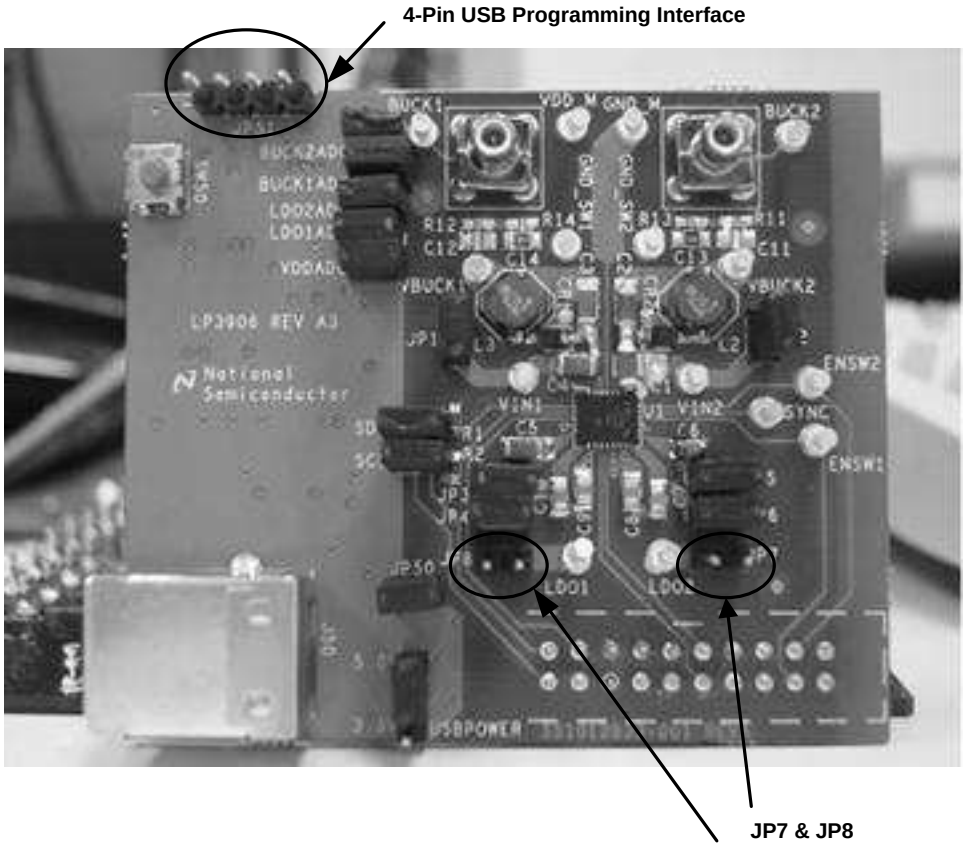


Figure 3. Starting Jumper Settings

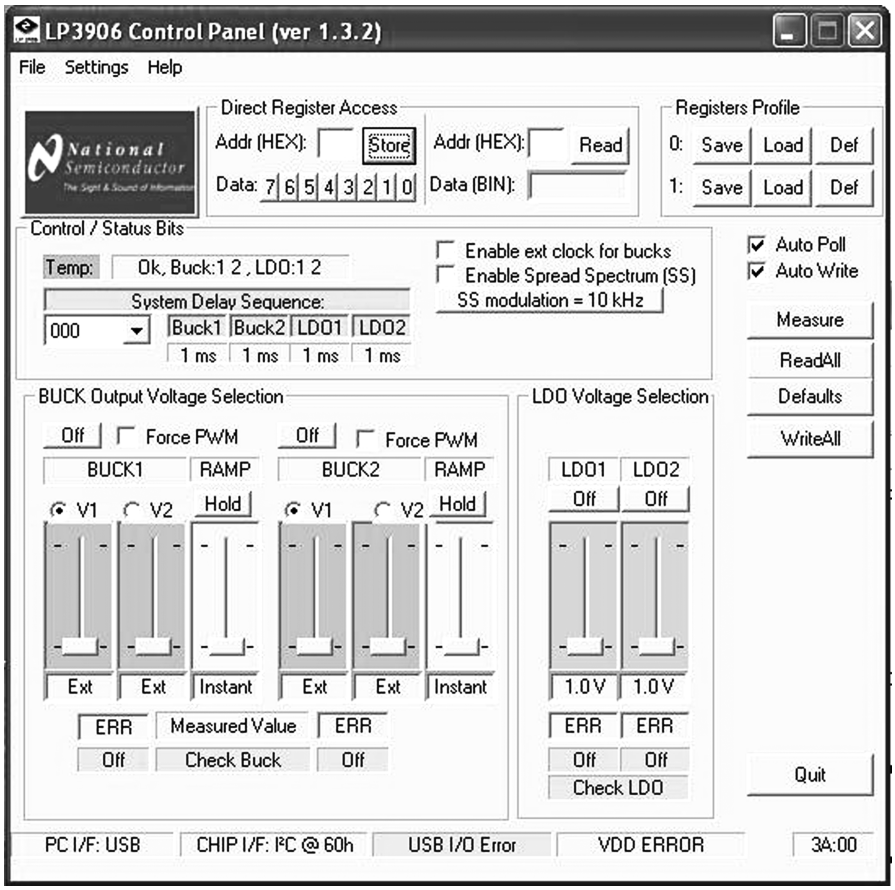


Figure 4. LP3906 Evaluation Software User Interface

6 Using the Evaluation Software

6.1 Register Interface

A register control established through an I2C compatible serial interface allows the user to directly program the registers by writing to and reading from the memory map registers. This provides the user with added flexibility in controlling the different functions of the LP3906. However, we caution the user to use this function only for debugging purposes, because sending wrong values could damage the part. Sliders and buttons provided below will accomplish the same commands in a more interactive way, and is also less prone to mistakes.

6.1.1 Using the Register Controls

Direct Register Access (left section of Figure 4 and Figure 5) is divided into two parts: Direct Register Write on the left and Direct Register Read on the right. To write to a specific register, simply type the register address in hexadecimal into the box, set the value through the specific bit buttons, and click “Write”. To read a value in binary, type in the register address in hexadecimal into the box on the right and click “Read”.

For example, to turn off all regulators except the LDO1 regulator, this could be done by typing in the number 10 into the “Addr (HEX):” box, clicking binary placeholder number 4, and then clicking store. The register should reflect the stored value assigned (00010000) when the user clicks the button “Read.” Please note that the same function could be more easily implemented through the graphical interfaces, and is in the users’ best interest use Direct Register Access only when necessary.

The register profile interface allows the user to save all his/her settings for use at a later time. The GUI is programmed to accommodate saving two sets of profiles.

Figure 5. Register Interface

6.2 Chip Control Interface

If the IC changes state and/or if the user assigns a new value to a register, the GUI may not reflect those changes if the “Auto Poll” button is not enabled. By hitting the “Read All” button, the user will manually renew the GUI so that it reflects the most current state of the IC. See right section of Figure 4 and Figure 6.

The “Auto Poll” check box refreshes the GUI every second to ensure that it mirrors the current state of the chip. The checkbox is on by default so that the user can constantly monitor the status of the IC. Similarly, the “Auto Write” check box will enable the signals generated from using the sliders or buttons to be sent to the chip. The check box is on by default, and should be unchecked if the user wishes not to change the settings on the chip.

The “Defaults” button will set all registers on the chip to the default settings when clicked. The “Measure” button will update the values measured on the chip by ADCs on the USB interface.

The Quit button allows the user to exit the program.

Figure 6. Chip Control Interface

6.3 Regulator Output Voltage Selection

The output voltages of all the LDO and buck converters can be programmed through I2C control registers by simply moving the slider (see bottom left section of Figure 4 and Figure 7). The buck regulators have 2 sliders and a Hold/Ramp button to control its output voltage. This prevents the user from scaling the bucks to the second voltage if the Hold/Ramp button is not depressed. The output of the buck regulator will reflect the setting of the slider that has its radio button clicked (V1 or V2).

The buck regulators also have a Hold/Ramp slider that determines how fast the regulators scale to the 2nd programmed voltage. The ramp time is measured from the time the chip receives the I2C signals from clicking the opposing radio button.

All of the regulators can also be hardware enabled or disabled via different configuration settings on the 20 pin header (described in Section 7.2). The buck regulators also have additional enable test points on the board.

The user can also force the bucks into PWM mode. Clicking the Force PWM check box on the GUI forces the respective regulator to stay in PWM mode even in the case of a light load (PFM mode). Forced PWM will be disabled by clicking the “Force PWM” check-box again.

The buck converters have a slider interface to provide an adjustable output voltage. By sliding the bar to the bottom of the slider, the user can use an external resistor divider network for setting the Bucks output voltage.

Force PWM mode is not recommended when a battery is powering the system.

The USB interface also contains ADCs to measure the output voltage of the regulators. To do so, simply connect the USB interface ADC jumpers shown in Figure 8. To measure the external voltages again, simply click the “Measure” button on the GUI.

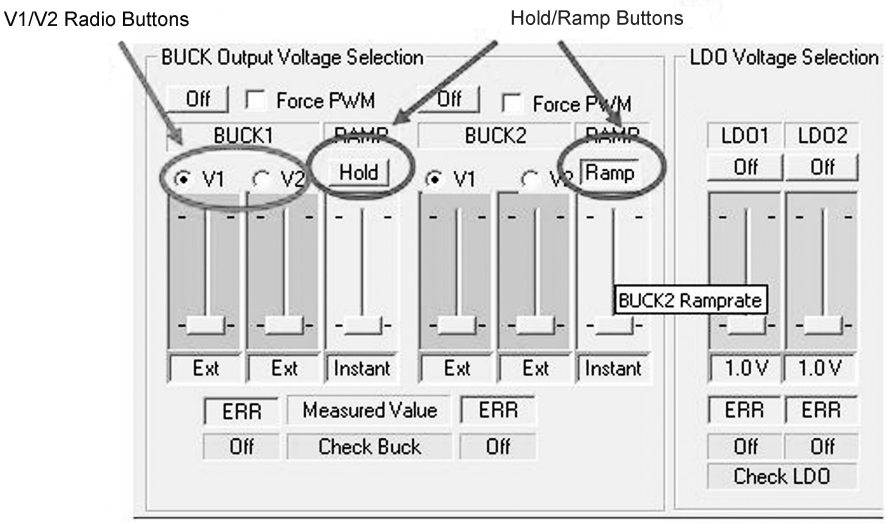


Figure 7. Regulator Output Voltage Selection Interface

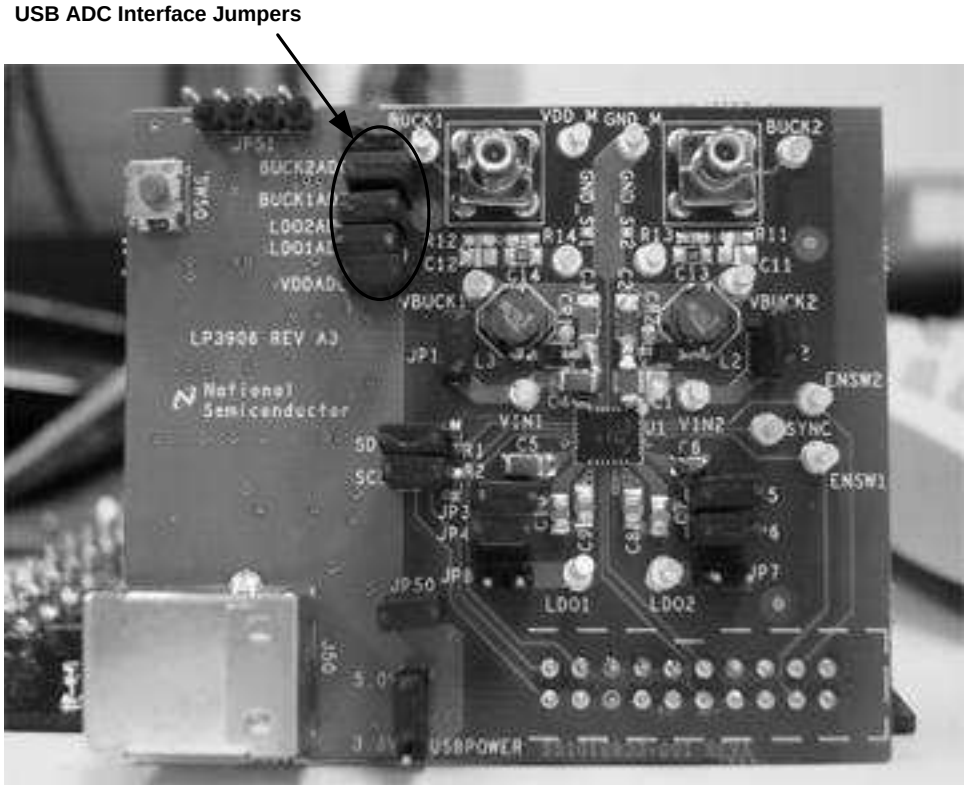


Figure 8. USB Interface ADC Jumpers

6.4 Buck and EN_T Control

The Control / Status Bits Control menu (see middle left section of Figure 4 and Figure 9) controls the following aspects of the chip:

1. **Temp** – Reflects the status of the regulators. If a buck or LDO regulator falls out of regulation because of the temperature, it will be shown in that panel.
2. **System Delay Sequence** – Allows for the user to program a preset delay sequence for the startup of the chip.
3. **Enable ext clock for bucks** – If checked, the user must input a 13 MHz clock to the SYNC pin of the IC. If unchecked, the bucks will run internally with a 2MHz clock.
4. **Spread Spectrum, SS modulation** – May help to reduce noise from the buck switchers. Described in *LP3906 Dual High-Current Step-Down DC/DC and Dual Linear Regulator with I2C Compatible Interface* (SNVS456).

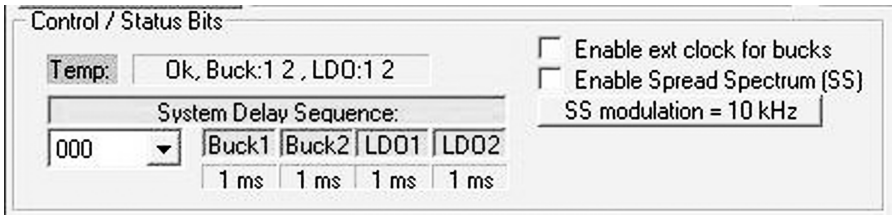


Figure 9. Interrupt Control Interface

7 Using the Evaluation Hardware

7.1 Powering the LP3906 Board

We recommend that the user power the LP3906 through an external power supply if any loads are attached to the regulators. In case no external power supply is available (as for showroom purposes), the USB interface can be used to power the chip.

7.1.1 External supply

The LP3906 Evaluation board can be powered using a battery or wall adapter as described in previous sections. Simply apply the voltage to the VDD_M pin referenced to GND_M.

Before applying power to VDD_M, be sure to disconnect the USB Power Jumper. Failure to do so may damage the USB chip and/or the IC. Full functionality of the GUI will still be available if powered by an external power supply.

7.1.2 USB Interface Supply

In case the external supply or battery is not available, the USB board can be used to power the LP3906 chip. Simply connect the USB Power Jumper to the 5V pin on the LP3906 evaluation board.

NOTE: External power supplies should be DISCONNECTED from the VDD_M pin, if powering from the USB.

The USB interface card can provide the following voltages:

- 5V from USB interface (default setting) -- USBPOWER needs to be set to 5V
- 3.3V -- USBPOWER needs to be set to 3.3V. Useful if the user wants to provide a lower voltage to the IC.

7.2 Enable Configurations Through the 20 Pin Header

Figure 10 shows how to enable or disable different regulators by jumping pins in the 20 pin header. One practical use of grounding the enable pins of the regulators is to signal a System Delay Sequence (EN_T). Using the System Delay Sequence is described in more detail in the datasheet (SNVS456), but the basics are described:

System Delay Sequence Information

- EN_LDO1, EN_LDO2, EN_SW1, and EN_SW2 have internal pullups and are by default ON.
- The power-on sequence (EN_T) is internally pulled down, and is by default OFF.
- If EN_T is connected to VDD or given a positive edge input from 0 to VDD, the enable sequence will start.

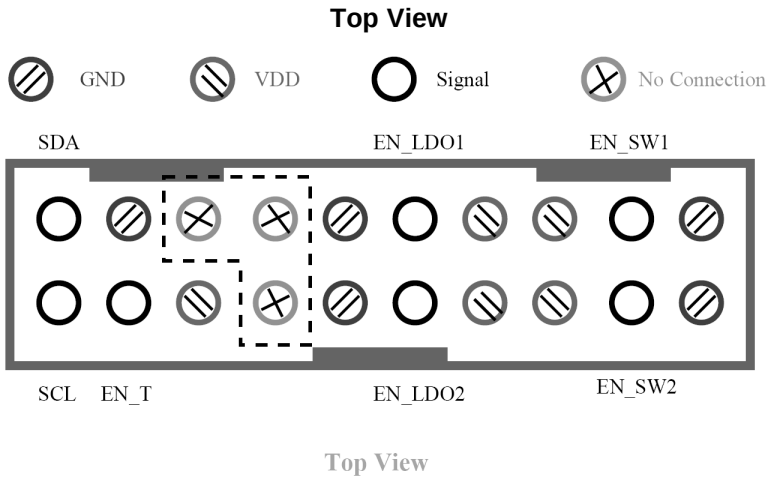


Figure 10. Header Connector

7.3 LP3906 Hardware Block Description

The evaluation board is fully populated with the LP3906.

The LP3906 Evaluation board is designed to allow the user to test each function independently as well as in the system. Jumpers 1-6 as described in the Jumper table allow the VDD and GND path of each of the blocks to be separated from the rest of the blocks. To look at each of the blocks, follow the instructions:

1. Start with all the jumpers connected.
2. Use the provided GUI to disable the desired block.
3. Remove the connecting jumpers based on the jumper table to isolate the power and ground planes of the block under test.
4. Connect a power supply (Vout + 0.3V) to the input of the desired block referenced to its corresponding ground.
5. Enable the block and proceed with normal testing.

The output voltage of the Low dropout regulators can be accessed at the 'Turrets' (LDO1 and LDO2) referenced to GND_M. These are marked on the silk screen of the evaluation board.

The output voltage of the two Buck Regulators can be accessed at the 'Turrets' VBUCK1, VBUCK2 referenced to GND_SW1, and GND_SW2.

External power supplies can be attached to VDD_M referenced to GND_M. The voltage supplied to the system must be between the range of 2.7 to 5.5V.

SMB Connectors

The SMB connectors above VBuck1 and VBuck2 are connected to the SW pin of Buck1 and Buck2, respectively. This will allow the user to monitor the switching of the regulators.

Resistive Pull-ups

The two I2C compatible signals SDA and SCL can be accessed externally via turrets I2C SCL, and I2C SDA. Both lines are pulled up via 22K resistors R1, R2.

External Control Resistor Divider

Each of the Buck Switch Regulators has the option to be externally compensated through the external resistive feedback network shown in Figure 11. If the user wishes to have the chip internally compensated with factory programmed settings, then a 0 ohm resistor should be placed across R14 for Buck 1 and R11 for Buck 2.

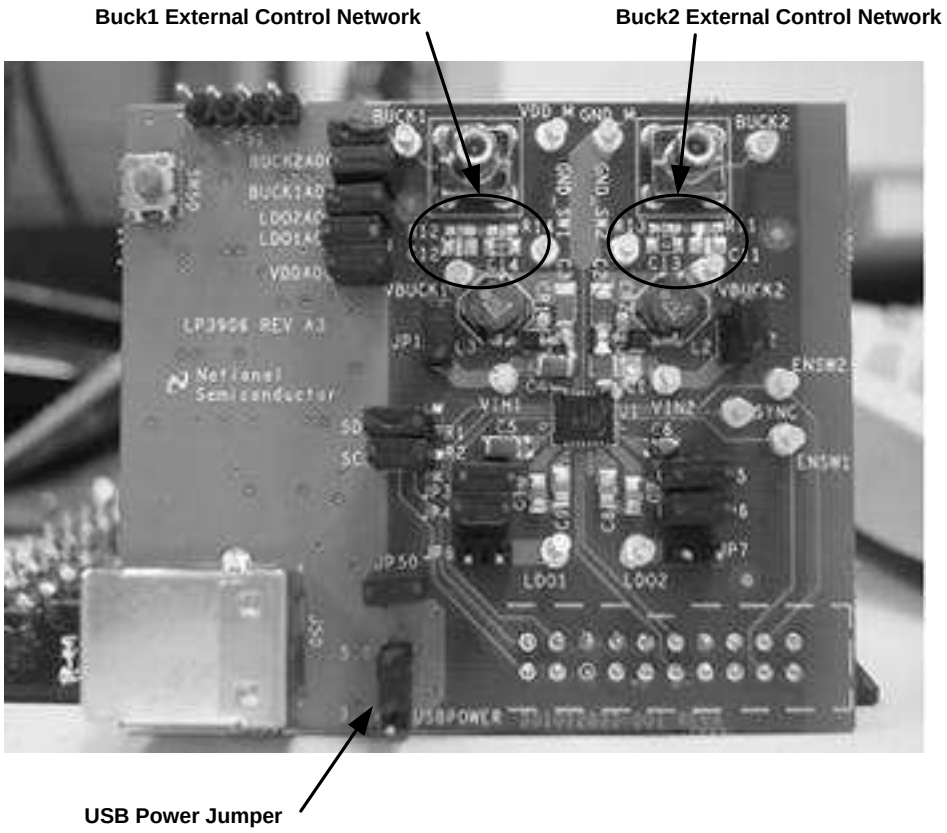


Figure 11. Buck Regulator Feedback Network

8 Jumper Settings

Table 1. Jumper Settings

Jumper	Purpose	Note
JP 1-6	These jumpers connect different Vins to the system VDD (VDD_M). JP1 connects Vin1 to VDD_M. JP2 connects Vin2 to VDD_M. JP3 connects the Buck core VDD to VDD_M. JP4 connects VINLDO1 to VDD_M. JP5 connects VINLDO12 to VDD_M. JP6 connects VINLDO2 to VDD_M.	JP1 and JP2 allow the bucks to be powered from the system power. JP4 and JP6 allow the LDOs to be powered from the system power. JP3 and JP5 powers the internal bias and error amplifiers from the system power. The voltage applied to AVDD and VINLDO12 should be in the range of 2.7 – 5.5V.
JP 7-8	These jumpers connect the output of LDO1 and LDO2 to GND. JP7 connects LDO2 to GND. JP8 connects LDO1 to GND.	These jumpers are used to connect the output of the respective LDOs to GND for short circuit testing purposes.
JP50	This jumper connects the GND of the USB interface with GND_M.	Enable pin logic input: Low = shutdown, High = normal operation. This pin should not be left floating. Short to V_{IN} using attached jumper for normal operation.
USBPOWER	This jumper allows the USB to power the board.	This jumper should be disconnected if powering from an external power supply. It should be set to 5.0V if powering from the USB.
SDA, SCL	These jumpers allow the GUI to interface with the chip.	Connect these jumpers for the GUI to work.
ADC	These jumpers connect outputs of various regulators to the ADCs of the USB.	Needs to be jumped to measure the voltages of different regulators from the GUI.

9 LP3906 Evaluation Board Schematic

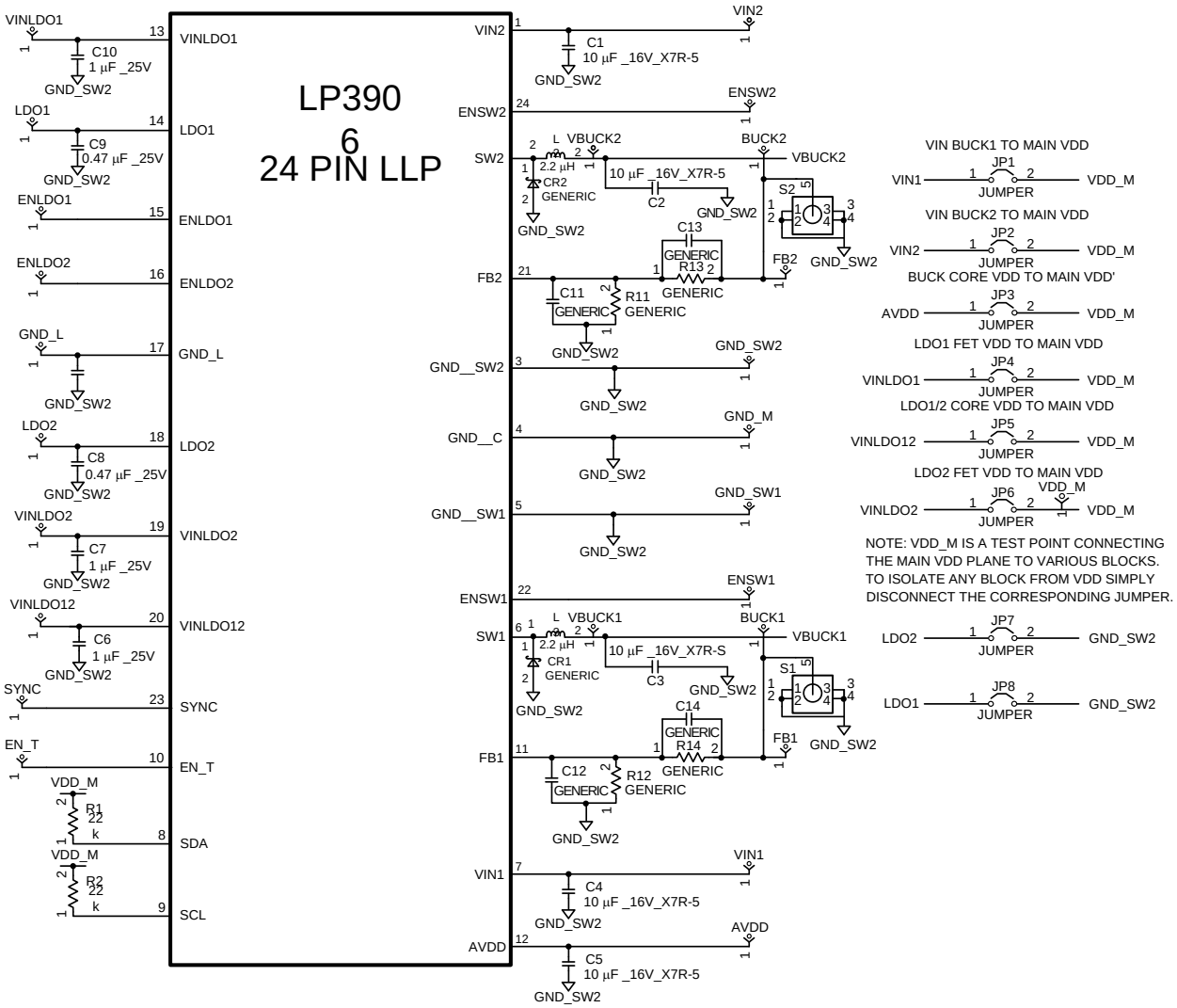


Figure 12. LP3906 Evaluation Board Schematic

10 List of Main Components for LP3906 Evaluation Board (not including USB interface)

Table 2. Main Components for LP3906 Evaluation Board

Reference Designator	Value, Size, Tolerance	Description	Vendor
C1-C5	10uF, 16V, X7R 01206	C3216X7R1C106M	TDK
C6,C7,C10	1uF, 16V, X7R, 0805	C2012X7R1C105K	TDK
C8,C9	0.47uF, 25V, X7R 0805	C2012X7R1E474K	TDK
R1,R2	22K OHM 1/10W 1% 0603 SMD	MCR03EZPFX2202	Rohm
R11, R13	0 OHM 0603 SMD	MCR03EZPJ000	Rohm
S1,S2		SMB Connector 131-1701-206	Emerson
L2,L3	2.2 uH @ I sat 2A	Buck boost inductor NP04SZB 2R2N	Taiyo Yuden
6 × 6mm 48 WQFN package	Power management IC	LP3906	Texas Instruments

11 PCB Layout Considerations

The evaluation board layers from top to bottom are:

1. Top, component side
2. Ground plane
3. Mid signal section
4. Bottom, solder side

For good performance of the circuit, it is essential to place the input and output capacitors very close to the circuit and use wide routing for the traces allowing high currents. Sensitive components should be placed far from those components with high pulsating current. Decoupling capacitors should be close to circuit's VIN pins. Digital and analog ground should be routed separately and connected together in a star connection. It's good practice to minimize high current and switching current paths.

11.1 Low Drop-Out Regulators

Place the filter capacitors very close to the input and output pins. Use large trace width for high current carrying traces and the returns to ground.

11.2 Buck Regulators

Place the supply bypass, filter capacitor, and inductor close together and keep the traces short. The traces between these components carry relatively high switching current and act as antennas. Following these rules reduces radiated noise.

Arrange the components so that the switching current loops curl in the same direction.

Connect the buck ground and the ground of the capacitors together using generous component-side copper fill as a pseudo-ground plane. Then connect this back to the general board system ground plane at a single point. Place the pseudo-ground plane below these components and then have it tied to system ground of the output capacitor outside of the current loops. This prevents the switched current from injecting noise into the system ground. These components along with the inductor and output should be placed on the same side of the circuit board, and their connections should be made on the same layer.

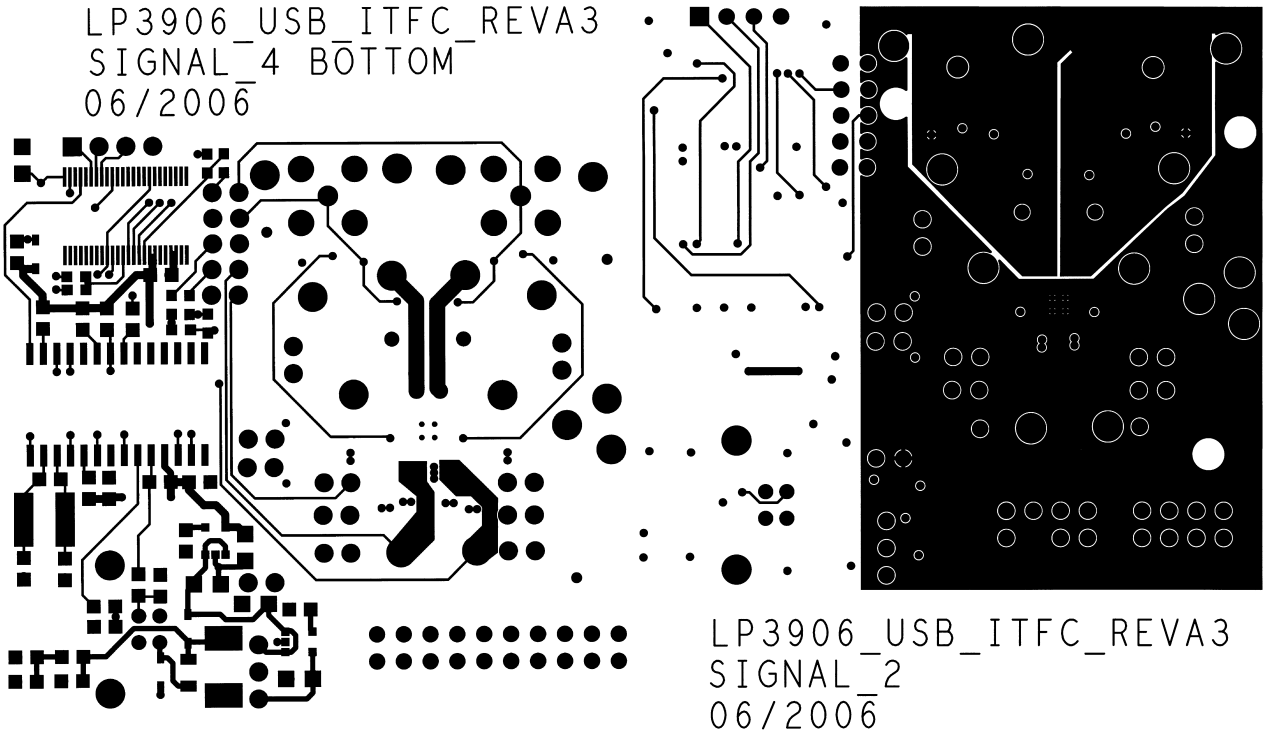
Route noise sensitive traces such as the voltage feedback path away from the inductor. This is done by routing it on the bottom layer or by adding a grounded copper area between switching node and feedback path. To reduce noisy traces between the power components, keep any digital lines away from this section. Keep the Feedback node as small as possible so that the ground pin and ground traces will shield it from the SW or buck output.

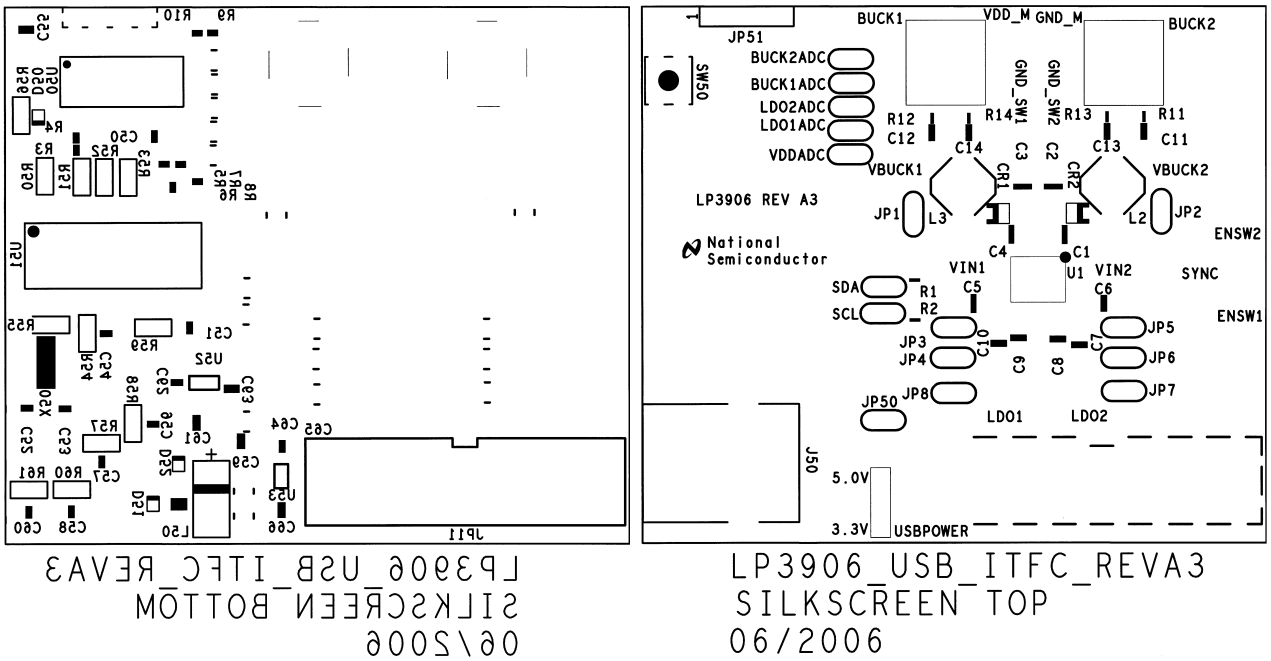
Use wide traces between the power components and for power connections to the DC-DC converter circuit to reduce voltage errors caused by resistive losses.

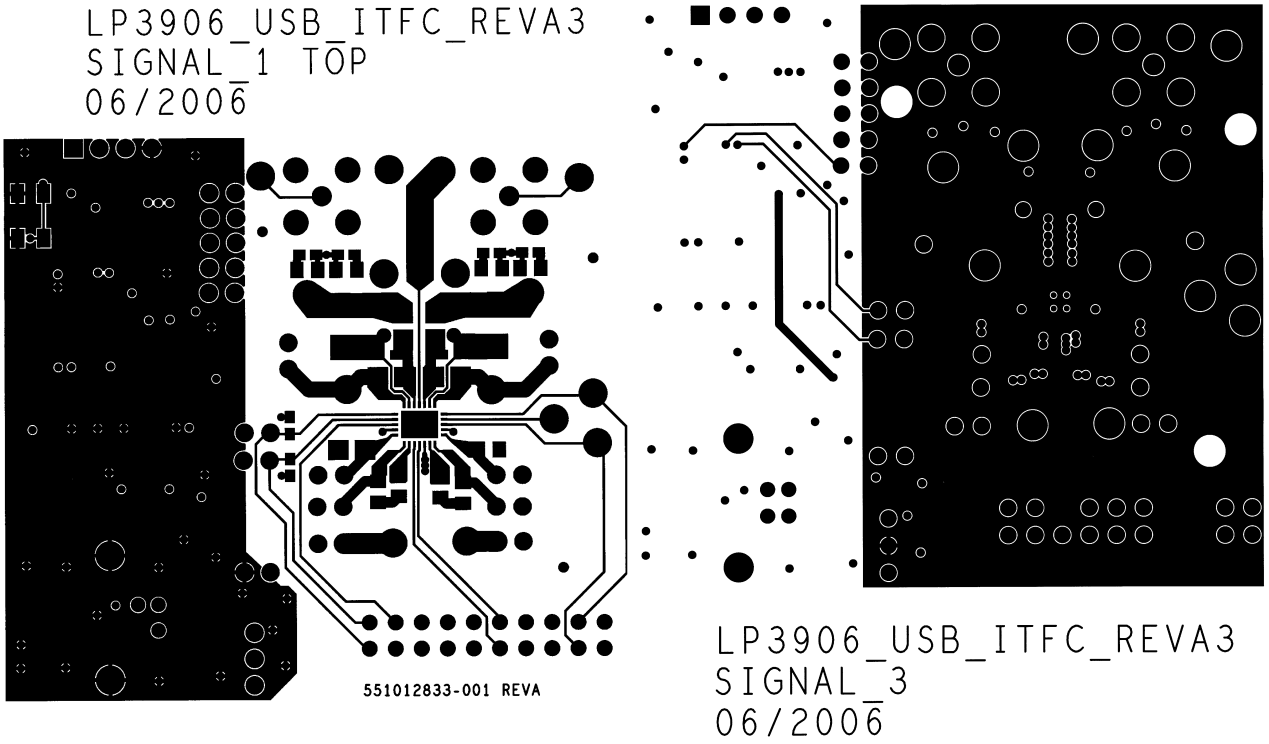
For the sense lines, make sure to use a Kelvin contact connection.

12 Gerber Files

The LP3906 is a four layer board. Following are the Gerber files for the board. The accompanying CD has the Gerber files in Cadence allegro format.







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