Using the LP8754EVM Evaluation Module

User's Guide

Literature Number: SNVU369
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The LP8754 Evaluation Module

This user's guide describes the operation of the evaluation module for the LP8754 Multi-Phase 6-Core Step-Down Converter from Texas Instruments (TI). The user's guide also provides design information including the schematic and Bill of Materials (BOM).

1 Overview

The LP8754EVM customer evaluation module demonstrates the integrated circuit LP8754 from TI. The LP8754 is a high-performance, multi-phase step-down converter designed to meet the power management requirements of the latest applications processors in portable applications. The device contains six step-down converter cores, which are bundled together in a 6-phase buck converter. This document covers user software provided with the EVM and design documentation that includes schematics and parts list.

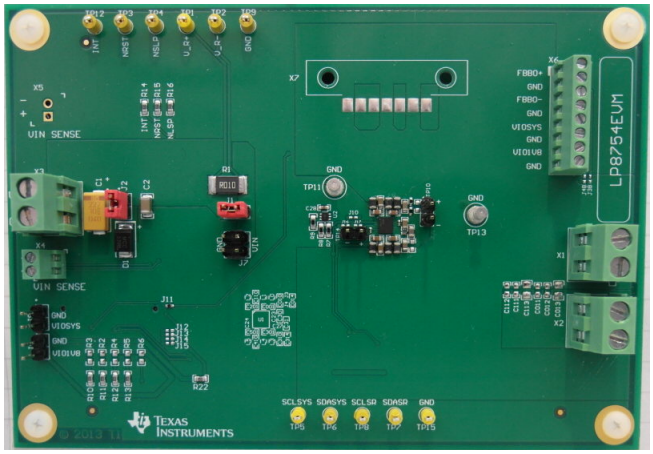


Figure 1. LP8754EVM

The evaluation module consists of two PCB boards, the LP8754 Evaluation Board, and the USB Interface Board. The boards are of the same size, and the LP8754 board is stacked on top of the USB Interface Board.

2 Quick Setup Guide

Many of the components on the LP8754 are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

On opening the LP8754EVM package, ensure that the following items are included:

- LP8754 Evaluation Board
- USB Interface Board
- USB Cable

If any of the items are missing, contact the closest Texas Instruments Product Information Center to inquire about a replacement.

2.1 Installing/Opening the Software

The EVM software is controlled through a graphical user interface (GUI). The software communicates with the EVM through an available USB port. The minimum hardware requirements for the EVM software are:

- IBM PC-compatible computer running a Microsoft Windows® XP or newer operating system
- Available USB port
- Mouse

The latest downloadable software is available at www.ti.com. Download the zip file onto your local hard drive, then unzip this folder. Make sure the USB Interface Board is connected to the Evaluation Board, and connect the USB Interface Board to the PC with the USB cable. Refer to Figure 1.

1. With the power supply disconnected from the unit under test (UUT), open the un-zipped folder, and click on lp8754_nnn.exe (nnn is the version number) to start the software.
2. On the Evaluation SW window bottom right corner you should see text “USB Board connected”. Refer to Figure 2.

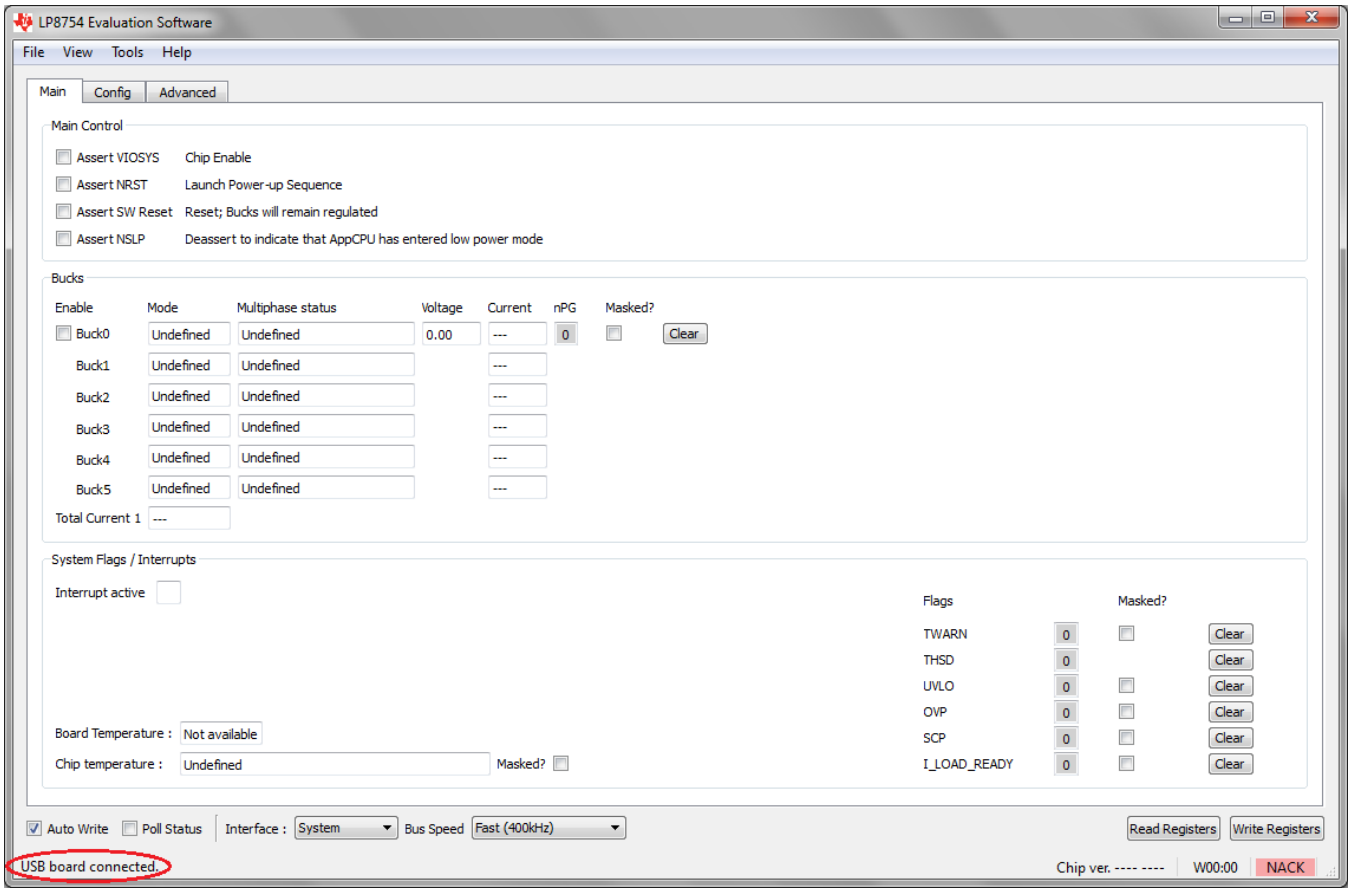


Figure 2. Evaluation Software Graphical User Interface (GUI) When USB Board Connected

2.2 Power Supply Setup

To power up the EVM, one power supply is needed. For full-load testing of the LP8754EVM, a DC-power supply capable of at least 10 A and 4 V is required. 5 A is suggested as a practical minimum for partial load. The power supply is connected to the EVM using connector X3. The power supply and cabling must present low impedance to the UUT; the length of power supply cables must be minimized. Remote sense, using connector X4, can be used to compensate for voltage drops in the cabling.

With the power supply disconnected from the UUT, set the supply to 3.7 V DC and the current limit to 5-A minimum. Set the power supply output OFF. Connect the power supply's positive terminal (+) to VIN and negative terminal (-) to GND on UUT (X3 Power-in terminal block). Check that jumpers on the boards are set as shown in Figure 1 (factory default jumper configuration).

Set power supply output ON, and then continue with the following steps.

1. On Evaluation software GUI, click on Assert VIOSYS. See Figure 3: Marking “1”.
2. Click on Assert NRST. See Figure 3: Marking “2”.
3. Click on Read Registers button. You should see ready message on green background next to the Read Registers button. See Figure 3: Marking “3”.
4. Check that the GUI indicates "PWM" under "Mode" and "Master; 1/6 Phases Active" under "Multi-phase" status. See Figure 3: Marking “4”.The EVM is now ready for testing with default register settings loaded.

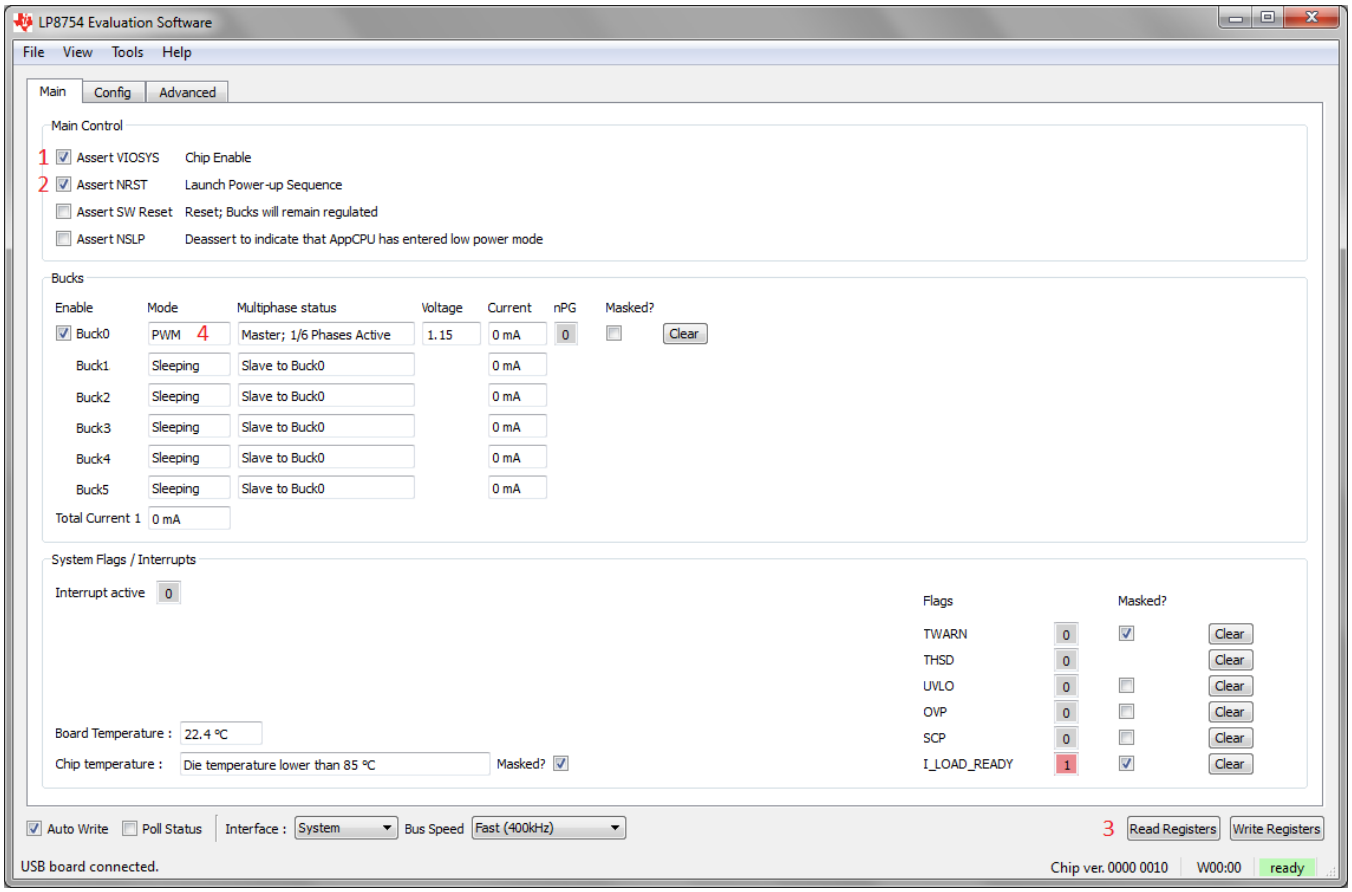


Figure 3. Evaluation Software GUI Showing Steps Needed to Power up the LP8754

2.3 Notes on Efficiency Measurement Procedure

Output Connections: An appropriate electronic load or high-power system source meter instrument, specified for operation down to 500 mV, is desirable for loading the UUT. The maximum load current is specified as 10 A. Be sure to choose the correct wire size when attaching the electronic load. A wire resistance that is too high will cause a voltage drop in the power distribution path which becomes significant compared to the absolute value of the output voltage. Connect an electric load positive terminal (+) to X1 and negative terminal (-) to X2. It is advised that, prior to connecting the load, it be set to sink 0A to avoid power surges or possible shocks.

Voltage drop across the PWB traces will yield inaccurate efficiency measurements. For the most accurate voltage measurement at the EVM, use TP14 to measure the input voltage and TP10 to measure the output voltage.

To measure the current flowing to/from the UUT, use the current meter of the DC power supply/electric load as long as it is accurate. Some power source ammeters may show offset of several milliamps and thus will yield inaccurate efficiency measurements. In order to perform very accurate I_q measurements on the UUT, disconnect input protective Zener diode D1 by removing the shunt J2 from the board. When connected, this diode will cause some leakage, especially on high VIN voltages. Also, the output voltage ADC on the USB Interface Board will load the output of LP8754 with a resistance in order of a hundred of kΩ. The 0-Ω resistor between the pads of J11 on the lower left corner of the EVB may also be removed (see Section 6).

3 GUI Overview

The evaluation software has the following tabs: Main, Config, and Advanced. The three tabs together provide the user access to the whole register map of LP8754.

3.1 Main Tab

The Main tab has the elemental controls for the EVM and provides a view to the chip status. Starting from top, the main controls are:

- Assert VIOSYS: This checkbox will assert 1.8-V voltage to LP8754 VIOSYS pin. This pin will enable the chip internal voltage reference and LDO, release POR, and launch OTP read cycle. The VIOSYS voltage is the reference voltage for the System I^2C bus.
- Assert NRST: This checkbox will assert 1.8-V voltage to LP8754 NRST pin. Asserting NRST will launch power-up sequence.
- Assert SW Reset: To perform a complete SW reset to the chip, assert and de-assert this checkbox. See the LP8754 datasheet for explanation of LP8754 reset scenarios.
- Assert NSLP: When this bit is asserted it tells LP8754 that the device it is powering is in a high-load condition state. On LP8754 this effectively prevents the bucks from entering the Low-Power PFM Mode (ECO).

NOTE: The recommended start-up sequence for LP8754 is to first assert VIOSYS, then write all needed configuration bits by using the GUI, and then to assert NRST.

NOTE: The NRST pin is the reference for the DVS (Dynamic Voltage Scaling) bus (that is, SmartReflex™ bus). NRST needs to be asserted before the chip will acknowledge any transmission on the DVS bus.

The Bucks section provides status information for all the 6 buck cores. The Mode field provides information on each of the buck core and can have any of the values given in Table 1:

Table 1. Mode Information

Buck Mode	
Disabled	Buck state machine in 'disable'
Soft Startup	Buck state machine in 'soft startup'. May occur when too much loading is present when powering-up the buck.
PWM	Pulse Width Modulation
PFM	Pulse Frequency Modulation
ECO	PFM with 'low power coasting' mode enabled. This means that lots of analog resources are disabled between PFM bursts. Reaction time to load transients is compromised, while Iq is minimized.
Sleeping	Multi-phase slave is passive.

The "Multi-phase Status" info field tells whether a buck core is configured as a master or slave. The field also tells how many phases are active.

An ADC on the USB interface card is connected to measure the output voltage of the buck converter, and this is displayed on GUI.

The "System Flags / Interrupts" section gives data on system faults and warnings. If the interrupt is set for any reason the Interrupt active field shall show ‘1’ on red background. The flag causing the interrupt will also be set on the Main tab. Interrupts on LP8754 can only be cleared by writing ‘0’ to associated registers. Any individual flag can be cleared by clicking the Clear button next to each flag field. The USB Interface Board uses an I^2C-accessible temperature sensor IC to sense the EVB temperature near the LP8754 IC. This information is presented in the "Board Temperature" field. LP8754 register 0x0D provides a coarse temperature indication of the chip. This info is interpreted into the "Chip Temperature" field when the "Poll Status" option is selected.

At the bottom of the GUI window is the "Auto Write" checkbox. If "Auto Write" is checked (default) any checking, un-checking or pull-down menu selections will immediately launch I^2C writes to the chip register(s). If not checked, the user can update the chip registers to correspond the configuration selected on the GUI by clicking "Write Registers".

If "Poll Status" is selected the software sends a query to the LP8754 at a fixed interval in order to detect the status of the chip, including operation mode, multi-phase status, and output current. If not selected, user can read the registers by applying "Read Registers". On the EVM both System I^2C and DVS (Dynamic Voltage Scaling) (that is, SmartReflex) buses can be used to interface the chip. The interface to be used can be selected from the Interface pull-down menu. "Bus Speed" pull-down menu selections are given in Table 2 below and are instantly applied for both buses. Notice that for DVS bus to work, NRST needs to be high.

Table 2. I^2C-Compatible Bus Support

Bus Speed Selection	Explanation
Fast (400 kHz)	Fast I^2C-compliant operation at 400 kHz
Fast++ (3.4 MHz)	I^2C protocol data transfer with 3.4 MHz clock rate. No writing of master code needed, but can done. Input filters correspond to HS lengths – 10 ns minimum filter length for SCL and SDA:
High-Speed (3.4 MHz)	HS I^2C-compliant data transfer with master codes.

3.2 Other Tabs and Menus

The "Tools" pull-down menu hosts another way of accessing the LP8754 registers. The "Direct Register Access" tool can be used to read or write any register. When using direct register access, un-checking the poll status checkbox is recommended. This way the GUI will only do the reads and writes commanded from the direct access dialog.

The "Config" and "Advanced" tabs provide the user with pull-down menus and check-boxes for the part of the register space that is not covered by the Main tab, such as output voltage control. These controls are self-explanatory. Please refer to the LP8754 datasheet for explanation of the functions.

3.3 Console

To show or hide the console, toggle the option in View pull-down menu. The console can be used to access the LP8754 registers. Registers can be read or written simply by referring to the logical registers by their name. The console has a number of integrated macros that are listed in Table 3.

Table 3. Console Macros

Command	Parameters	Explanation
register_name	= register value | -	Write a value to writable I^2C register or logical register. If no parameter given, will return the current register value. The logical register names are the same as given in the datasheet, and must be in uppercase.
		Example: VSET_B0 = 40
wait	(time)	Wait for time given in ms. Useful in loops.
advanced		Change to advanced user mode.
user		Return from advanced to regular user mode.
iout	(buck number)	Returns the measured load current of the chosen buck core.
i2c_bus	sr | sys | -	Change serial bus communications from the console and the GUI to be made with the specified bus. If called with no parameter treated as query and current selection is returned.
0x	address = data or address[bits] = data	I^2C read or write command. addr = value examples: 0x12 = 0xaa 0x12[7] = 1 0x12[3:0] = 15

The console supports use of scripts. If a text file containing commands supported by the console is stored in the same folder with the evaluation software executable, then the script can be launched from the console by typing the text file name, like script.txt. For demonstration purposes, the evaluation software comes with a set of scripts, which are loaded when Power Saver, Balanced, or High Performance buttons on the "Advanced" tab are clicked. These scripts (saved as script1.txt, script2.txt and script3.txt) will load a collection of register settings that will save energy, maximize load transient performance, or achieve a balance between the two. Clicking the User button will load a script "script4.txt". By default this file contains a demo which loops through all output voltage settings (VSET_B0). User can modify this file for specific register settings.

4 Bill of Materials

Designator	Description	Manufacturer	Part Number	Qty.
!PCB	Printed Circuit Board	Any	SV600763-001 REV A	1
C001, C201, C301, C501	CAP, CERM, 10µF, 10V, ±10%, X5R, 0603	TDK	C1608X5R1A106M	4
C1	CAP, TANT, 220µF, 10V, ±10%, 0.05Ω, 7343-31 SMD	AVX	TPSD227K010R0050	1
C2	CAP, CERM, 100µF, 6.3V, ±20%, X5R, 1206	MuRata	GRM31CR60J107ME39L	1
C010, C30, C31, C110, C310, C410	CAP, CERM, 22µF, 10V, ±20%, X5R, 0603	Samsung	CL10A226MP8NUNE	6
C23, C24, C27	CL03 Series 0201 1000nF 6.3 V 20 % X5R SMD	Samsung	CL03A105MQ3CSNH	3
C28	CAP, CERM, 0.1µF, 10V, ±10%, X5R, 0402	MuRata	GRM155R61A104KA01D	1
D1	Diode, Zener, 5.1V, 5W, SMB	Micro Commercial Co	SMBJ5338B-TP	1
H1, H2, H3, H4	MACHINE SCREW PAN PHILLIPS 4-40	B&F Fastener Supply	NY PMS 440 0050 PH	4
H5, H6, H7, H8	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	4
H19, H20, H21, H22	M4 CIRC CLEARANCE SPACER 5MM	Harwin Inc	R40-6710594	4
J1, J2, J8, J9	Header, TH, 100mil, 2x1, Gold plated, 230 mil above insulator	Samtec, Inc.	TSW-102-07-G-S	4
J3, J4, J11	RES, 0 ohm, 5%, 0.063W, 0402	Vishay-Dale	CRCW04020000Z0ED	3
J5	Connector, SMT, High Speed, 20 pairs	Samtec, Inc.	QTE-020-01-L-D-A	1
J7	Header, TH, 100mil, 2x2, Gold plated, 230 mil above insulator	Samtec, Inc.	TSW-102-07-G-D	1
L0, L1, L2, L3, L4, L5	Inductor, Multilayer, Ferrite, 470nH, 2.7A, 0.04 ohm, SMD	MuRata	LQM21PNR47MGH	6
R1	RES, 0.01Ω, 1%, 3W, 2512 High Power Current Sense Chip Resistor	Bourns	CRA2512-FZ-R010ELF	1
R7, R8, R9	RES, 1.8kΩ, 5%, 0.1W, 0603	Vishay-Dale	CRCW06031K80JNEA	3
R10, R11, R12, R13, R14, R15, R16, R22	RES, 0 ohm, 5%, 0.1W, 0603	Vishay-Dale	CRCW06030000Z0EA	8
SH-J9, SH-J12	Shunt, 100mil, Gold plated, Black	3M	969102-0000-DA	2
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP12, TP15	Test Point, TH, Miniature, Yellow	Keystone	5004	11
TP11, TP13	Terminal, Turret, TH, Double	Keystone	1502-2	2
U1	LP8754 Multi-phase 6-Core Step-Down Converter, YFQ0049AEAK	Texas Instruments	LP8754YFQT	1
U2	Low Power Digital Temperature Sensor With SMBus/Two-Wire Serial Interface in SOT563, DRL0006A	Texas Instruments	TMP102AIDRL	1
X1, X2, X3	PC terminal block, Pitch: 5.08 mm, Number of positions: 2	Phoenix Contact	1715721	3
X4, X5	Phoenix Contact screw terminal 2 way, 2.54mm pitch	Phoenix Contact	1725656	2
X6	Phoenix Contact screw terminal 8 way, 2.54mm pitch	Phoenix Contact	1725711	1

5 Board Layout

This section describes the board layout of the LP8754EVM. See LP8754 data sheet for specific PCB layout recommendations.

The board is constructed on a 4-layer PCB. Figure 4 shows the top view of the entire board and Figure 5 through Figure 10 show the component placement, layout and 3D view close to the LP8754 device. Vias under the LP8754 are filled microvias from top layer to the GND plane (layer 2), buried vias between 2nd-layer and 3rd-layer and microvias from 3rd-layer to bottom layer.

Routing is mostly done on top and bottom layers. Top layer contains the large copper area connecting the VOUT pads of the inductors and output capacitors together and to the load terminals. 2nd layer is the ground plane and 3rd layer is the VIN plane. Also the bottom layer contains large copper area filled with ground. Input capacitors are placed as close to the LP8754 as possible for keeping the critical VIN and GND traces short. Output capacitors and inductors are placed around the input capacitors. Using the 0603 size input and output capacitors and 2.0 mm x 1.2 mm size inductors the total solution size is about 82.5 mm^2.

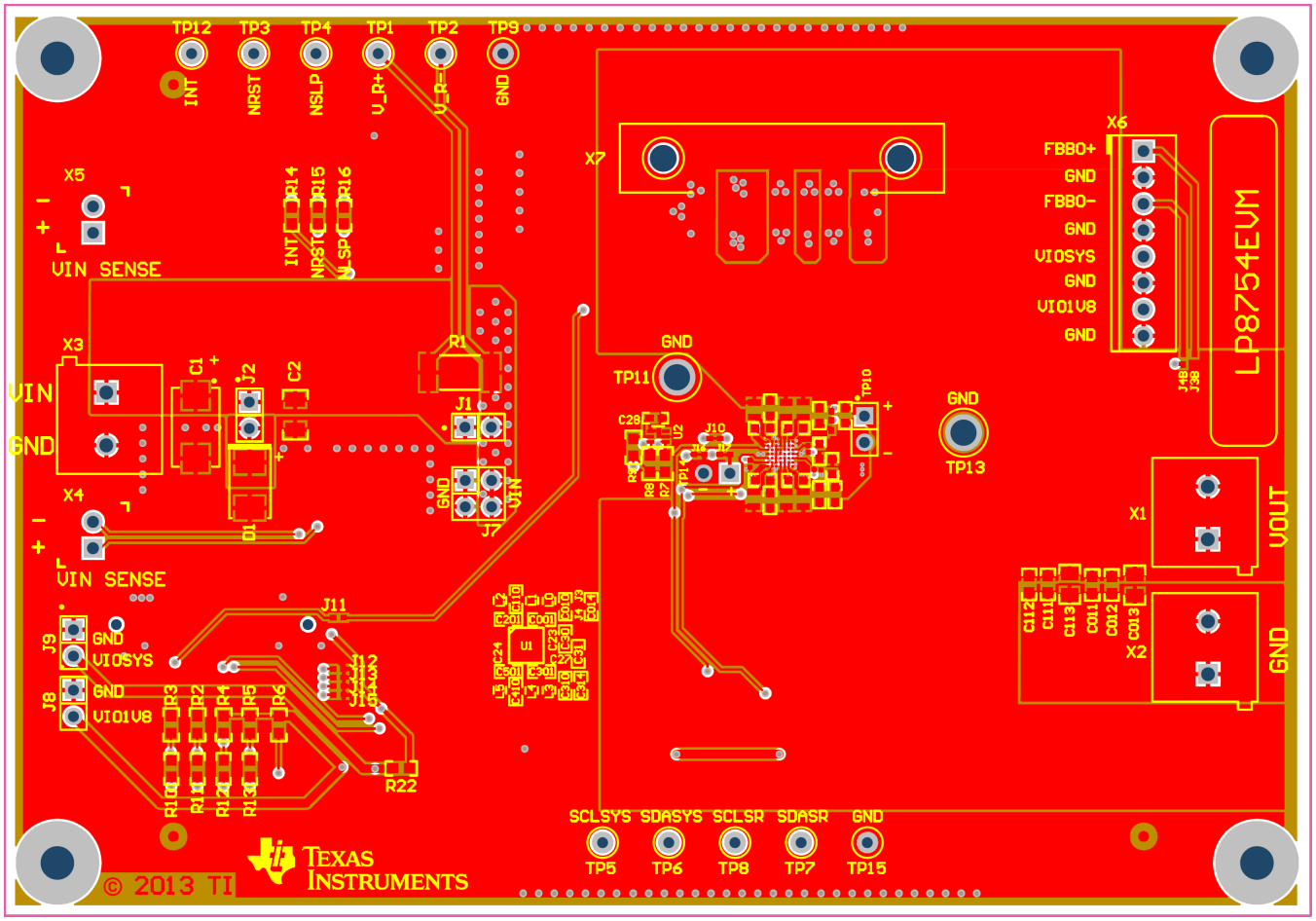


Figure 4. Top view of the LP8754EVM

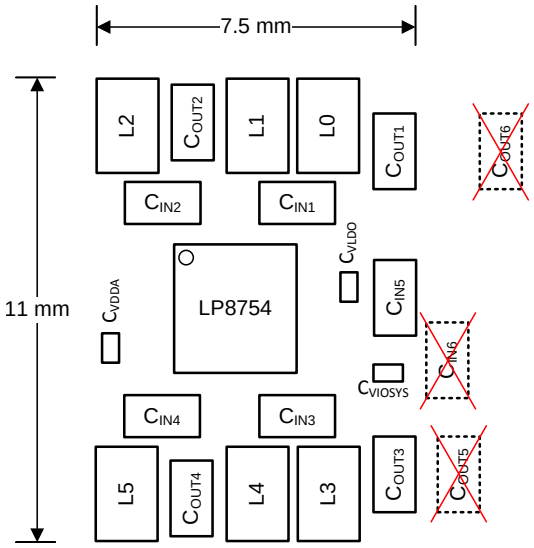


Figure 5. Component placement near the LP8754. Capacitors marked with X are optional.

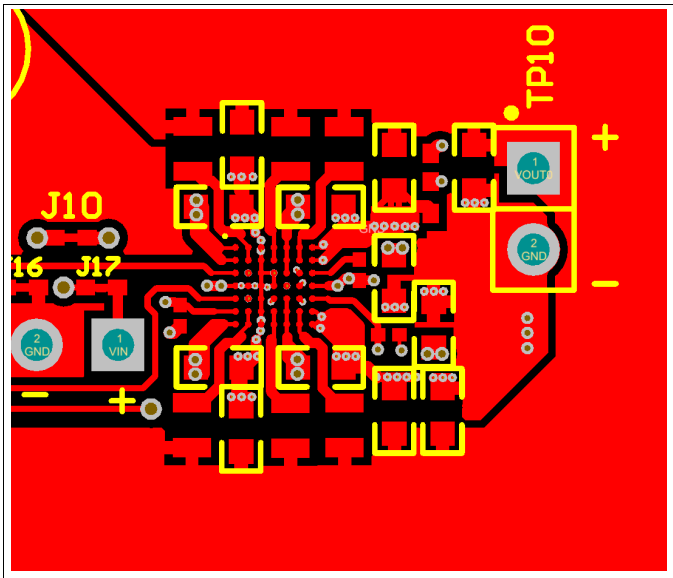


Figure 6. Top-layer. Input capacitors are placed close to the LP8754 and routed on top layer. GND nets are connected to the GND plane (2nd layer) with microvias. VIN nets are connected to the VIN plane (3rd layer) with vias in pads of the input capacitors. VOUT pads of the output capacitors and inductors are connected together with large copper area.

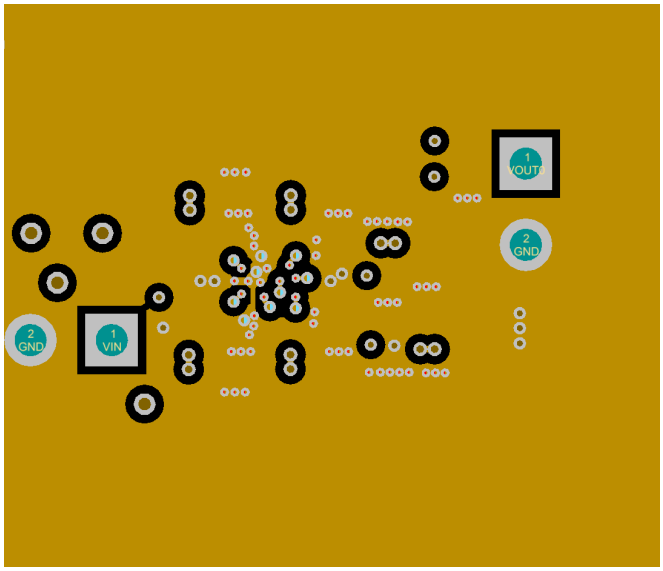


Figure 7. 2nd Layer (GND). GND plane kept intact under the high current traces to provide shortest possible return path for high frequencies.

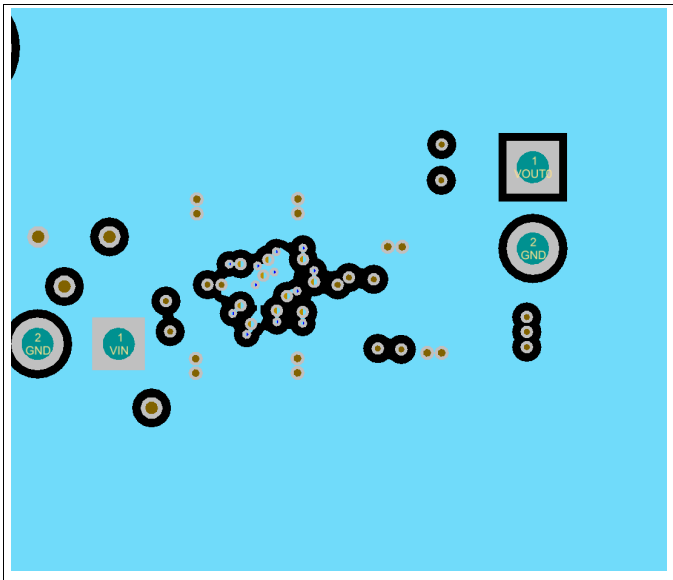


Figure 8. 3rd Layer (VIN). Plane kept intact around the LP8754. Below the LP8754 is small ground area connecting the microvias (from 3rd to bottom layer) and buried vias (from 2nd to 3rd layer).

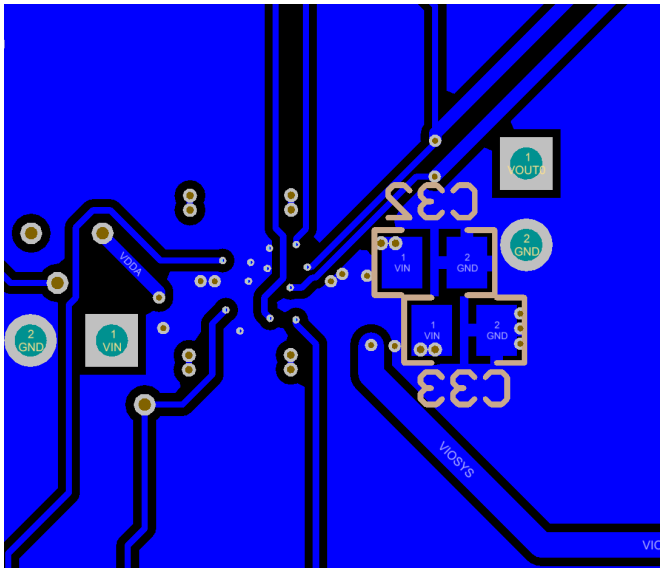


Figure 9. Bottom-Layer and Silk. Footprints for optional input capacitors C32 and C33. GND filling in bottom layer for sinking heat through the GND vias.

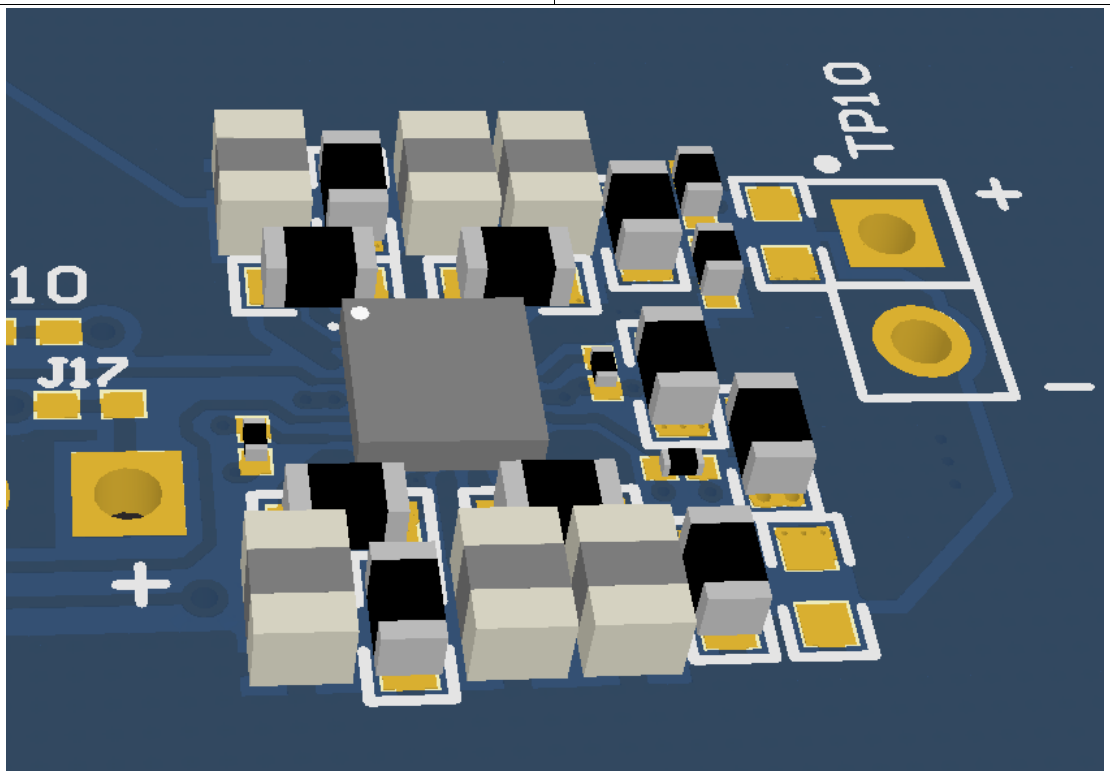
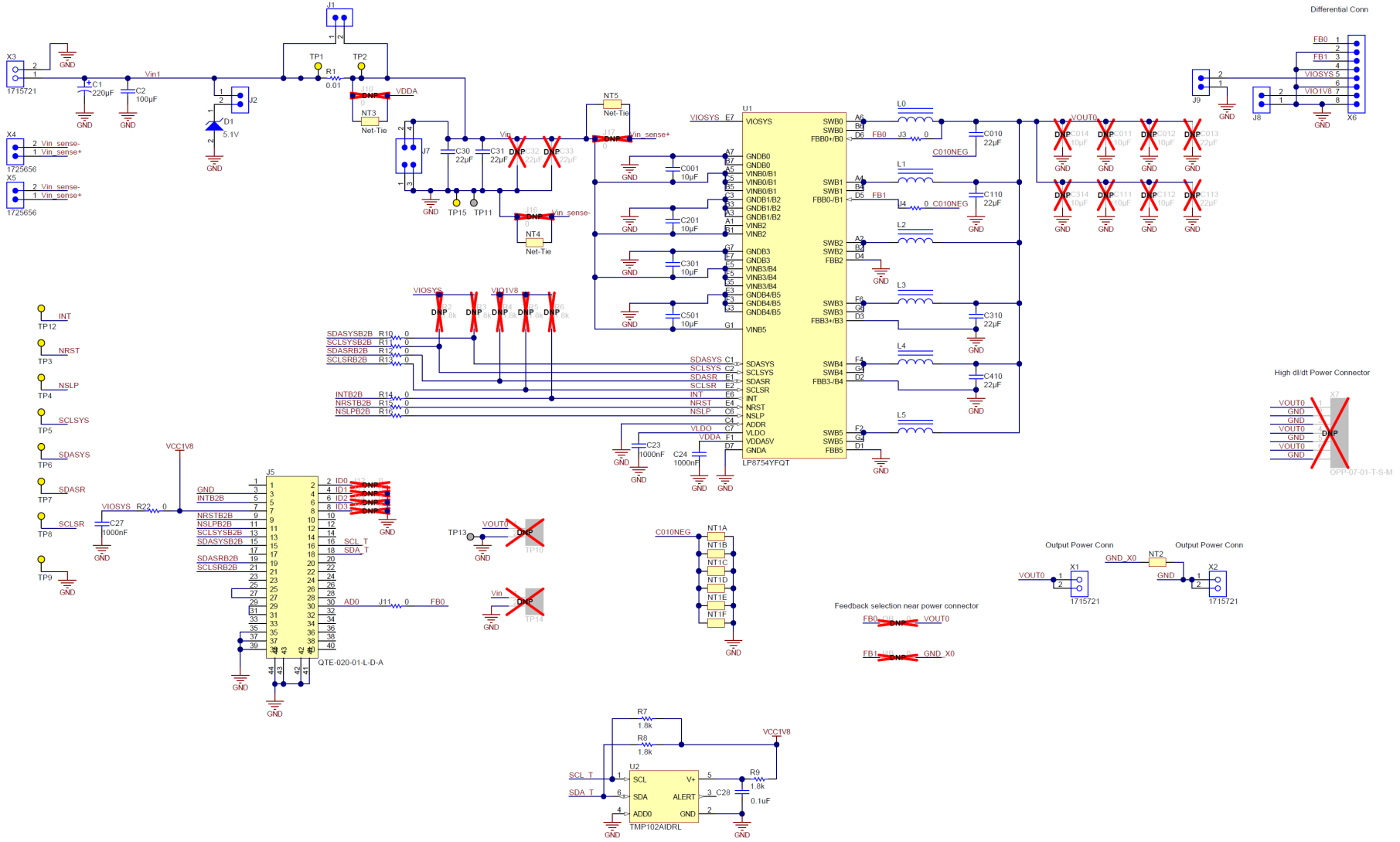


Figure 10. 3D View Showing the LP8754 and Nearest Components

6 LP8754 Schematic



STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms and conditions that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.

   2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

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