



Table of Contents

1 Introduction.....	2
2 Width/Spacing Proposal for Escapes.....	3
3 Stackup.....	4
4 Via Sharing.....	5
5 Floorplan Component Placement.....	6
6 Critical Interfaces Impact Placement.....	7
7 Routing Priority.....	8
8 SerDes Interfaces.....	9
9 DDR Interfaces.....	10
10 Power Decoupling.....	13
11 Route Lowest Priority Interfaces Last.....	14
12 Summary.....	15

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

The AM62Ax is based on the Cortex-A53 microprocessor, M4F microcontroller with dedicated peripherals, 3D graphics acceleration, dual display interfaces, and extensive peripheral and networking options for a variety of embedded applications. The AM62Ax is available in a 18-mm × 18-mm FBGA package with a 0.8-mm ball pitch. The package BGA design is built leveraging TI Flip Chip BGA Technology (FC-BGA) technology. This document is intended to provide a reference for escape routing on the AM62Ax device. Care must be taken to route signals with special requirements such as DDR, high speed interfaces. Refer to the [High-Speed Interface Layout Guidelines](#) and [DDR Routing Guidelines](#) for more details. Details on Power Delivery Network are provided in [AM62x PDN Application note](#) and any routing and layout requirements specified in those documents supersede the generic requirements provided here.

2 Width/Spacing Proposal for Escapes

The AM62Ax has been designed to support the following. The AM62Ax package supports a similar feature set as several other competing solutions with smaller package area and wider line width. This solution reduces PCB foot print and utilizes lower cost PCB rules, enabling compact and low-cost systems.

Table 2-1. Width/Spacing Proposal for Escapes

PCB Feature	PCB Routing Requirements	Comments
Minimum via diameter	18 mils	Via pads dia - 18 Mils Via hole dia - 8 Mils
Via hole size	8 mils	
Minimum trace width/spacing required in the BGA breakout (Inner Layer)	Trace width – 3.5 mils Spacing – 3.49 mils	
Minimum trace width/spacing required in the BGA breakout (External Layer)	Trace width – 3.5 mils Spacing – 4 mils	
Number of layers used for escape	8	<ul style="list-style-type: none"> • Top (1 Layer) • Signal (3 Layer) • Power (3 Layer) • Bottom (1 Layer)
BGA land pad size	18 mils	
Package Size	18 mm x 18 mm	
PCB layers (signal routing, total) recommended		<ul style="list-style-type: none"> • Top (1 Layer) • Signal (3 Layers) • Power (3 Layers) • Ground (4 Layers) • Bottom (1 Layer)

3 Stackup

PCB stack-up is one of the first and most important considerations in realizing a successful PCB. The AM62Ax device supports a BGA array of 22x22 with a 0.8-mm pitch and a body size of 18 mm. Due to the number of rows of signal balls around the periphery, TI recommends three signal routing layers. PDN compliance and robustness is critical to meet all the performance objectives of the device and associated peripherals. To enable this, TI recommends allocating three layers for power planes. Ground planes must be added adjacent to the power planes and adjacent to the outer layers for shielding and controlled impedance routing. High speed interfaces such as DDR, CSI, and USB require ground planes for impedance matching. Additionally, to meet the higher DDR interface speeds, ground layers both above and below the DDR signals are recommended. The escapes and routing on the AM62Ax board design was achieved with 12 layers as shown in the following table.

Table 3-1. Example PCB Layer Stack-up

PCB Layer	Layer Routing, Planes or Pours
Layer 1	Component pads, ground, and signal escapes
Layer 2	Ground
Layer 3	Signal Routing
Layer 4	Ground
Layer 5	Signal Routing
Layer 6	Power/Ground ref for DDR
Layer 7	Power
Layer 8	Power
Layer 9	Ground
Layer 10	Signal Routing
Layer 11	Ground
Layer 12	Component pads, power, and ground routes

An example 12-layer board stack-up for AM62Ax is described above. This board is designed for optimum signal integrity on the high-speed interfaces while limiting the board size. The AM62Ax board is implemented without HDI (High Density Interconnect) and does not use micro vias, which are both intended to save board cost. All vias on the AM62Ax board are Plated Through Hole (PTH) and pass completely through the board. Proper analysis shall be performed to validate both signal and power integrity, if further optimizations are required to reduce PCB stack-up and/or routing rules illustrated in this document.

4 Via Sharing

The FC-BGA pattern implemented on the AM62Ax design offers opportunities for via sharing. Vias are shared across BGA pins. [Figure 4-1](#) and [Figure 4-2](#) show the via sharing opportunities for VDD_LDDR4 and VSS power supplies, respectively. Via sharing across BGA pins provides for easier escape routing and also robust electrical connection by connecting multiple pins.

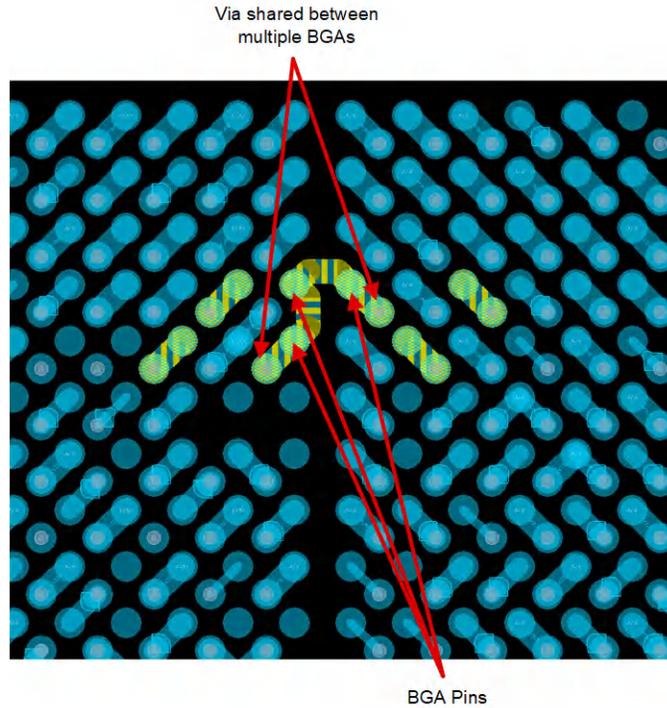


Figure 4-1. Via Sharing for VDD_LPDDR4 Domain

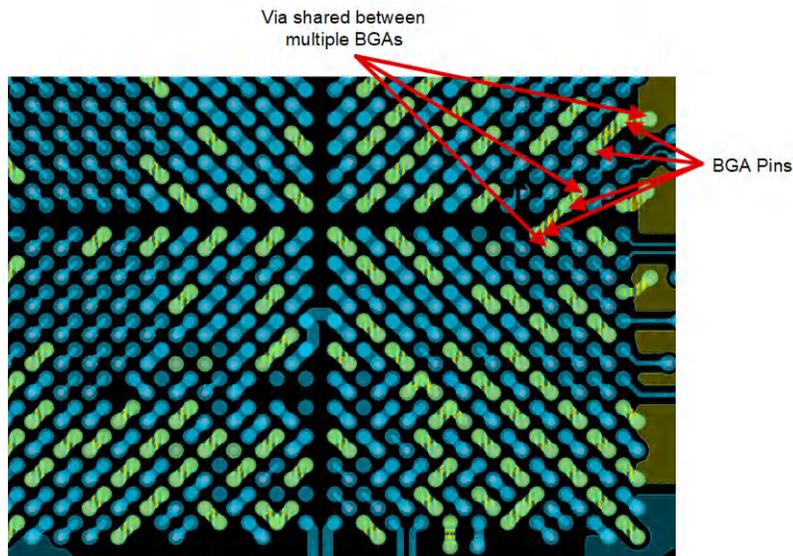


Figure 4-2. Via Sharing for VSS

6 Critical Interfaces Impact Placement

Placement of the AM62Ax device and some of the component and/or connectors is also dictated by some of the highest performance interfaces, such as DDR, CSI, USB, and so forth. Additionally, due to the PCB losses at multi-gigabit rates, there are routing distance limits that may also limit component placement.

7 Routing Priority

As indicated above, critical interfaces affect component placement options. The next step in PCB design is to prioritize routing to these critical interfaces. Those with higher priority must be completed before implementing those of lower priority. It is imperative to route interfaces with the higher priority first. PCB layout teams often end up in a time intense, iterative process with sub optimal results when routing priorities are not established.

The table below lists a recommended priority order for interfaces contained on the AM62Ax family of devices. Individual design requirements may drive a need for adjustment of the priorities but this serves as a good baseline and has been used for the board example illustrated in this document.

Table 7-1. Routing Priority

Interface	Routing Priority
DDR4/LPDDR4	10 (Highest Priority)
CSI	9
OSC	8
USB2, OSPI	8
Power distribution	7
RGMII	6
eMMC	5
Clocks	5
MII / RMI	4
SPI	4
Motor control	4
Analog	3
GPMC	2
GPIO	1
UART / CANUART	1
I2C / Temp Diode	1 (Lowest Priority)

The multi-gigabit DDR (dual data-rate) interface is the most critical due to its data rate and loss concerns. DDR is at the top of the priority list because it is very sensitive to PCB losses. Additionally, being single ended in nature makes it highly susceptible to signal integrity issues such as crosstalk, especially at the high speeds targeted in this design. Next in the priority list is the CSI (Camera Serial) interface. The limited length for these routes might affect the PCB placement of the CSI connector and the AM62Ax device. CSI signals are found on the outer layers of the BGA footprint allowing some of the CSI traces to escape from the BGA without vias.

The asynchronous and low speed interfaces are at the bottom. This leaves the synchronous and source-synchronous interfaces on the top ordered by data rate. The one surprise may be power distribution. If left to last, it results in poor decoupling performance or current starvation and excessive power supply noise due to insufficient copper to carry the power and ground currents. **Space for copper and decoupling must be allocated before routing the middle and low priority interfaces.**

8 SerDes Interfaces

The package BGA ball map is also arranged to support routing the high priority interfaces first. Therefore, the SerDes CSI interfaces are located close to the outer rings. The lanes located on the outermost row of BGAs can be escaped on the top layer. The lanes located on inner BGA rows require vias to escape as a differential pair on the bottom or on an interior layer. The BGA map facilitates this for inner rows. See [Figure 8-1](#) for an example of the SerDes signals on the AM62Ax board on the top layer and on an inner layer. Wide traces can limit the signal loss but could violate the impedance requirements. For more detailed information on routing Serdes signals, refer to the document on [High-Speed Interface Layout Guidelines](#).

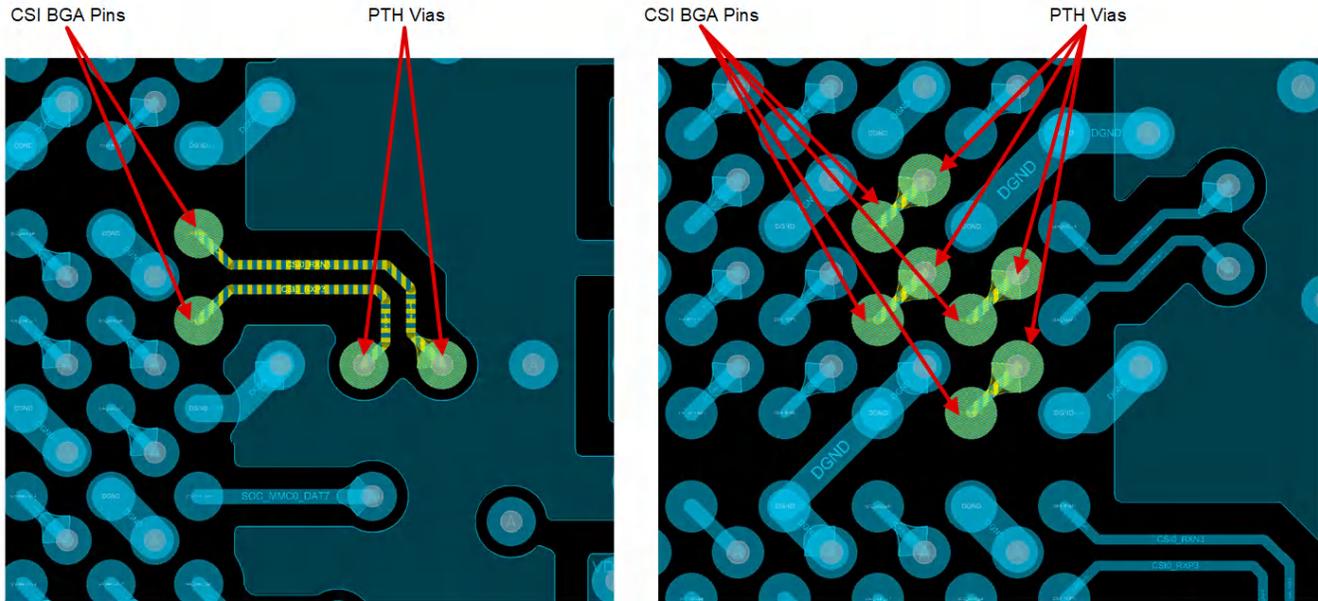


Figure 8-1. Serdes CSI Escapes for Top Layer (Left) and Inner Layer (Right)

9 DDR Interfaces

The AM62Ax SoC supports connection to either a DDR4 or LPDDR4 device. The DDR signals must be routed at the highest priority, as noted in [Table 7-1](#). Refer to the [DDR Routing Guidelines](#) document for detailed recommendations for DDR routing. The images below show the BGA breakout for the DDR interface on the AM62Ax Board. Routing for both DDR4 and LPDDR4 use a similar escape, with LPDDR4 requiring a lesser number of signals.

The DDR SDRAM memory devices are normally arranged so that the data group balls are closest to the AM62Ax device. The Package BGA ball map has been carefully planned to place the DDR address and command signals between data byte lanes 0 and 1 and data byte lanes 2 and 3.

[Figure 9-1](#) and [Figure 9-2](#) illustrate how to escape the DDR byte lanes 0 and 1, respectively. Similarly, [Figure 9-3](#) and [Figure 9-4](#) illustrate the escape of DDR byte lanes 2 and 3, respectively. The use of Plated Through Hole (PTH) vias make the routing of these signals between the SoC and SDRAM possible on any layer.

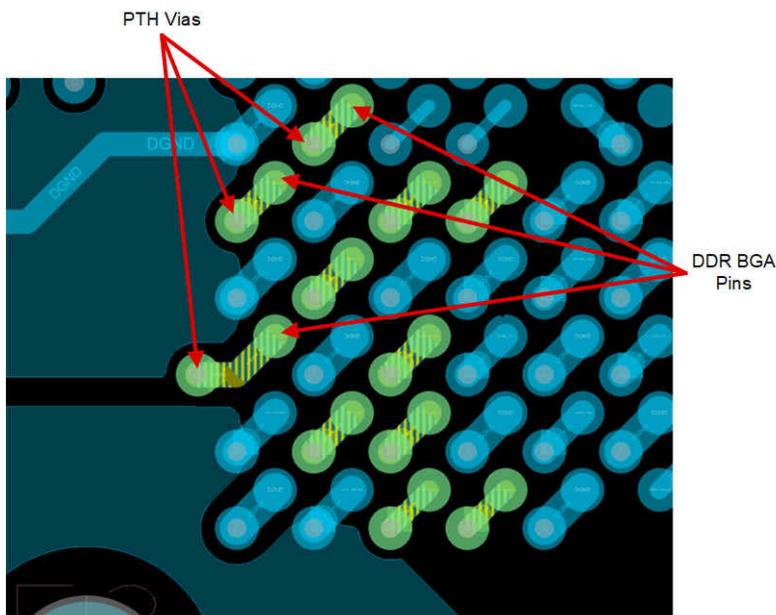


Figure 9-1. DDR Byte Lane0 Escape

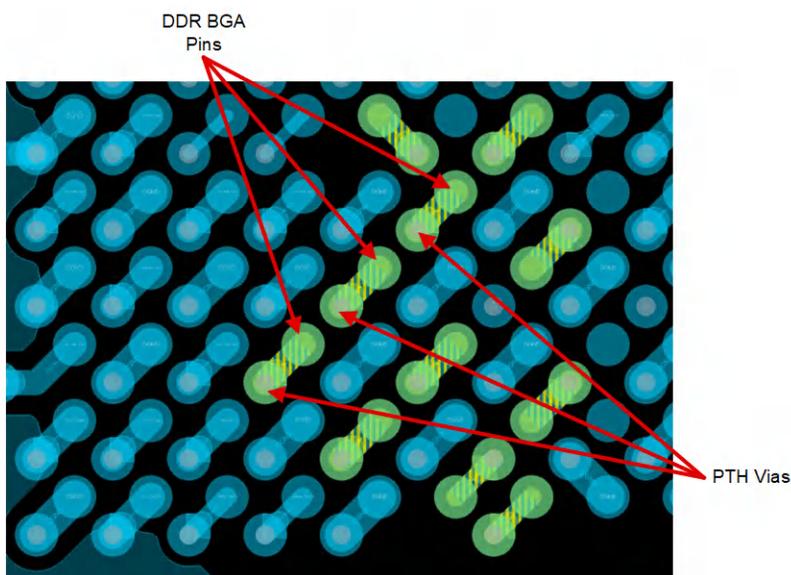


Figure 9-2. DDR Byte Lane1 Escape

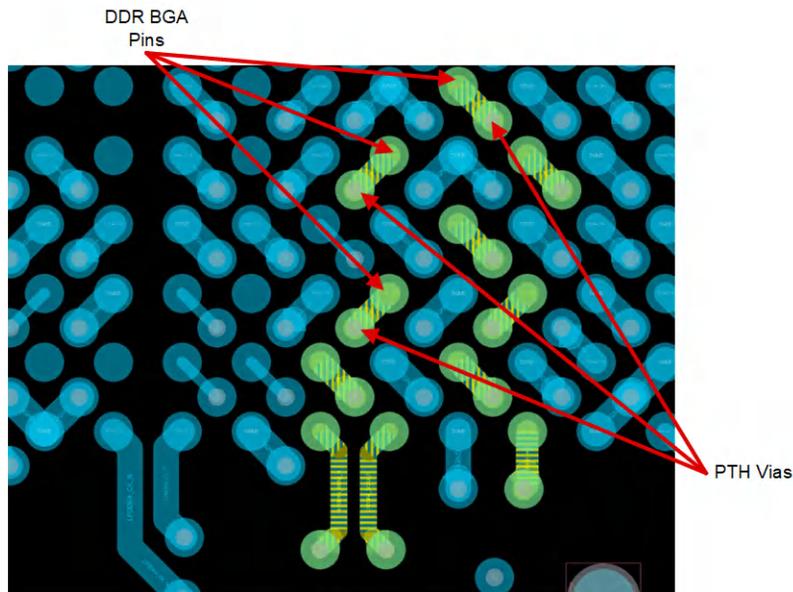


Figure 9-3. DDR Byte Lane 2 Escape

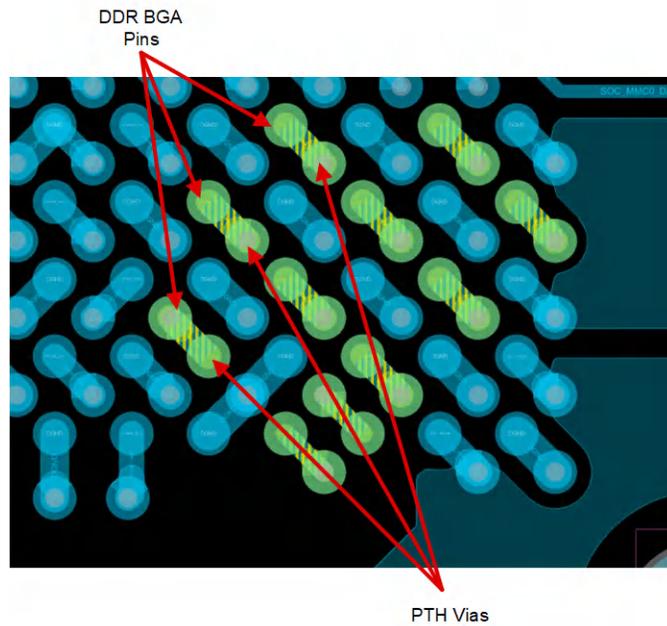


Figure 9-4. DDR Byte Lane 3 Escape

The address, command, and clock signals are routed directly to the memory device.

The top and inner layers are used to escape and route the address and command signals. The traces must be length matched to ensure that the signals arrive at the memory at the same time. Length matching must be from the SoC to memory pin individually, and must include the stub to the memory pad and all via lengths. Refer to the [DDR Routing Guidelines](#) document for detailed recommendations for DDR routing.

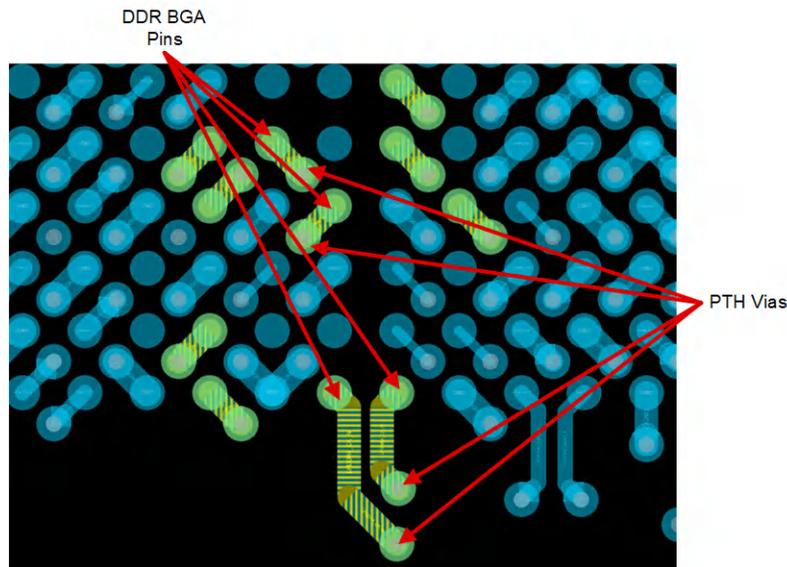


Figure 9-5. DDR Address/Cmd Escape

The escapes of the address and command signals for an LPDDR4 interface on these layers are shown above in [Figure 9-5](#).

Address signals are routed directly from the SoC to the via next to the associated pad for the memory device. This requires that the address signals escape in the correct order. It is required to have the same number of vias for each of the address and command signals. The use of Plated Through Hole (PTH) vias allows the flexibility of routing the address/cmd signals on any layer.

10 Power Decoupling

The middle priority interfaces and the power distribution planes and pours are routed next after the SerDes and DDR interfaces. TI recommends completing all SerDes and DDR routing before continuing with other interfaces. The power distribution planes and pours and all of the decoupling must be placed before PCB simulations are executed for the SerDes and DDR routes, as these can influence the return currents for the high-speed interfaces. The highest speed source-synchronous interfaces, such as RGMII and QSPI, may also require simulation, so these may also need to be completed at this time.

Special care is needed for the 1-uF output capacitors connected to the CAP_VDDS* BGA pins on the AM62Ax device. These capacitors should be placed as close to the pin as possible, and a low inductance path should be present between the CAP_VDDS BGA pin and the supply pad on the capacitor. The layout used on the CAP_VDDS0, CAP_VDDS1, CAP_VDDS5, and CAP_VDDS6 nets on the AM62Ax board is shown below in [Figure 10-1](#). Note the sharing of the GND pad of the capacitors with other capacitors in the vicinity, which allows saving routing resources. Also, it is important to keep the PTH vias for the capacitor power and GND pad connections as close to each other as possible to minimize the loop inductance.

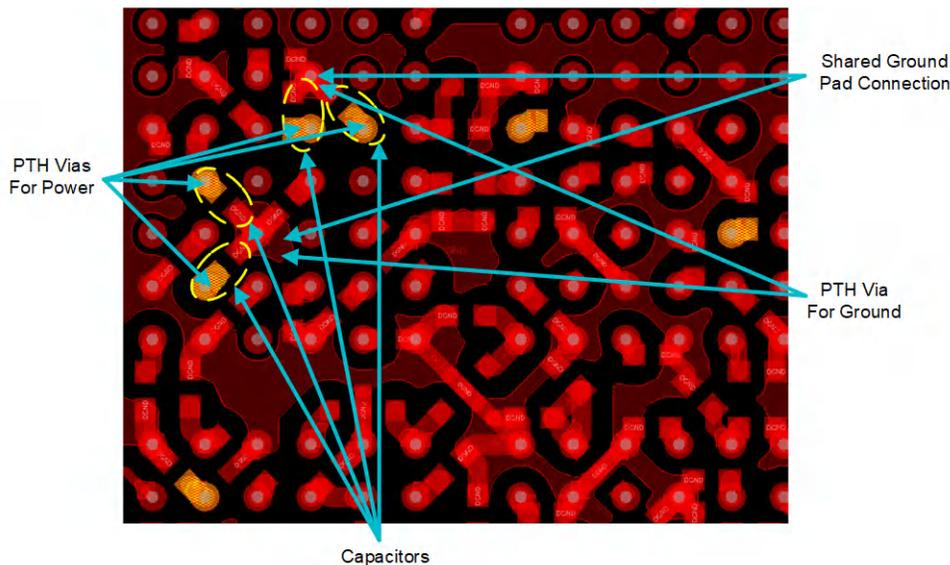


Figure 10-1. Output Capacitor Placement for CAP_VDDS Nets

This placement can be improved if the capacitors can be placed directly under the SoC. The decoupling capacitors for the VDD_CORE and VDDS_DDR supplies should also receive the same priority as those on the CAP_VDDS* pins and should be placed under the socket, with minimum inductance connections to the respective BGA pins on the AM62Ax device.

11 Route Lowest Priority Interfaces Last

When the length matching and simulations for high speed interfaces and DDR have been completed for the highest priority interfaces and the Power Distribution Network (PDN) analysis has been completed, then the layout can continue with the medium and then the lower priority interfaces.

12 Summary

A picture with the AM62Ax with all signals and power escaped is shown in [Figure 12-1](#).

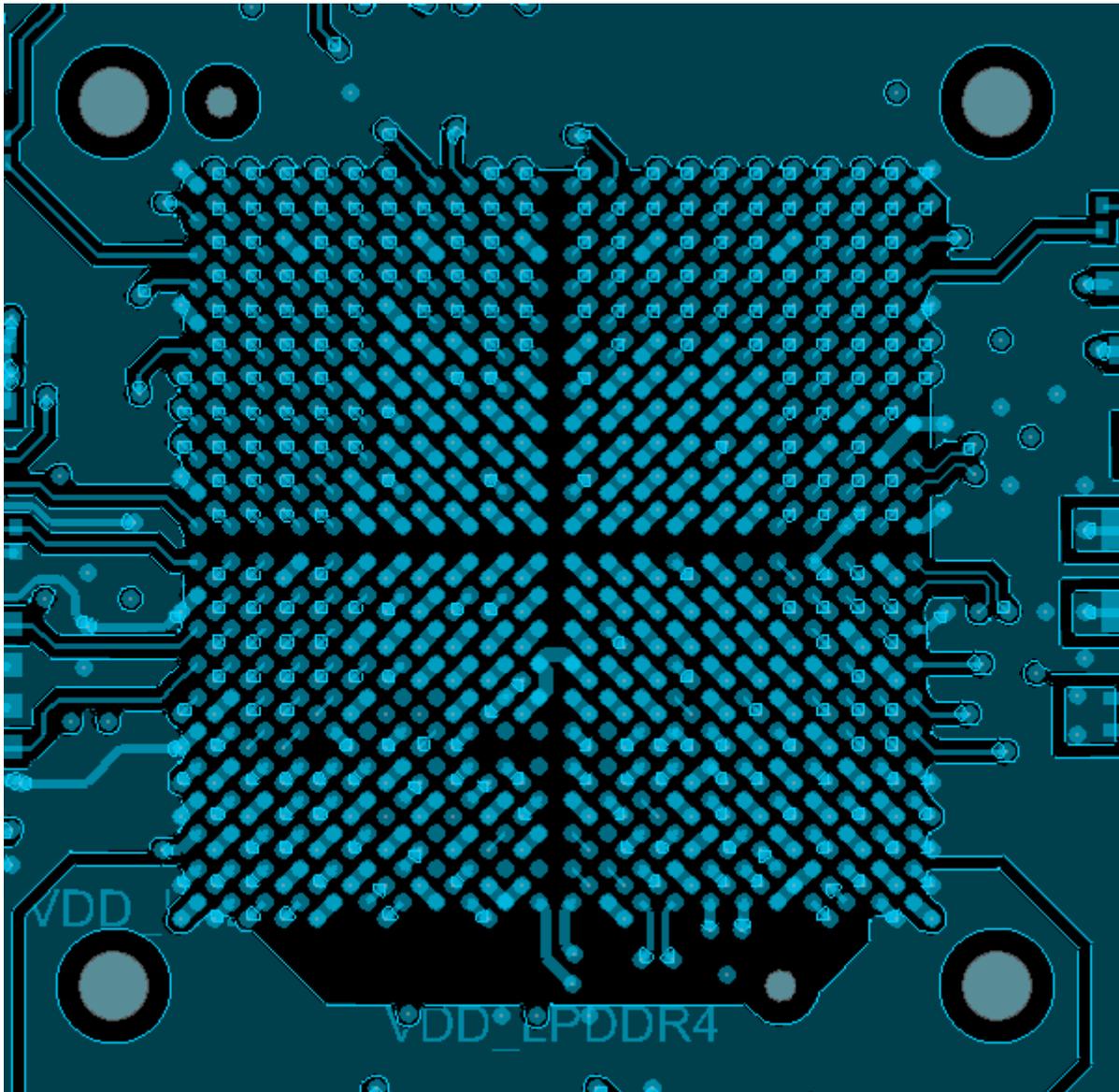


Figure 12-1. AM62Ax with Complete Signal and Power Escapes

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated