Technical Article **Designing a Digital-controlled Power Supply**



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The power-supply industry is currently transitioning from analog to digital control, especially in high-performance power-supply design. In fact, digital controllers now control most AC/DC power supplies used in servers.

Compared to their analog counterparts, digital controllers provide greater flexibility and performance. But those switching from analog control to a digital solution face new challenges where continuous signals are represented by a discrete format: 1 or 0. In this blog series, I'll provide a practical guide to designing a digital-controlled power supply.

Digital Control Fundamentals

As shown in Figure 1, analog control uses discrete components such as resistors, capacitors and operational amplifiers to generate a control effort, u(t). This output commands a plant's output, y(t), to match a reference, r(t), through a sensor, H(s).



Figure 1. Analog Controlled Feedback System

Figure 2 illustrates a typical digital-power control system, with the feedback signal, f(t), sampled and converted to a digital signal through an analog-to-digital converter (ADC). It is then compared with a reference to get a digital error signal. A digital compensator uses this error signal to generate a corresponding pulse-width modulation (PWM) signal to control the power stage. Compared to Figure 1, the control principle is the same but the implementation is different: one is continuous while the other is discrete.



Figure 2. Digital Controlled Feedback System

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A Design Example

Let's design a simple boost converter using Texas Instruments' UCD3138 controller.

The UCD3138 is a fully programmable digital power supply controller offering superior levels of integration and performance in a single chip solution. The flexible nature makes it suitable for a wide variety of power conversion applications, include power factor correction (PFC), LLC resonant converter, phase shifted full bridge, etc. In addition, multiple peripherals inside the device are specifically optimized to enhance the performance of AC/DC and isolated DC/DC applications and reduce component count.

Figure 3 is a block diagram of a UCD3138-controlled boost converter. The signal interface is straightforward: the converter output voltage is attenuated and connected to the control loop feedback input pin. It is then compared with an internal programmable reference to get an error. The error is then sent to an error ADC (EADC) and digitized. This digital error signal then goes through a proportional-integral-derivative (PID) digital compensator, and the output of the PID generates the corresponding PWM duty cycle. All the compensations are internal, no any external compensation circuit needed.



Figure 3. A UCD3138-Controlled Boost Converter Block Diagram

In addition, UCD3138 has built in analog comparators with programmable reference, it can be used to implement fast overvoltage protection (OVP). The analog comparator will be trigged if the sensed Vout signal is higher than a pre-defined threshold, all the PWM signals will shut down to protect the power supply. The input voltage can also be measured by ADC for input brownout protection.

Close the Loop

When talking about loop control, pole/zero are common terms for analog power engineers, but the digital control world usually uses PID. A traditional PID is combined with an extra a in the UCD3138 to provide a two-pole two-zero digital compensator, as shown in Figure 4.





Figure 4. UCD3138 PID Structure

Equation (1) calculates the transfer function for this PID in the z domain:

$$\frac{y}{e} = K_P + K_I \frac{(z+1)}{(z-1)} + K_D \frac{z-1}{z-\alpha}$$
(1)

Both K_P , K_I , K_D and a are programmable and can be adjusted on the fly; this means that the control loop can be dynamically changed based on the operational condition to achieve best performance. Nonlinear PID control is also supported for fast transient response.

Just as in analog power-supply designs, the goal for control-loop designs is to find the right pole/zero such that the system has a desired loop bandwidth and enough stability margins. Here's a typical sequence to design a UCD3138 control loop:

- 1. Derive the small-signal model of the power stage.
- 2. Choose the appropriate K_P, K_I, K_D and a such that the loop has the desired bandwidth and enough stability margins.
- 3. Load K_P , K_I , K_D and a into the UCD3138 and turn on the power converter.
- 4. Fine-tune K_P, K_I, K_D and a until the converter performance meets your desired specifications. For example, the Vout deviation during load transient should within a specific range.
- 5. Use a frequency analyzer to measure the actual loop bandwidth and stability margins. If they do not meet your desired specifications, repeat step 4.

See the additional resources section for more information about how the UCD3138 PID controller works, and the design examples of how to tune the control loop with the help of a frequency analyzer.

In the case that you are familiar with the traditional analog compensator, as shown in Figure 5, and you want to keep the same compensation in your digital design, you can use Equations 2, 3, 4 and 5 to translate the poles/zeros in the time domain into K_P , K_I , K_D and a in the z domain.







$$K_{P} = \frac{C1 \cdot R1(C2 + C3) + C2^{2} \cdot R2}{R1(C2 + C3)^{2}}$$
(2)

$$K_{I} = \frac{Ts}{2 \cdot R1(C2 + C3)}$$
(3)

$$K_{D} = \frac{2 \cdot C2^{2} \cdot R2(C1 \cdot R1(C2 + C3) - C2 \cdot C3 \cdot R2)}{R1 \cdot (C2 + C3)^{2}(C2(2 \cdot C3 \cdot R2 + Ts) + C3 \cdot Ts)}$$
(4)

$$\alpha = \frac{C2(2 \cdot C3 \cdot R2 - Ts) - C3 \cdot Ts}{C2(2 \cdot C3 \cdot R2 + Ts) + C3 \cdot Ts}$$
(5)

Now you have a UCD3138-controlled power converter ready to be tested. In part 2, I'll talk about how to write firmware to make it work.

Additional Resources

- Download the UCD3138 data sheet.
- Read more about the UCD3138 control theory.
- Read the TI application note, UCD3138 PFC Tuning
- Download the Fusion Digital Power Studio GUI for Isolated Power Applications User's Guide.

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