Application Report
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TPS659037 Operation With Higher Capacitive Loading

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ABSTRACT

This application report addresses use-cases where external components demand a higher capacitive loading than the rating of the TPS659037 SMPS-outputs (57-µF maximum per phase). The specification of the device with a rating of nominal 47 µF and maximum of 57 µF holds true. Exceeding these values is at the risk of the user and requires thorough validation in the system. This report is solely intended to provide guidelines on reasonable loading.

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1 Introduction

The TPS659037 device has been designed to drive processors such as OMAP5, Jacinto-6, and similar processors. The supply-domains of these processors have decoupling requirements that can be met with the rating of 47 µF typical (57 µF maximum) per phase, two times this value for dual-phase-operation, and three times this value for triple-phase operation.

The demand for higher decoupling capacitance is mainly driven by external components other than the processor, such as an external memory or physical-layer parts (Ethernet-Phys, Serializers, Deserializers, and other components).

With the number of SMPSs offered by the TPS659037 device and with the limited power-consumption of the processors, the rails of the TPS659037 device can be freed to supply external components in many use-cases. In such cases, it is possible that the decoupling requirements of those external components exceed the rating of the TPS659037 device.

This report addresses the circumstances that may allow for a higher capacitive loading.

CAUTION

This application report only provides guidelines. Operating the device outside of the recommended operating conditions is at the customer's own risk.

2 Device Versions

This document applies to any variant of the TPS659037 device such as orderable TPS659037xZWSR, where *x* designates the OTP-revision (one-time programmable memory).

3 Platform Connection Example

shows an example for the detailed connections between a processor and the TPS659037 device. SMPS7 and SMPS9 are entirely available to drive loads other than the processor, while SMPS3 drives the memory-supply of the processor plus the external memory. SMPS8 shares the power for the processor and external I/Os as well.

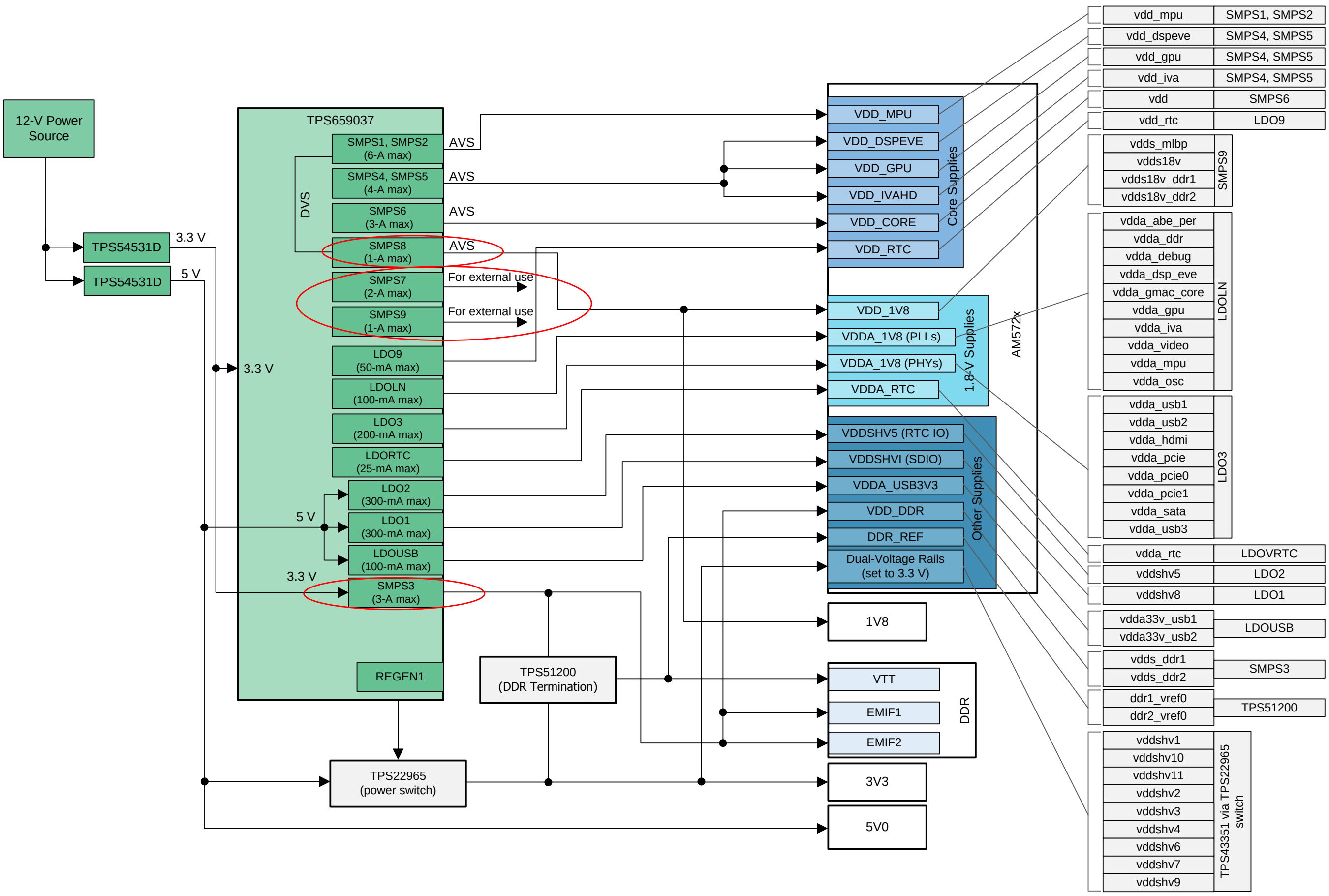

Figure 1. Processor Connection With TPS659037

4 Specification

The device is rated for an output capacitance of 47 µF typical (57 µF maximum). The following lists several reasons for the limited range:

- Internal compensation and therefore no option to adapt to external components
- Wide range of input voltage, output voltages, switching frequencies, loading, and other parameters
- The capacitance must cover temperature-range, process-variation, aging, and others (to a smaller extent)

A wider range of output capacitance can potentially be supported if some of the previously listed reasons are narrowed down. Because additional parameters, such as the ESR of capacitors and parasitics of the layout, have an effect and load-step response and inrush-current is affected, thorough investigation and validation of the user's design is essential.

5 Approach

A higher output-capacitance is most critical at low output voltages. The device supports output voltages down to 0.7 V, while the majority of applications demand an output voltage of at least 1 V. The external components with high decoupling-capacitance needs require an even higher output voltage (1.8 V, 1.5 V or 1.35 V for DDR-Memory and typically 1.8 V or 3.3 V for I/Os and physical layers).

While various input voltages, temperatures, and load conditions are being used, process variation has little effect on the acceptable range of output capacitance. For the purpose of this application report, the focus is on output voltages of 1 V or higher, across the entire supply-voltage range, temperature range, and load conditions.

Because of the similarities between the various SMPSs, SMPS7 was used as a representative for single-phase rails. SMPS12 was used as representation of the second dual-phase supply, SMPS45. Because the triple-phase operation of SMPS123 already allows for three times the single-phase loading (3 × 47 µH = 141 µH) and, is in all known cases used for a processor domain with limited decoupling needs, SMPS123 was not further evaluated.

Initially, simulations on actual silicon schematics were performed to get an overview of the acceptable capacitance, phase-margins, distribution over process, temperature, inductor-tolerance, and loading with various input and output voltages.

The results confirmed that with an output voltage of 0.7 V, only slight increases in output capacitance are possible. Therefore, no further evaluation with higher loading was tested for this output voltage. The results also determined that at output voltages of 1 V and higher, the potential increase in capacitance was limited. Similarly, the supply voltage had a stronger effect for single-phase. Therefore, a 3.3-V supply versus a 4.2-V supply and 5-V supply was distinguished. Because no significant impact was observed for multiphase, the evaluation was focused on the same capacitive loading (194 µF) for all supply-voltages (3.3 V , 4.2 V, and 5 V) for dual-phase operation.

The evaluation was conducted using gain-phase analysis with combinations of the following parameters:

- Supply voltage (VSYS)
- Output voltage
- Output voltage
- Load capacitance for single-phase (SMPS7) and dual-phase (SMPS12)

With a correlation between simulation and measurements, load-step-analysis was performed with all combinations of the following parameters:

- Supply voltage (VSYS)
- Output voltage
- Load-step: 800 mA to 2 A to 800 mA
- Load capacitance for single-phase (SMPS7) and dual-phase (SMPS12)
- Various temperatures: cold, room-temperature, and hot

6 Test Results

Based on the performed tests, single-phase rails could support up to 90-µF total capacitive loading (COUT of the SMPS plus all decoupling at the point of load) at a 3.3-V supply and a minimum output voltage of 1 V. At a 4-V supply or higher and minimum output voltage of 1 V, up to 130-µF capacitance can be supported. In any case, such a high capacitance would present an operation outside of the specification and thorough testing within the environment of the user is essential.

Notes:

- Load-step-responses showed stable behavior with 130 µF even at a 3.3-V supply, however the phase-margin is reduced. Therefore, TI recommends not to exceed 90 µF with such low supply voltages.
- The additional capacitance was soldered directly onto the output capacitor. This placement results in drops or overshoots on VOUT that potentially exceed the transient response-specification. In an actual design with distributed loads and capacitance, the behavior at the actual load is expected to be better, but demands thorough evaluation by the user in the specific design. Similarly, the additional ESR introduced by traces to the load capacitance change the gain-phase-plot. Therefore using the previously listed values as guidelines only is essential but the system behavior must be adequately validated in the actual design by the user.

Figure 2 shows the frequency band down to 1 Hz, proving no additional poles or zeroes at low frequencies. The following plots focus on the relevant region above 100 Hz.

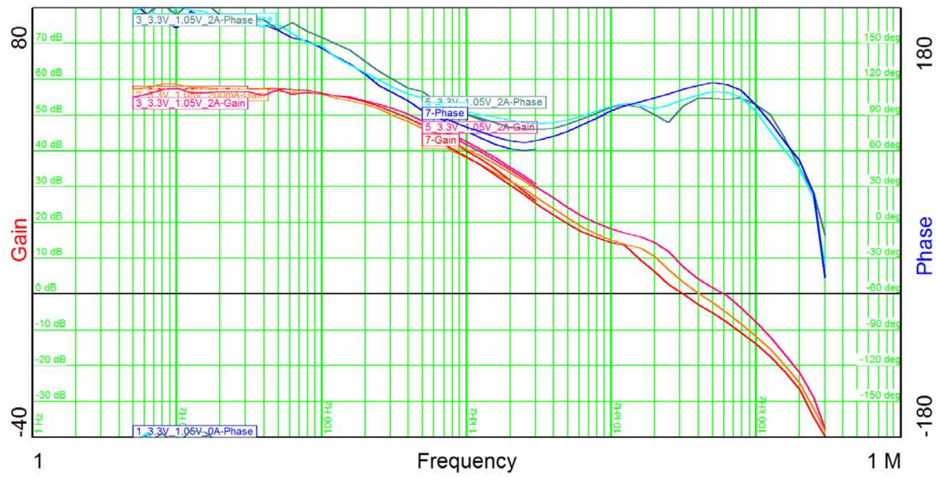

Figure 2. Single-Phase Gain-Phase-Plot With 3.3-V Input, 1.05-V Output, 94 µF

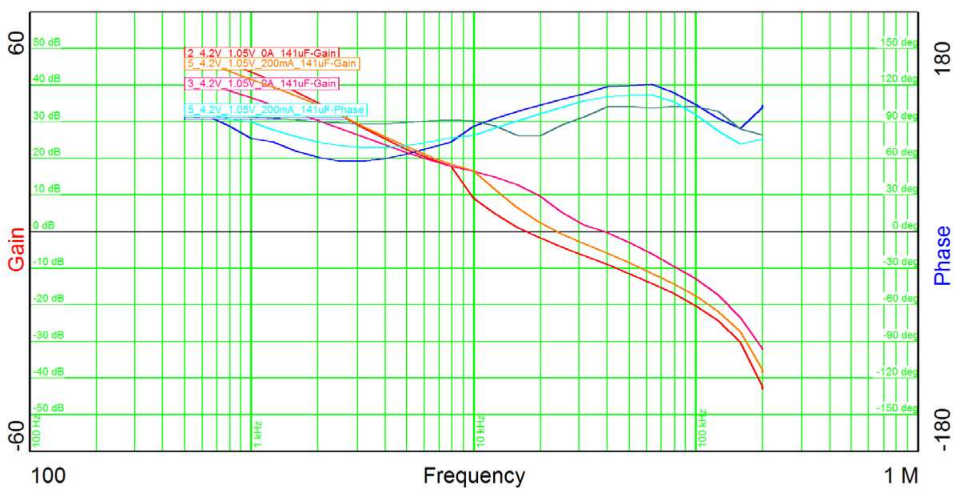

Figure 3. Single-Phase Gain-Phase-Plot With 4.2-V Input, 1.05-V Output, 141 µF

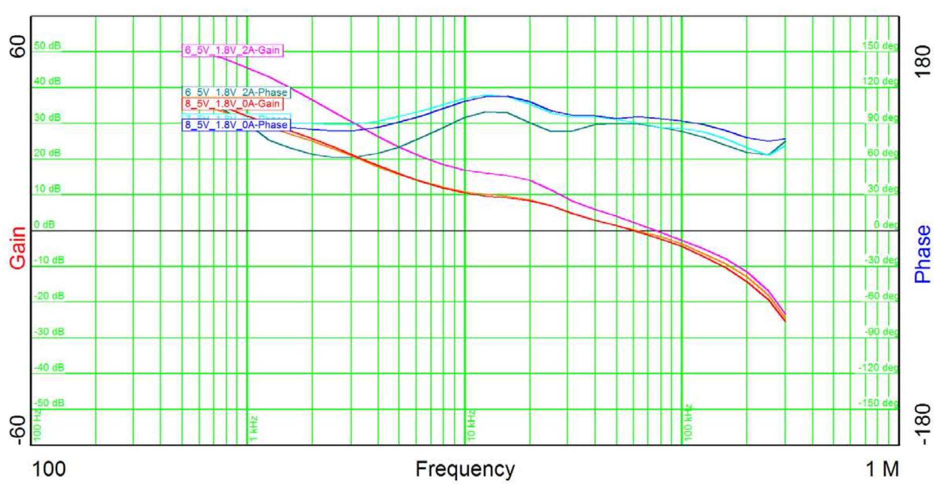

Figure 4. Single-Phase Gain-Phase-Plot With 5-V Input, 1.8-V Output, 94 µF

For dual-phase operation, load-step responses show stability to double the nominal output capacitance and a total capacitive output load of up to 180 µF can be supported for output voltages of 1 V or above.

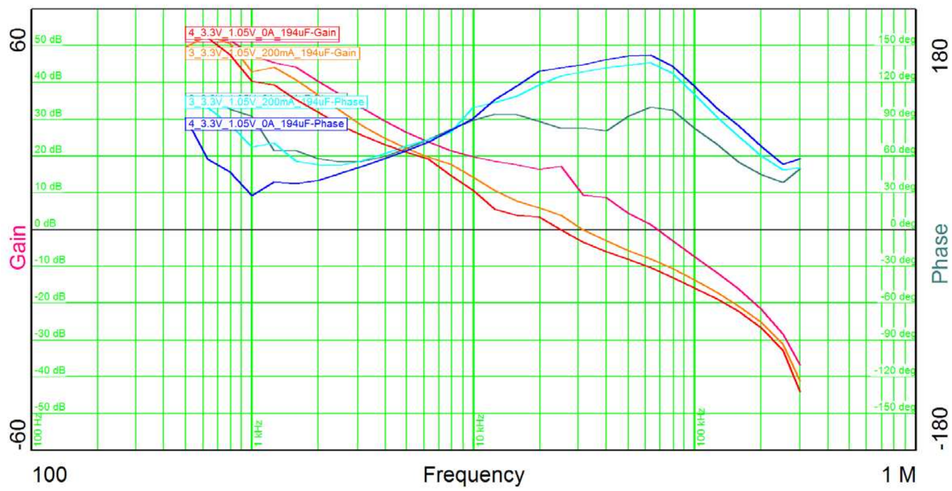

Figure 5. Dual-Phase Gain-Phase-Plot With 3.3-V Input, 1.05-V Output, 194 µF

6.1 Load-Step Response

The various scenarios were proven by the load-step-response tests, which were performed over temperature. The following figures show the previously used example-conditions and were taken at high temperature (hot), which represents the worst case condition. The figures show overshoots and undershoots in the < 30-mV range for load steps of 800 mA to 2 A to 800-mA with very fast transients (approximately 7 A/µs). The magenta curve shows the output current (50 mV/Div over a 100-mΩ shunt resulting in 500 mA/Div). The yellow curve shows the output voltage which is DC-coupled (20 mV/Div). The timescale is 100 ns/Div.

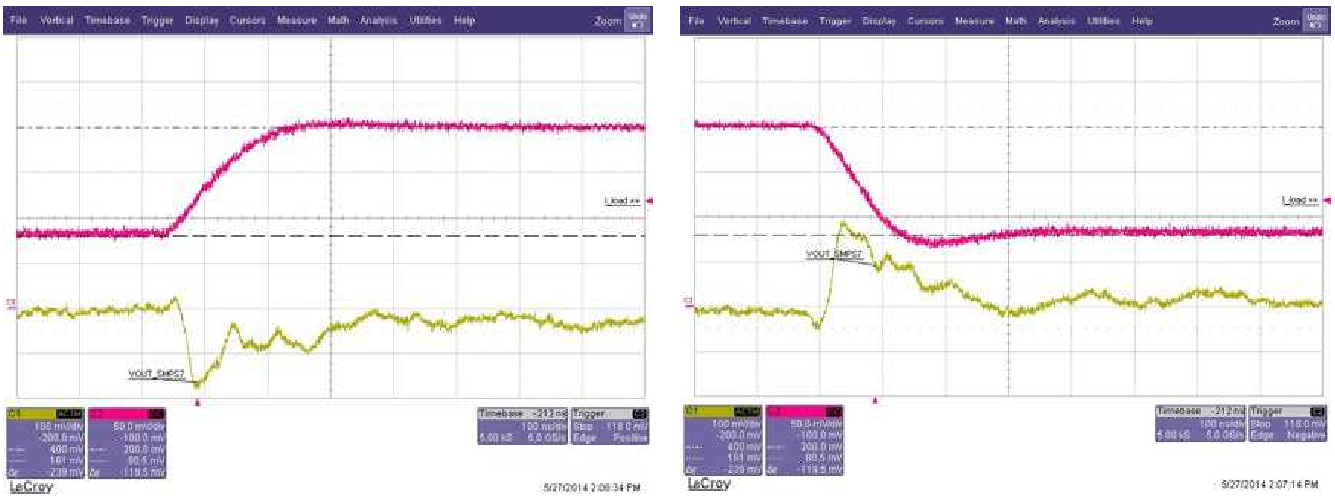

Figure 6. Single-Phase Load-Step Response 3.3-V Input, 1.05-V Output, 94 µF, Hot

Figure 7. Single-Phase Load-Step Response 3.3-V Input, 1.8-V Output, 94 µF, Hot

Figure 8. Single-Phase Load-Step Response 5-V Input, 1.05-V Output, 94 µF, Hot

Figure 9. Single-Phase Load-Step Response 5-V Input, 1.8-V Output, 94 µF, Hot

Figure 10. Single-Phase Load-Step Response 5-V Input, 3.3-V Output, 94 µF, Hot

The multiphase rail shows even less overshoots or undershoots which takes advantage of the multi-phase approach.

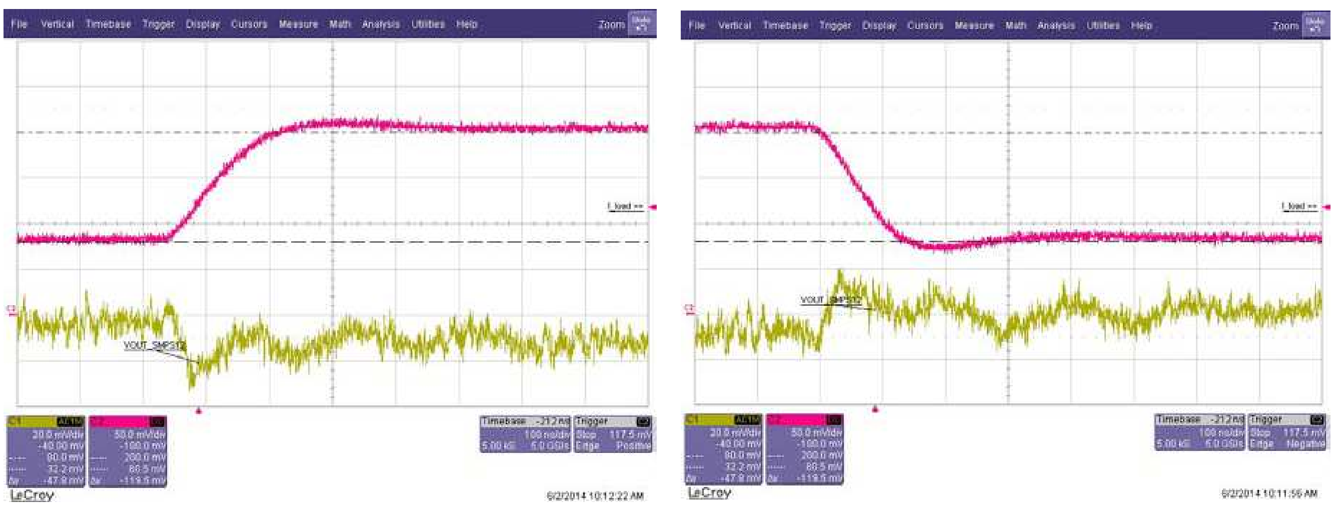

Figure 11. Dual-Phase Load-Step Response 3.3-V Input, 1.05-V Output, 194 µF, Hot

Figure 12. Dual-Phase Load-Step Response 3.3-V Input, 1.8-V Output, 194 µF, Hot

Figure 13. Dual-Phase Load-Step Response 5-V Input, 1.05-V Output, 194 µF, Hot

Figure 14. Dual-Phase Load-Step Response 5-V Input, 1.8-V Output, 194 µF, Hot

Figure 15. Dual-Phase Load-Step Response 5-V Input, 3.3-V Output, 194 µF, Hot

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