Input and Output Characteristics of Digital Integrated Circuits at 5-V Supply Voltage

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Contents

List of Illustrations

List of Illustrations (Continued)

List of Illustrations (Continued)

Abstract

This application report presents a comprehensive collection of the input and output characteristic curves of integrated circuits from various 5-V logic families. These curves go beyond the information given in data sheets by providing additional details regarding the characteristics of the components. This knowledge is particularly useful when, for example, a decision must be made as to which circuit should be used in a bus system, or when the waveforms that can be expected in a transmission system need to be predicted by using a Bergeron chart. These oscillograms are of great assistance when generating models for simulation programs, which analyze the dynamic behavior of the integrated circuits in a particular environment.

1 Introduction

The parameters given in the data sheets of integrated circuits can give only a very limited indication of their actual behavior in a system. Generally, data sheets give only information regarding the behavior over the input and output voltage range of 0 to 5 V. Even the output currents specified over this range only provide an incomplete picture of the actual performance that can be expected.

But, often the behavior outside the normal operating conditions is of interest. This is, for example, the situation when the characteristic curves are used to predict the signal waveforms resulting from line reflections.

With the input/output (I/O) characteristics, use of the Bergeron method, and knowledge of the load resistor, the amplitude of the line reflections can be determined.

This application report contains the input and output characteristics of integrated logic circuits, operating at V_{CC} = 5 V.

Many modern logic families are specified for operation at different supply voltages. For example, the AHC logic can be used at 5-V, 3.3-V, or even at 2.5-V supply voltage.

Since three supply voltages are currently used, it is necessary to provide I/O characteristics at these different voltage levels. This report deals exclusively with devices operated at V_{CC} = 5 V.

Two other application reports regarding this topic are available:

- *Input and Output Characteristics of Digital Integrated Circuits at 3.3-V Supply Voltage*, literature number SZZA010
- *Input and Output Characteristics of Digital Integrated Circuits at 2.5-V Supply Voltage*, literature number SZZA012

In view of the wide range of integrated circuits available, it is necessary to limit this information to typical characteristics only.

In Sections 2 and 3 of this report, the input and output characteristics of the following circuits are representative of other components that behave similarly in circuits:

’00 The characteristic curves of this NAND gate are representative of all logic circuits having normal drive capability, such as gates, flip-flops, counters, multiplexers, etc.

’40 For a range of applications, gates are available in several logic families having increased drive capability. Such components can supply about three times the output current, when compared with the normal drive capability of the logic circuits mentioned above.

’1004 A special group of driver circuits introduced into the ALS and AS family for applications require a very large output current. These components play a particularly significant role in clock-distribution systems.

’240 The output characteristics of these bus-interface circuits are of particular importance when choosing a circuit family for a specific system requirement. As mentioned elsewhere in this report, the available output current has a decisive influence on the distortion of signals on bus lines.

’25240 The incident wave switching (IWS) driver was developed to meet the requirements imposed by fast bus systems and applications with exceptionally low-resistance lines. Because these components play a very significant role in applications of this kind, their characteristic curves also have been included.

Table 1 gives an overview of the input and output characteristics, which are shown in Figures 1 through 77 in the remaining sections of this application report.

Because input characteristics depend exclusively on the technology used, rather than on the logical function of the device, only one representation per logic family is shown (gate function ’00 or driver function ’240) in the input-characteristics section.

Table 1. Representatives of the Different Logic Families

FAMILY	TYPE				
	’00	’40	’240/’244	’1004	’25240
SN74	√	√			
SN74LS	√	√	√		
SN74S	√	√	√		
SN74ALS	√	√	√	√	
SN74AS	√		√	√	
SN74F	√	√	√		
SN74HC	√		√		
SN74AHC	√		√		
SN74AC	√		√		
SN74BCT			√		√
SN74ABT†			√		√†
SN74ABTE†			√†		
SN74LV	√		√		

† For the ABT/ABTE families, the measurements were taken using the bidirectional devices SN74ABT25245 and SN74ABTE16245.

Section 4 contains the calculation of line reflections using the Bergeron method, based on the SN74AHC240 device. Measurement results, demonstrating different switching behaviors of the various logic families, are given in Section 5. For these measurements, the devices under test were loaded with a 1.3-m-long coaxial cable having a characteristic impedance of 50 Ω. The end of the cable was not connected, i.e., open circuit. These waveforms provide good insight into the dynamic behavior of the components.

2 Input Characteristics

In the positive range, the high impedance of the input stage of the logic circuit determines the input characteristics of logic circuits (see Figures 1 through 12).

For bipolar circuits, a base-emitter current, which flows into the input circuitry, is needed. Therefore, the input resistance for bipolar logic devices is in the range of several kilohms. Negative voltage peaks are limited by a protection diode.

CMOS and BiCMOS circuits have CMOS inputs. The CMOS input stages are exclusively controlled by the applied voltage, so there is no current flowing into the input stage. Therefore, the input impedance of CMOS and BiCMOS devices is much higher and is in the range of megohms. Again, negative voltage peaks are limited by a protection diode.

The input stages of some CMOS logic families (SN74HC, SN74AC) also have an input protection diode, that is connected to V_{CC}. This diode limits the positive input voltage to maximum V_{CC} + 0.7 V.

The bus-hold circuit is a special input circuit that is an option for many ABT devices. Inputs of devices that have the bus-hold circuit hold the last valid logic state. This feature is suitable where an input remains undefined, e.g., during a high-impedance state on the bus. Using the bus-hold circuit eliminates the need for pullup or pulldown resistors.

Devices with the bus-hold circuit are designated by an H in their nomenclature, for example, SN74ABTH245.

A more detailed application report, *Bus-Hold Circuits*, literature number SZDAE15, is available from Texas Instruments (TI™).

Additional application reports and other related literature are listed in Section 7, *References*.

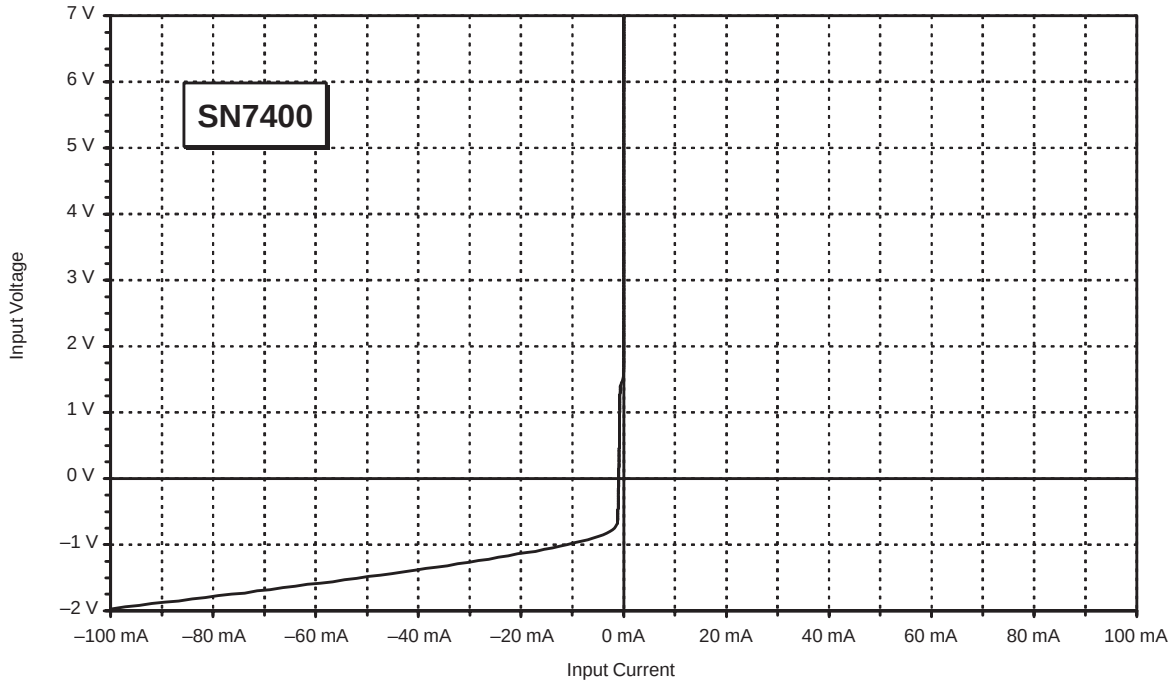

Figure 1. Input Characteristic of the SN74xxx Series

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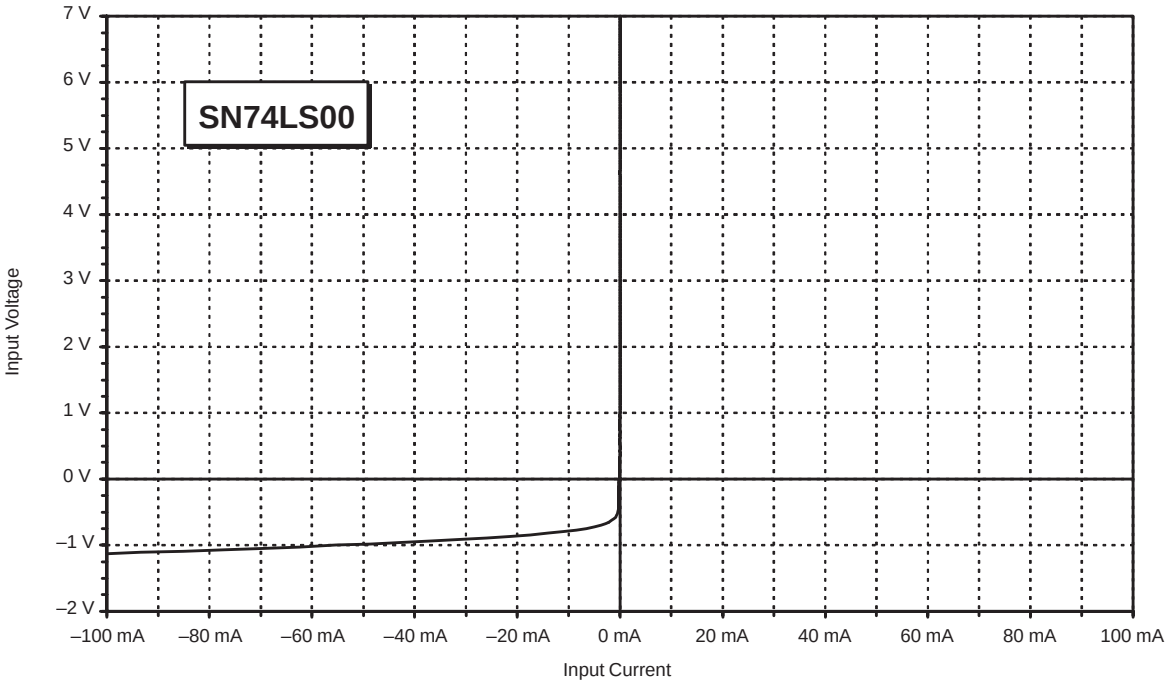


Figure 2. Input Characteristic of the SN74LSxxx Series

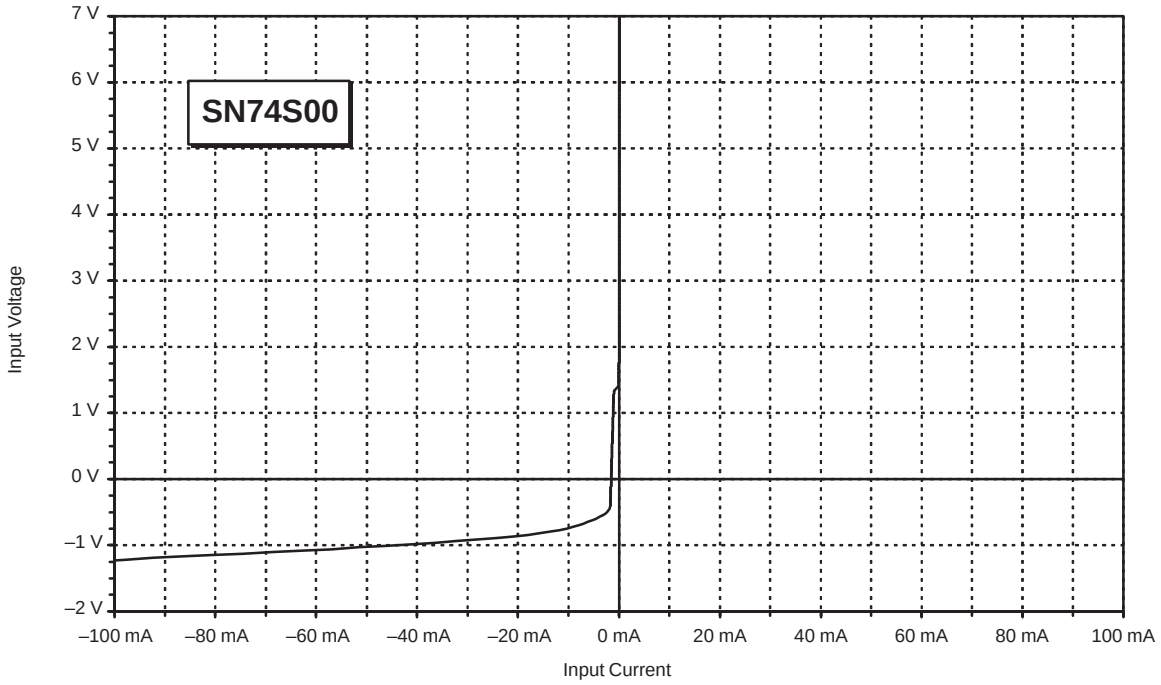


Figure 3. Input Characteristic of the SN74Sxxx Series

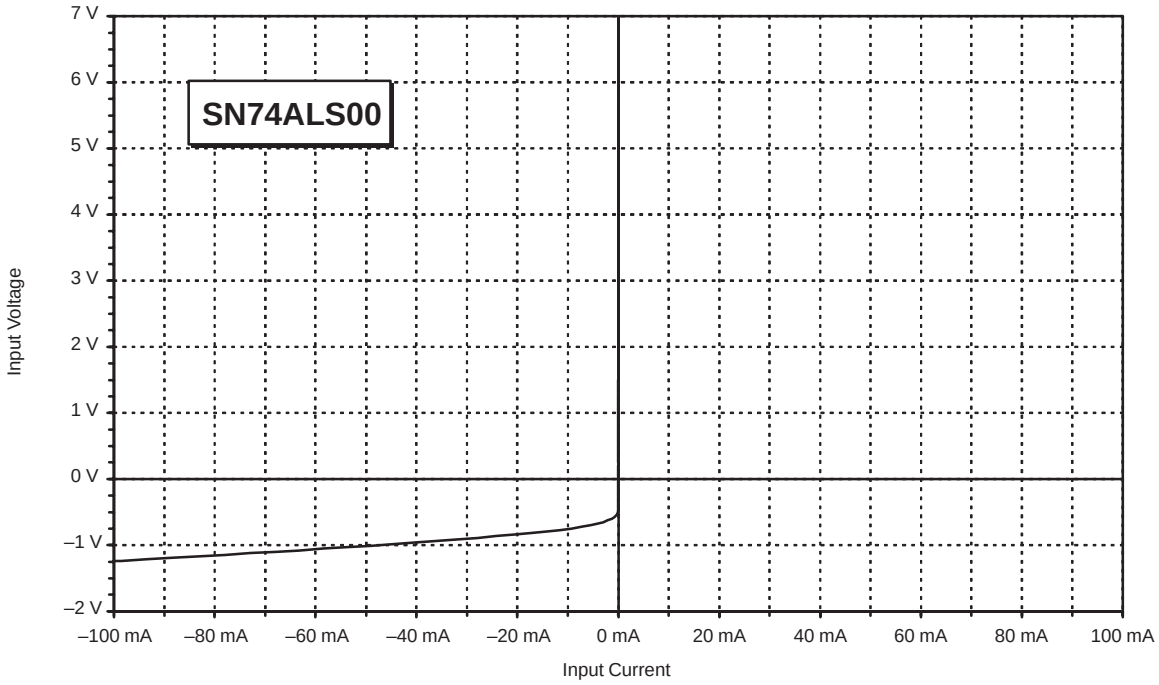


Figure 4. Input Characteristic of the SN74ALSxxx Series

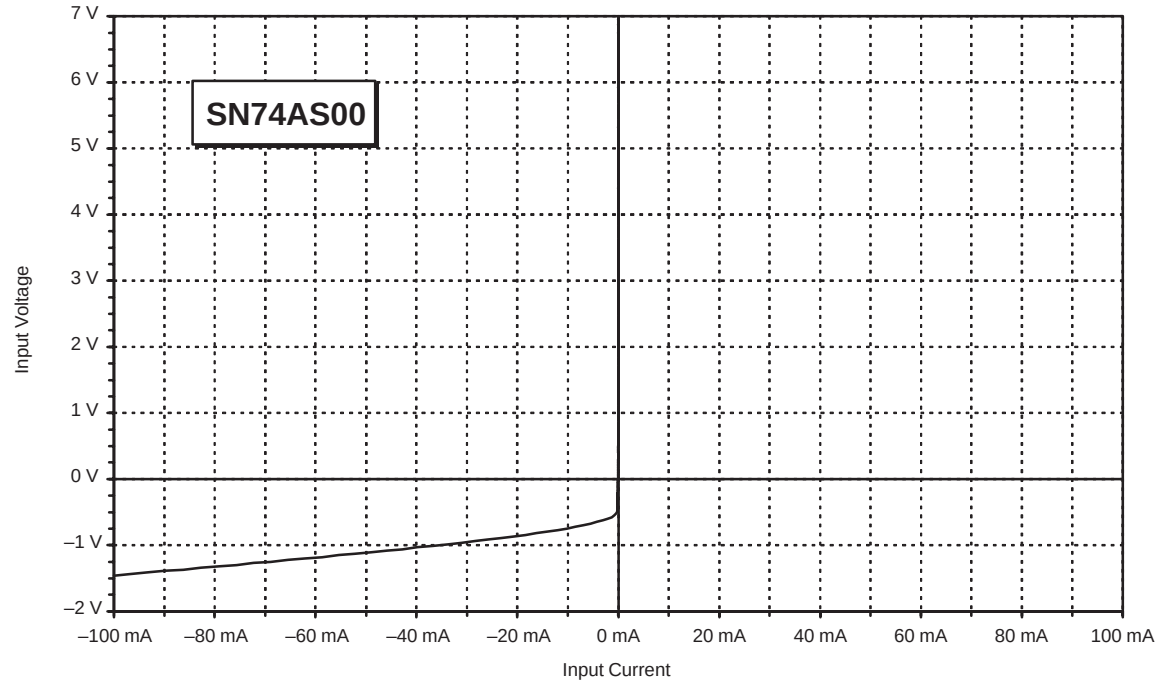


Figure 5. Input Characteristic of the SN74ASxxx Series

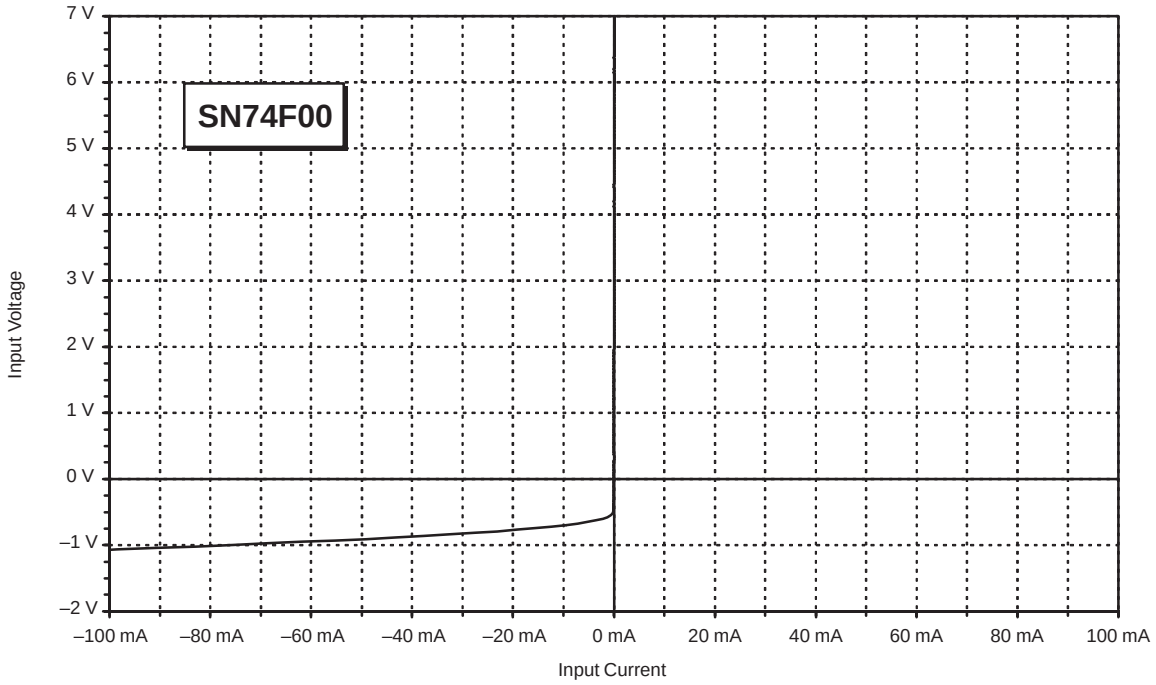


Figure 6. Input Characteristic of the SN74Fxxx Series

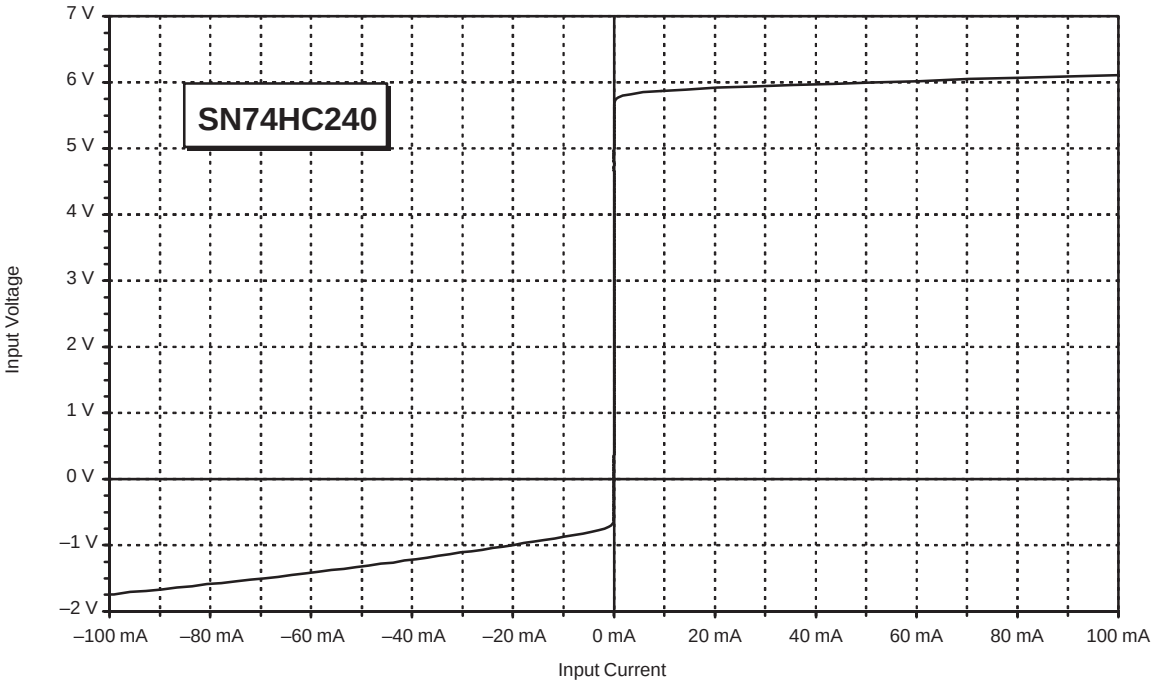


Figure 7. Input Characteristic of the SN74HCxxx Series

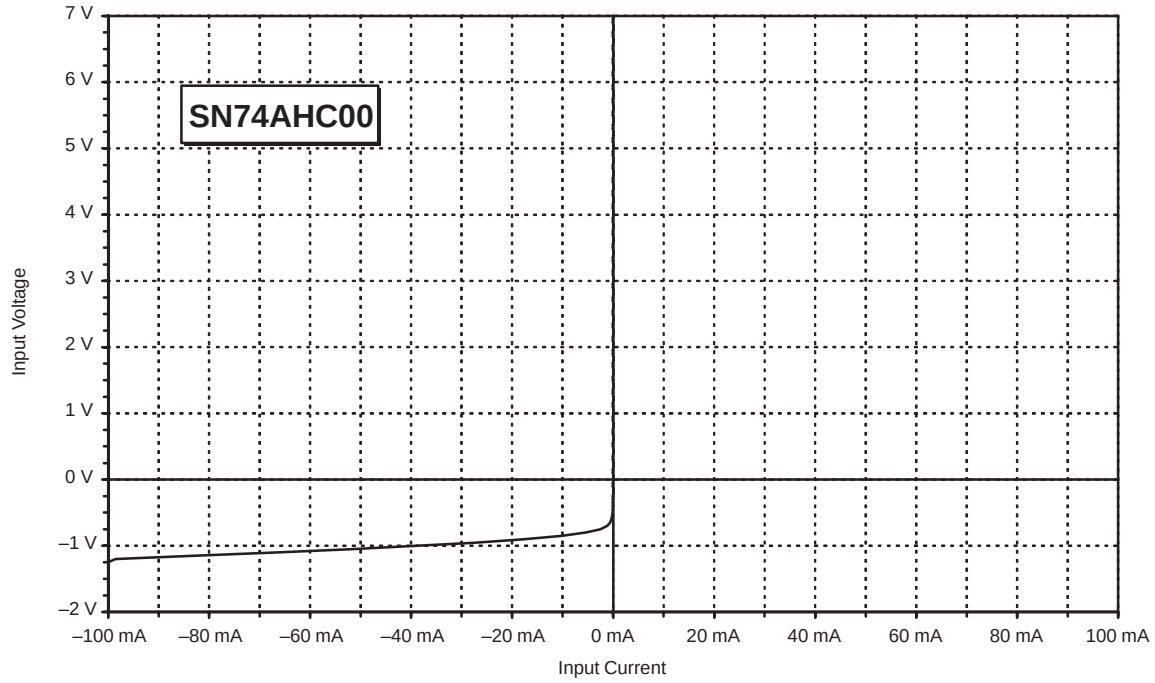


Figure 8. Input Characteristic of the SN74AHCxxx Series

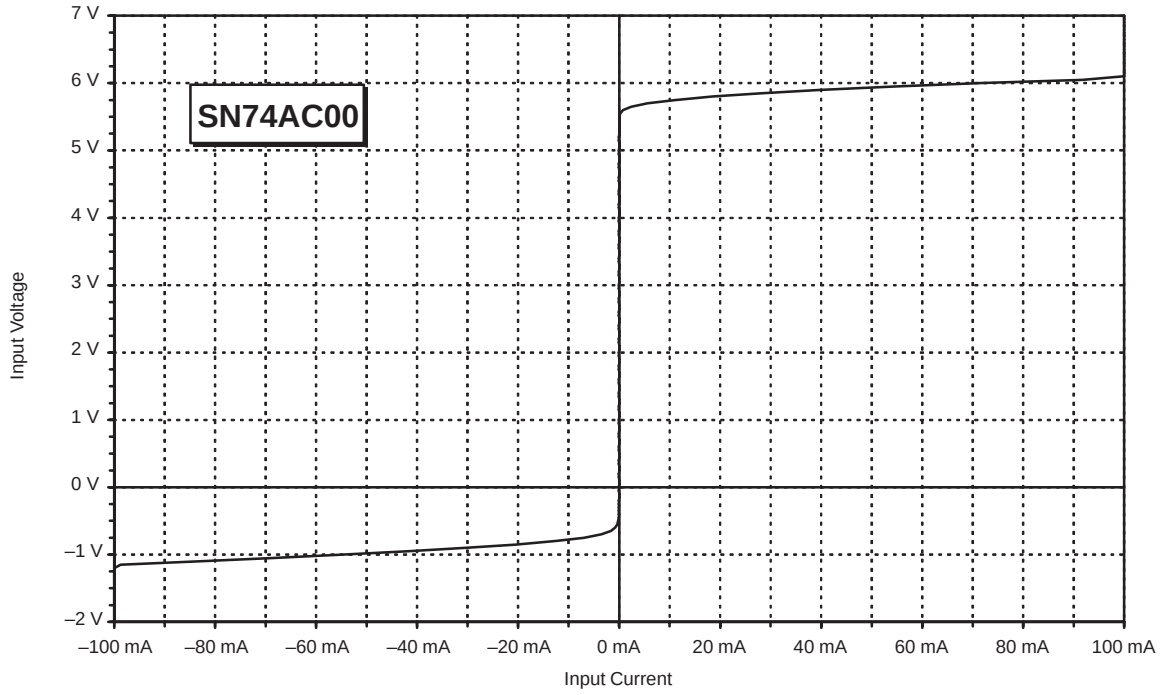


Figure 9. Input Characteristic of the SN74ACxxx Series

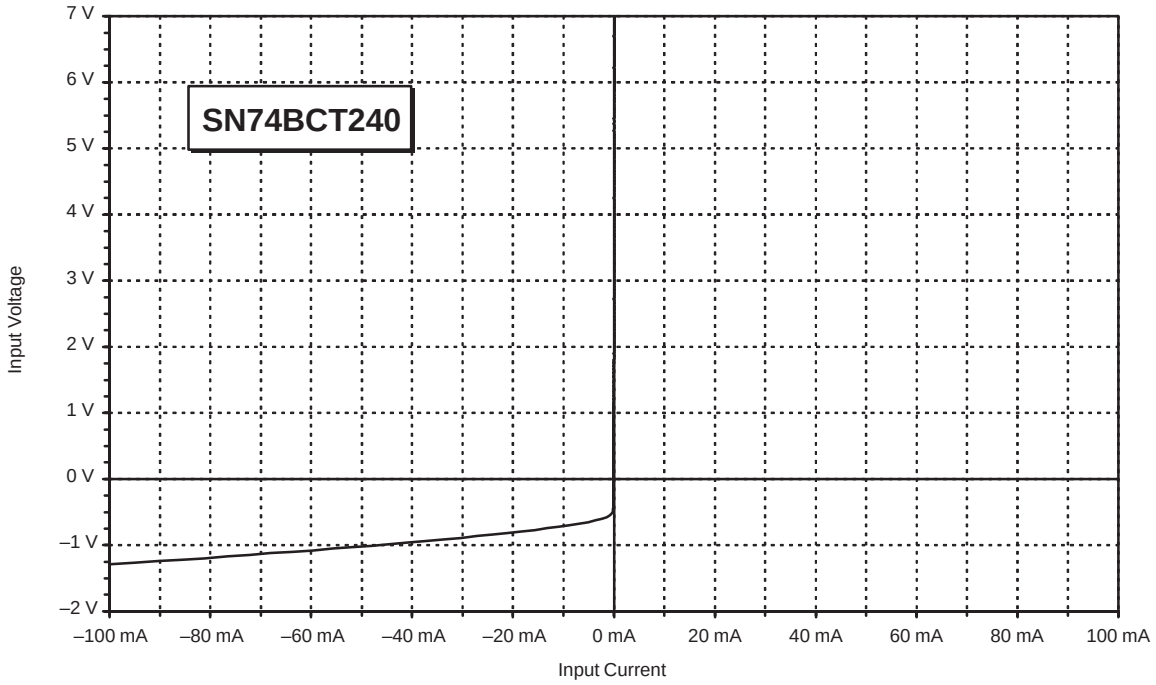


Figure 10. Input Characteristic of the SN74BCTxxx Series

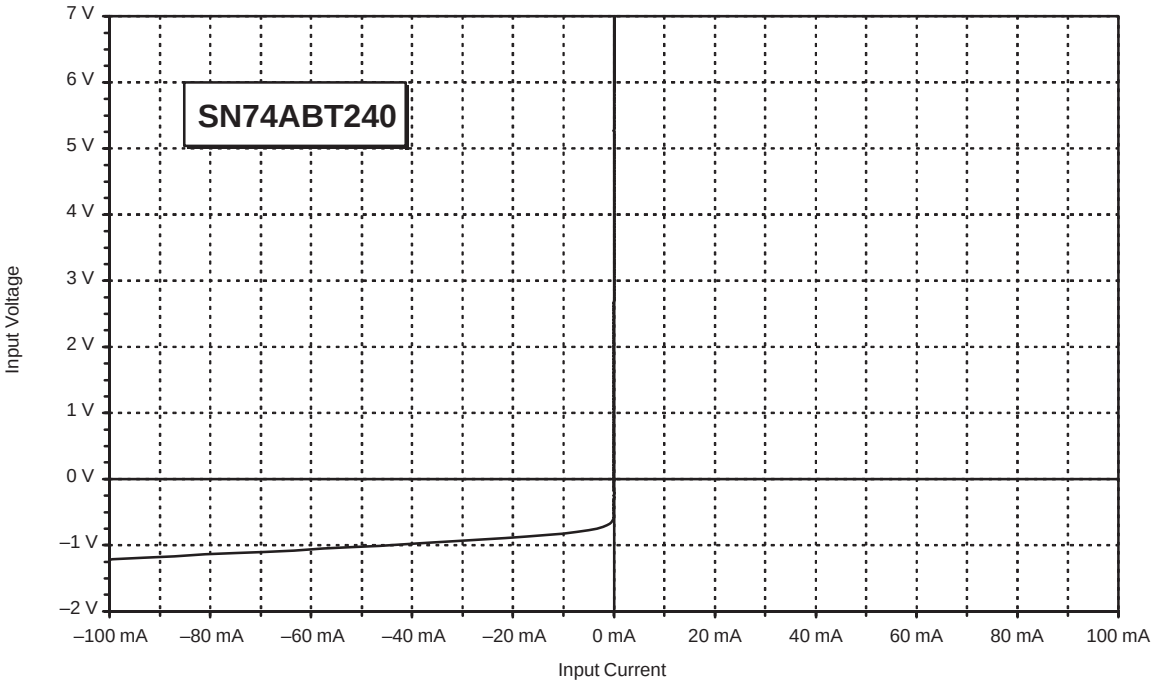


Figure 11. Input Characteristic of the SN74ABTxxx Series

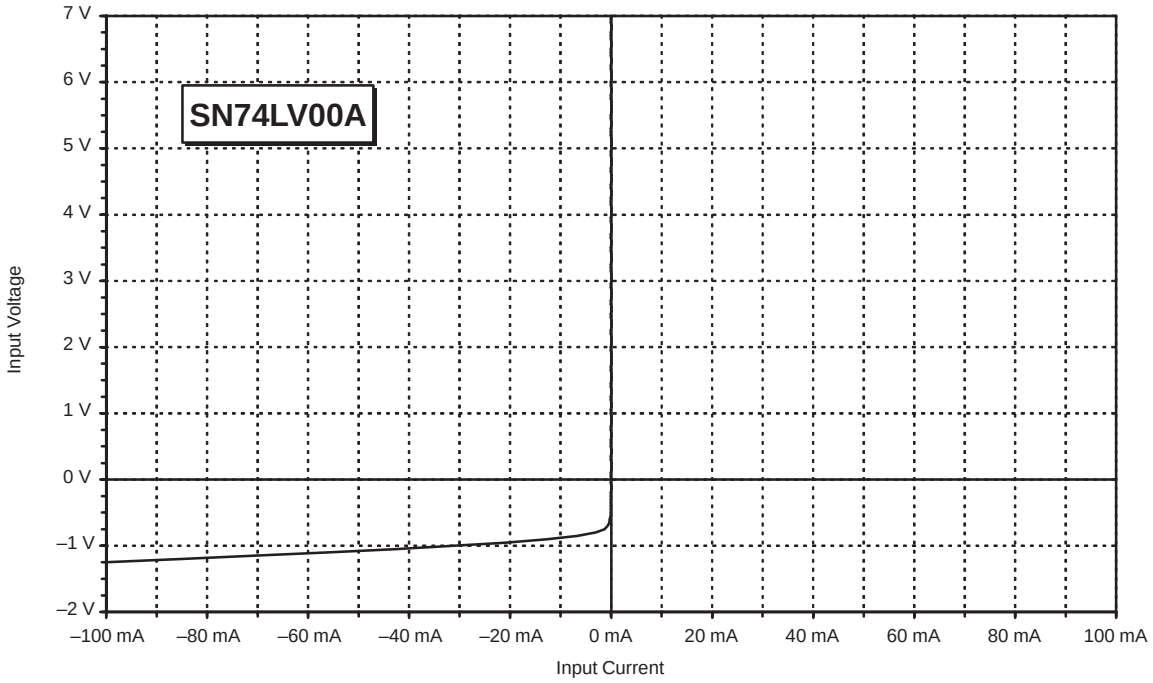


Figure 12. Input Characteristic of the SN74LVxxx Series

3 Output Characteristics

The output stage of a logic circuit in the high state behaves like a voltage source with an open circuit voltage of 5 V for CMOS logic, and 3.6 V for TTL and BiCMOS logic (see Figures 13 through 43). The internal resistance for the high state is inversely proportional to the drive capability of the device. The value of the internal resistance for the standard logic families is in the range of 30 Ω to 40 Ω. The internal resistance of the IWS driver is lower than 5 Ω.

In the low state, for positive voltages, the output resistance is based on the internal resistance of the conducting transistor, i.e., collector-emitter for bipolar and BiCMOS technologies and drain-source resistance for CMOS technologies. Again, negative voltage peaks are limited by a protection diode.

The output stages of some CMOS logic families (SN74HC, SN74AC) also have an input protection diode, which is connected to V_{CC}. This diode limits the positive input voltage to maximum V_{CC} + 0.7 V.

TI offers driver options in the ABT family with integrated series resistors rated at about 25 Ω.

Using the damping resistors at the output stage, the effective output impedance of the driver is about 30 Ω. If the value of the line impedance also is about 30 Ω, no line reflections will be observed at the output of the device. In this case, the beginning of the line is terminated perfectly.

This option is especially beneficial for memory applications. In those applications, overshoots and undershoots may cause malfunctions. In point-to-point applications, nearly ideal signal shapes can be achieved. The 2 following the alphabetical part of the device number indicates the series damping resistor, for example, SN74ABT2245.

Further information on the topic of series damping resistors is given in the TI application report, *Bus-Interface Devices With Output-Damping Resistors or Reduced-Drive Outputs*, literature number SCBA012A.

More application reports and other related literature are listed in Section 7, *References*.

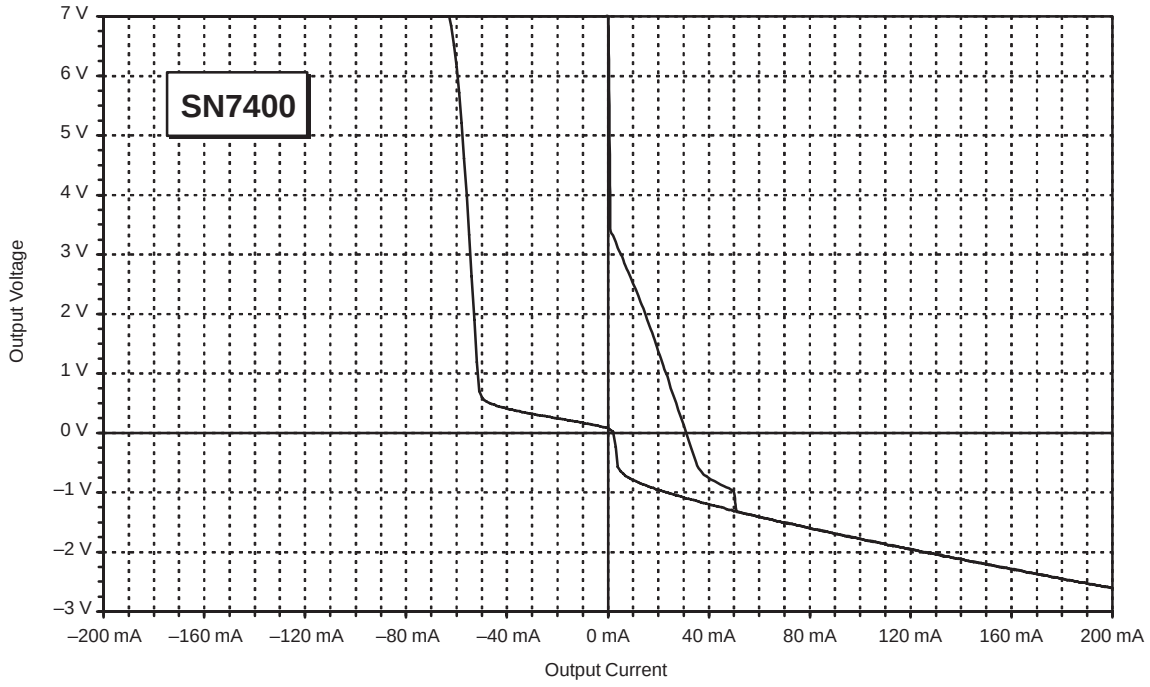


Figure 13. Output Characteristic of the SN7400

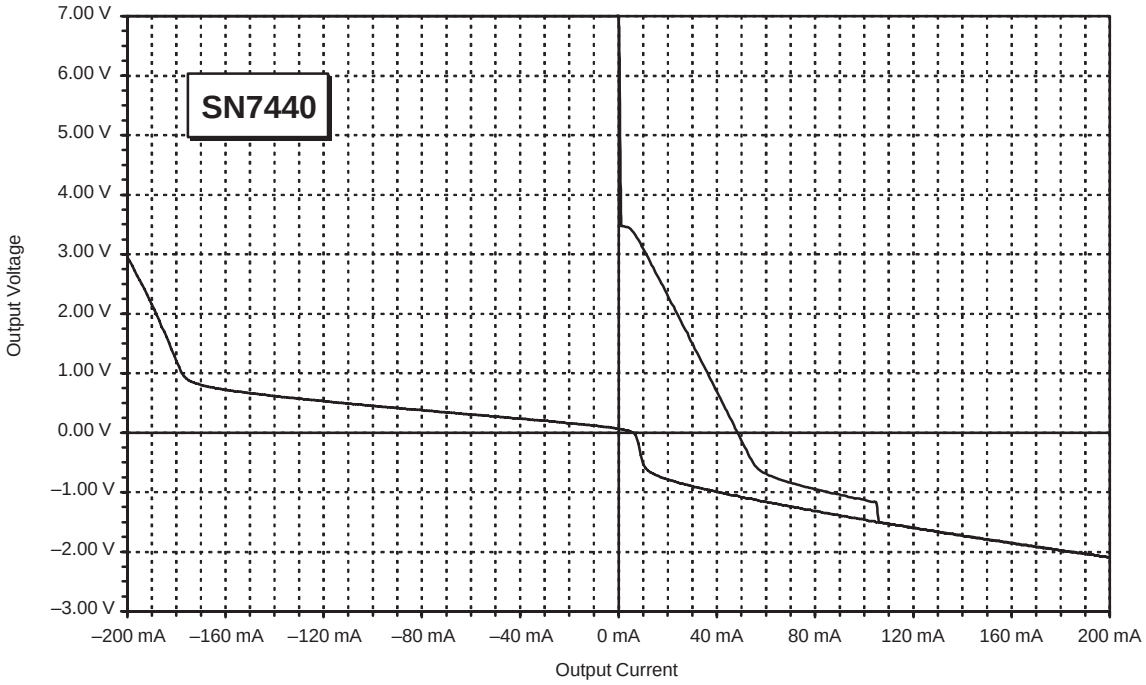


Figure 14. Output Characteristic of the SN7440

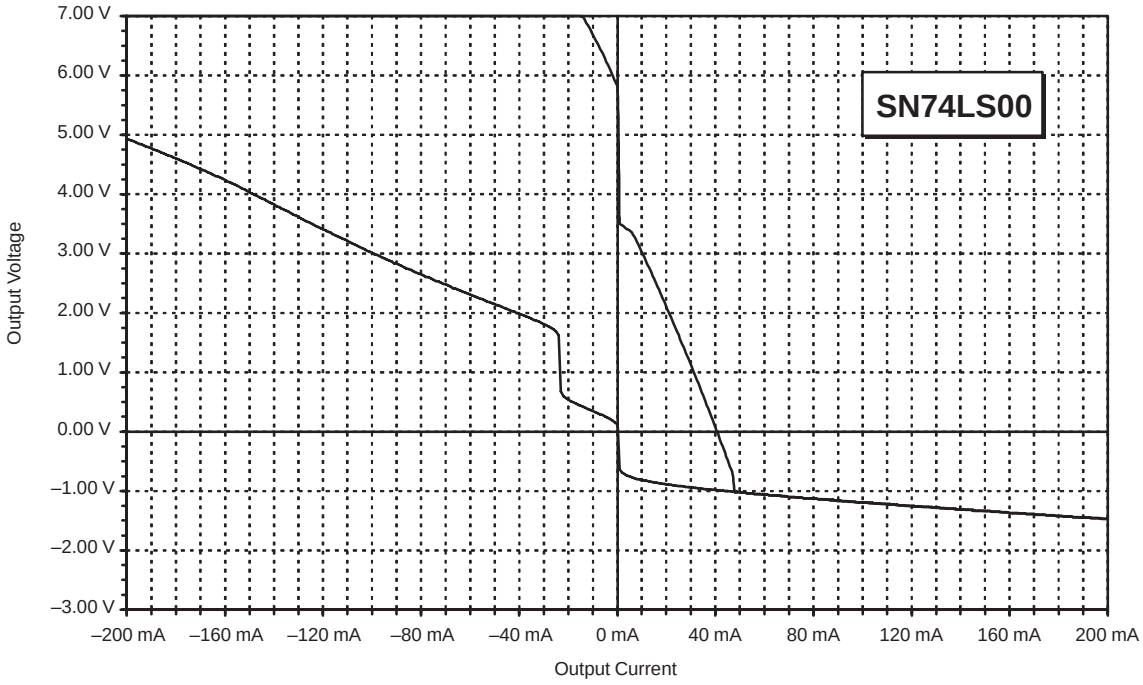


Figure 15. Output Characteristic of the SN74LS00

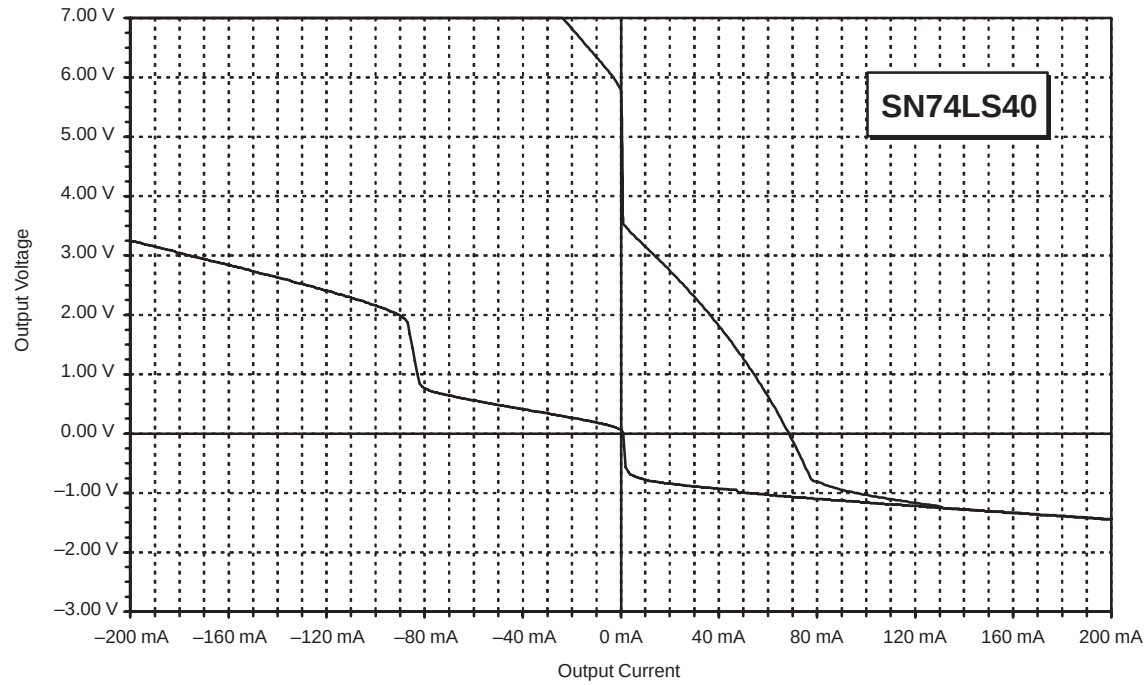


Figure 16. Output Characteristic of the SN74LS40

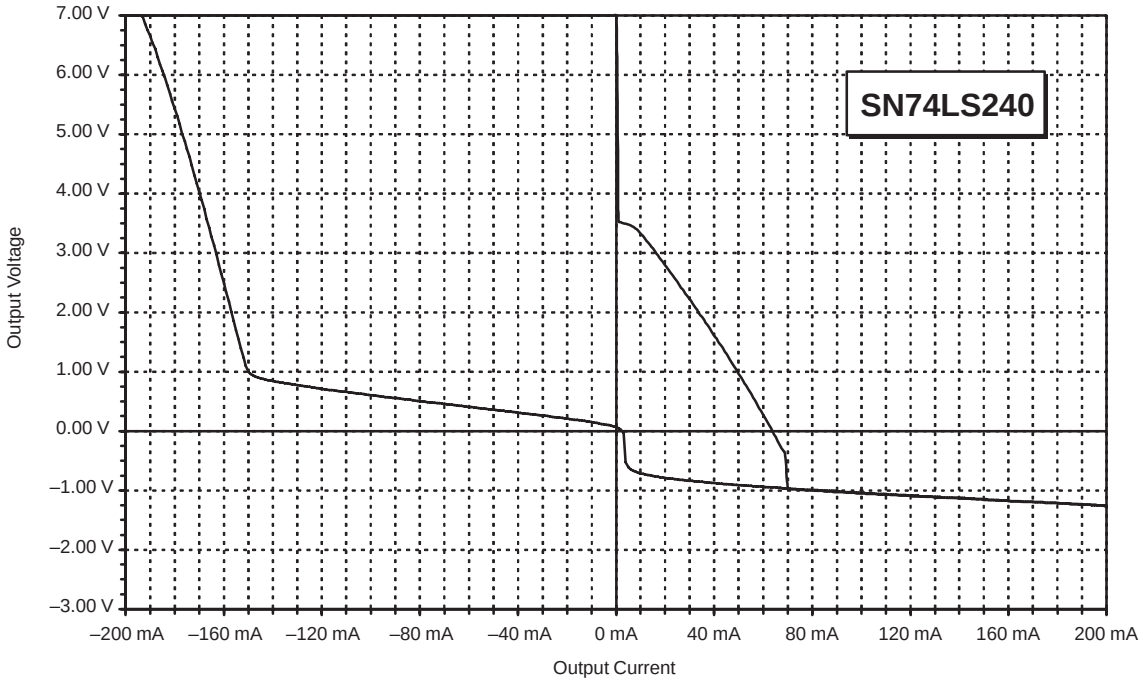


Figure 17. Output Characteristic of the SN74LS240

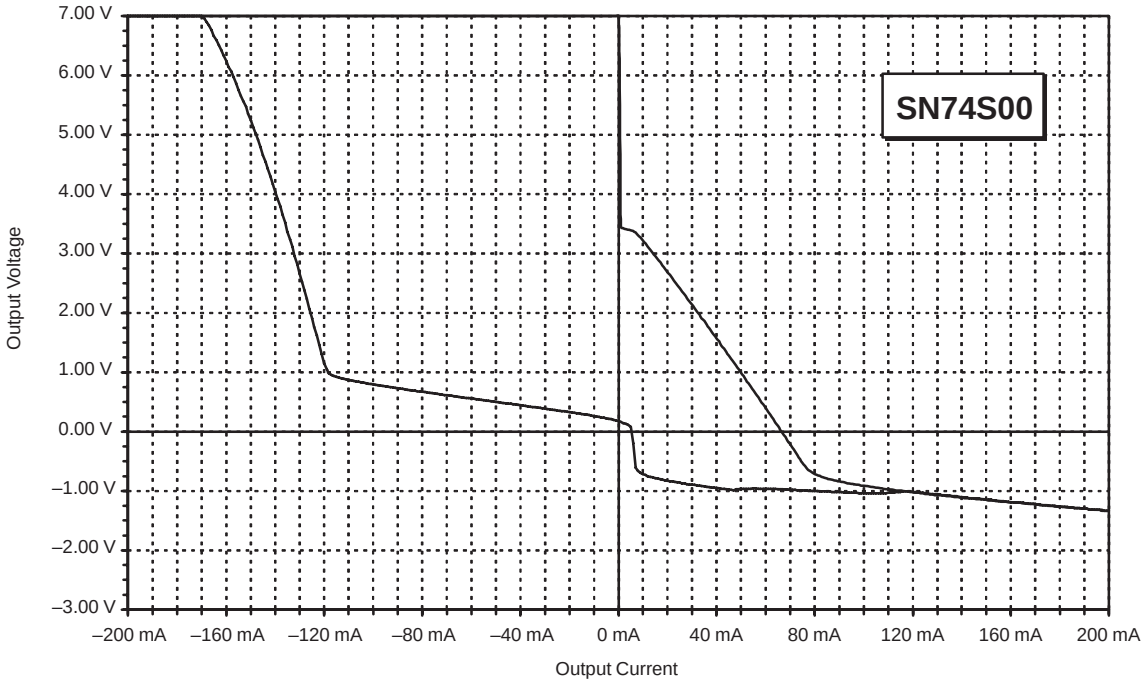


Figure 18. Output Characteristic of the SN74S00

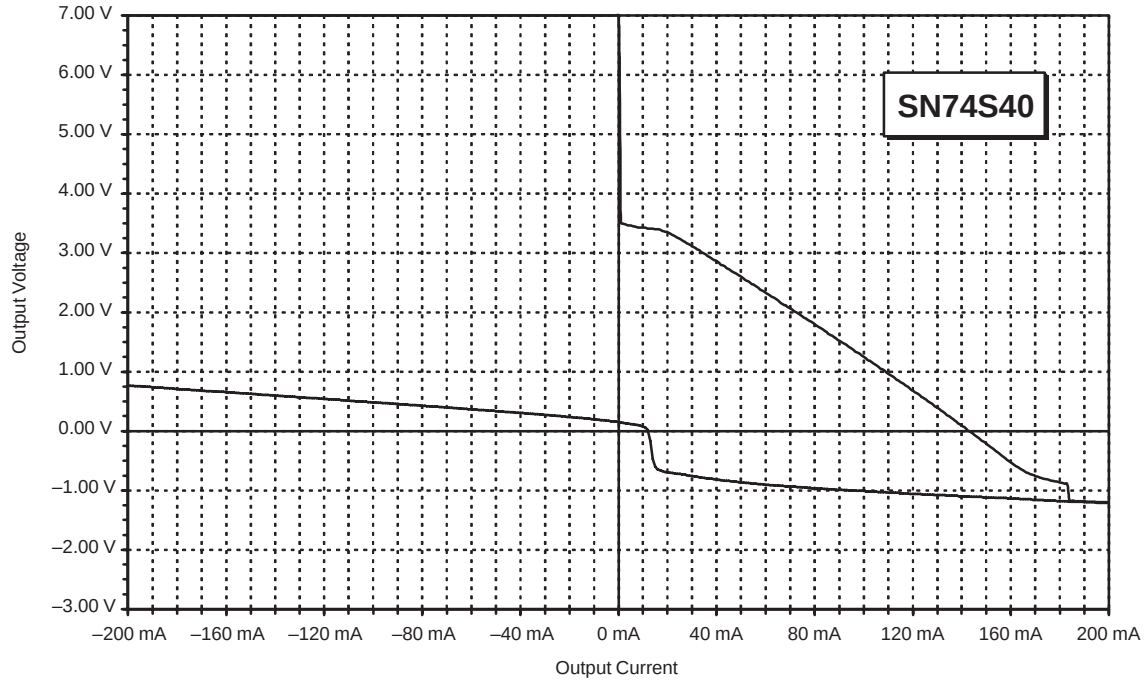


Figure 19. Output Characteristic of the SN74S40

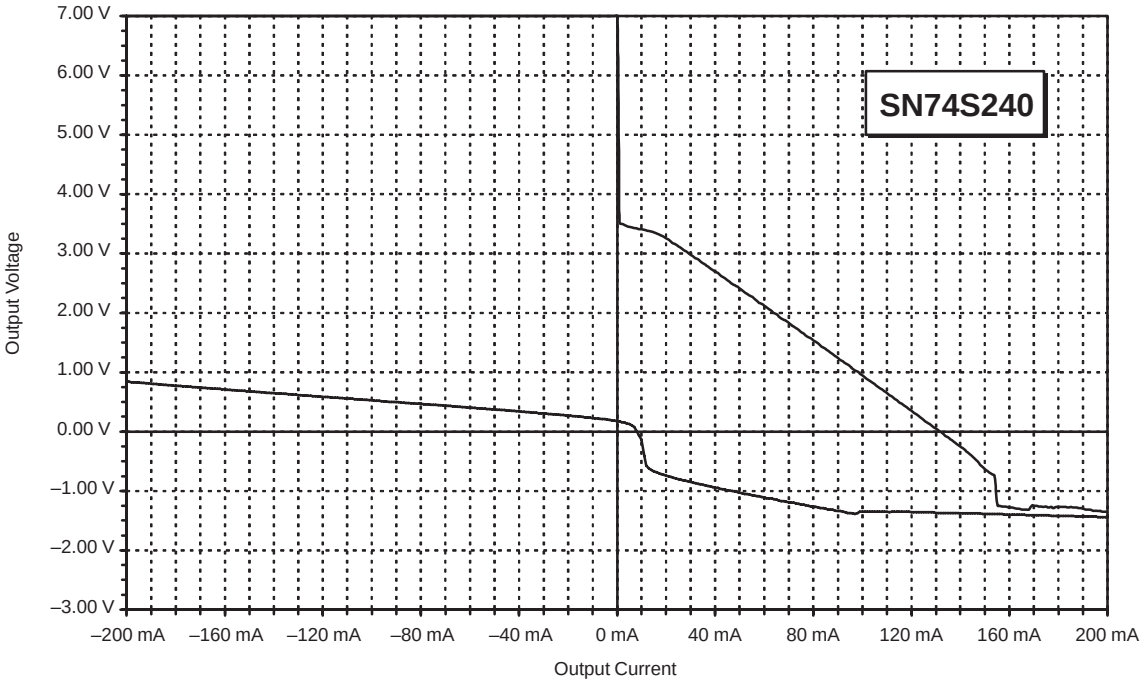


Figure 20. Output Characteristic of the SN74S240

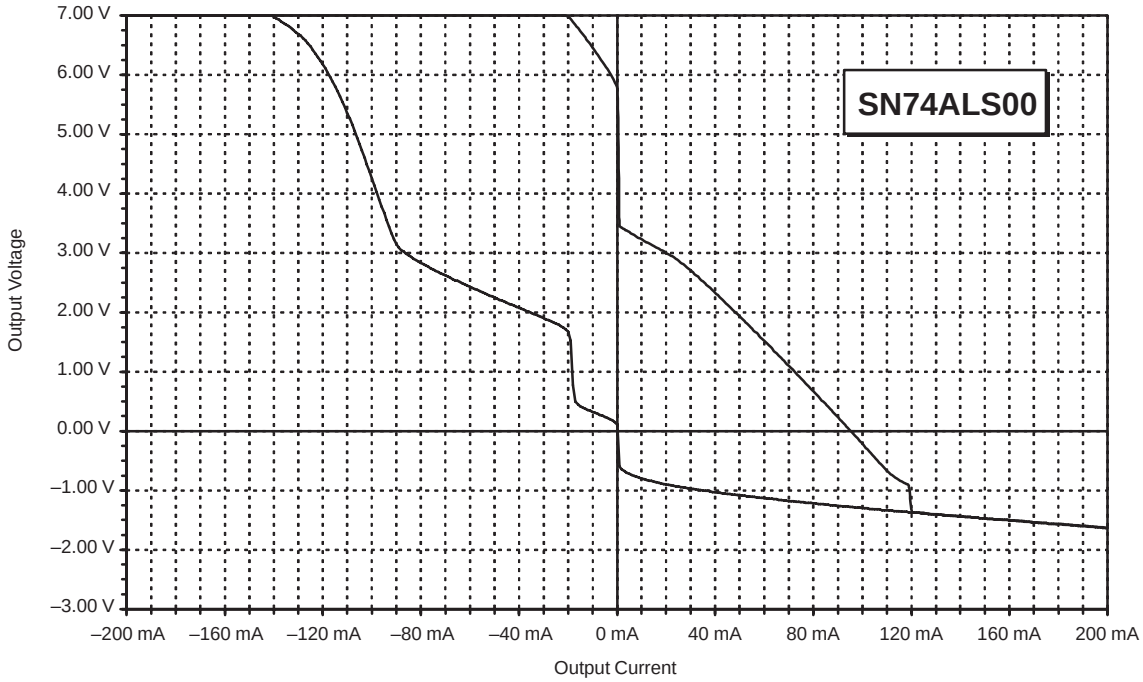


Figure 21. Output Characteristic of the SN74ALS00

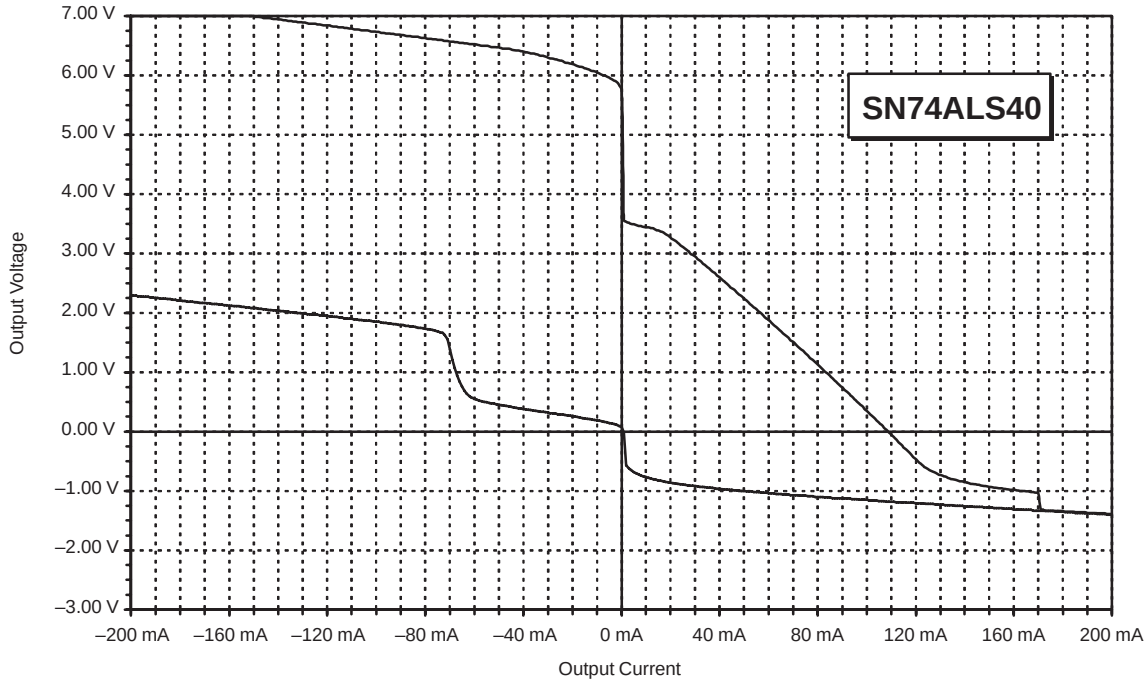


Figure 22. Output Characteristic of the SN74ALS40

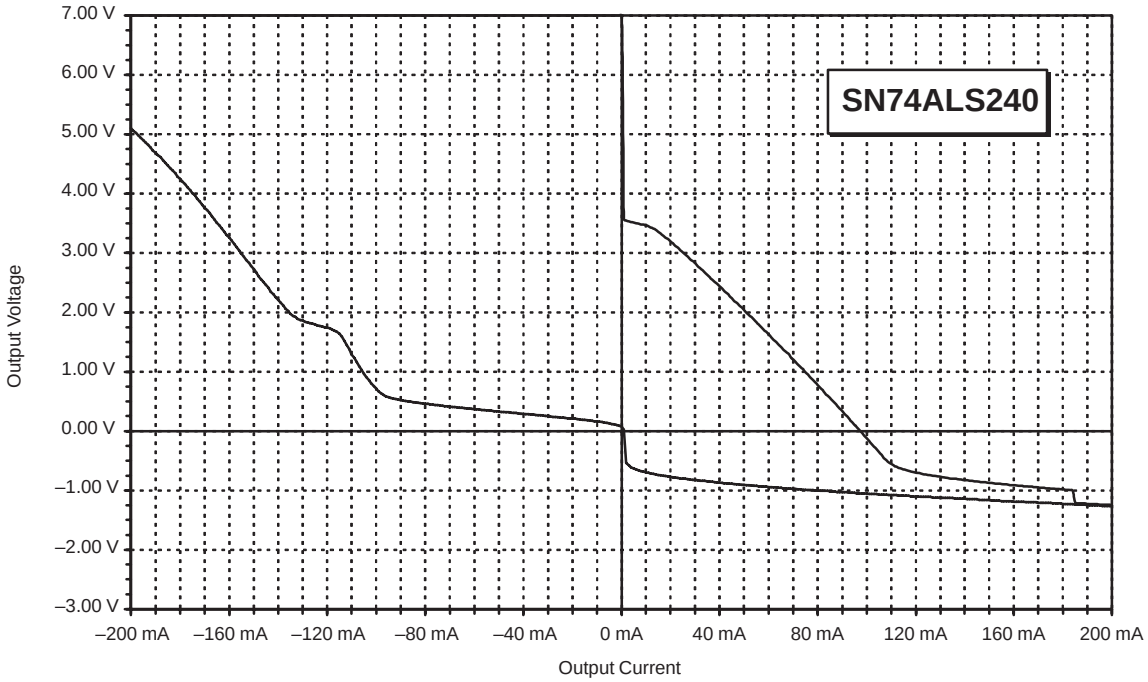


Figure 23. Output Characteristic of the SN74ALS240

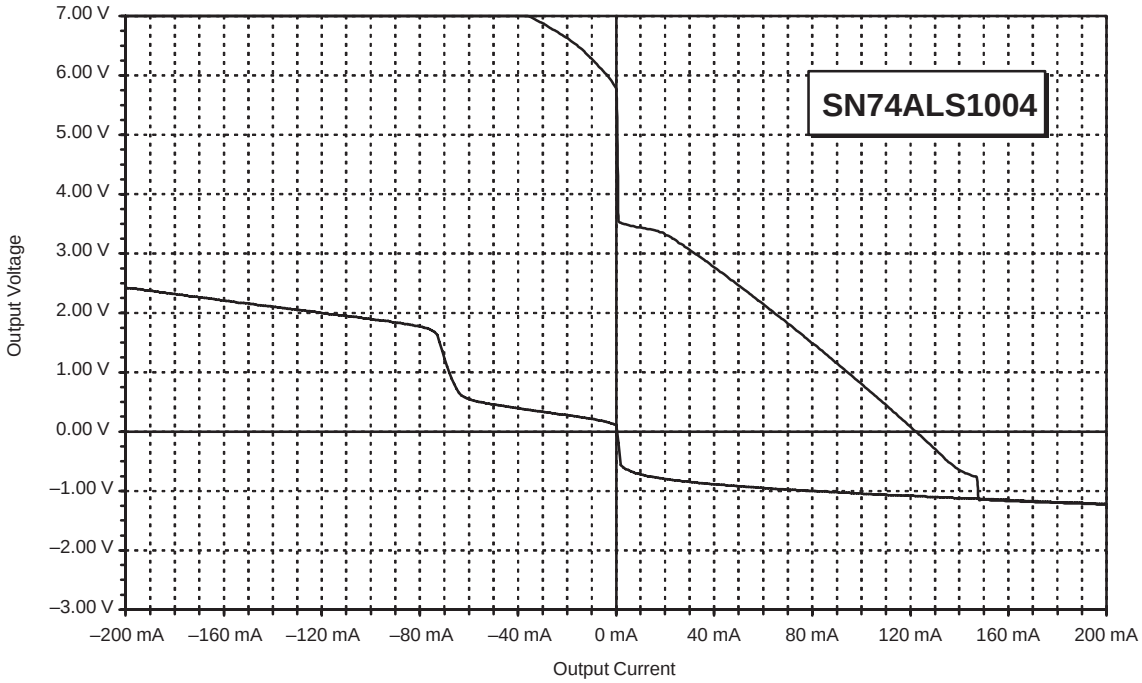


Figure 24. Output Characteristic of the SN74ALS1004

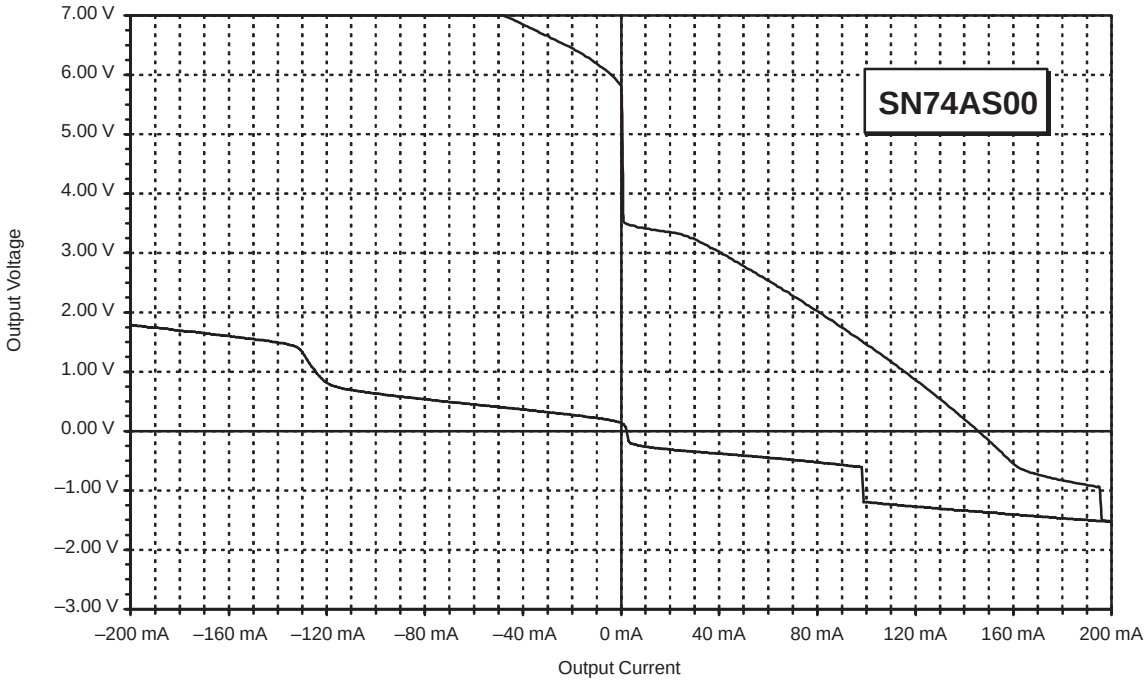
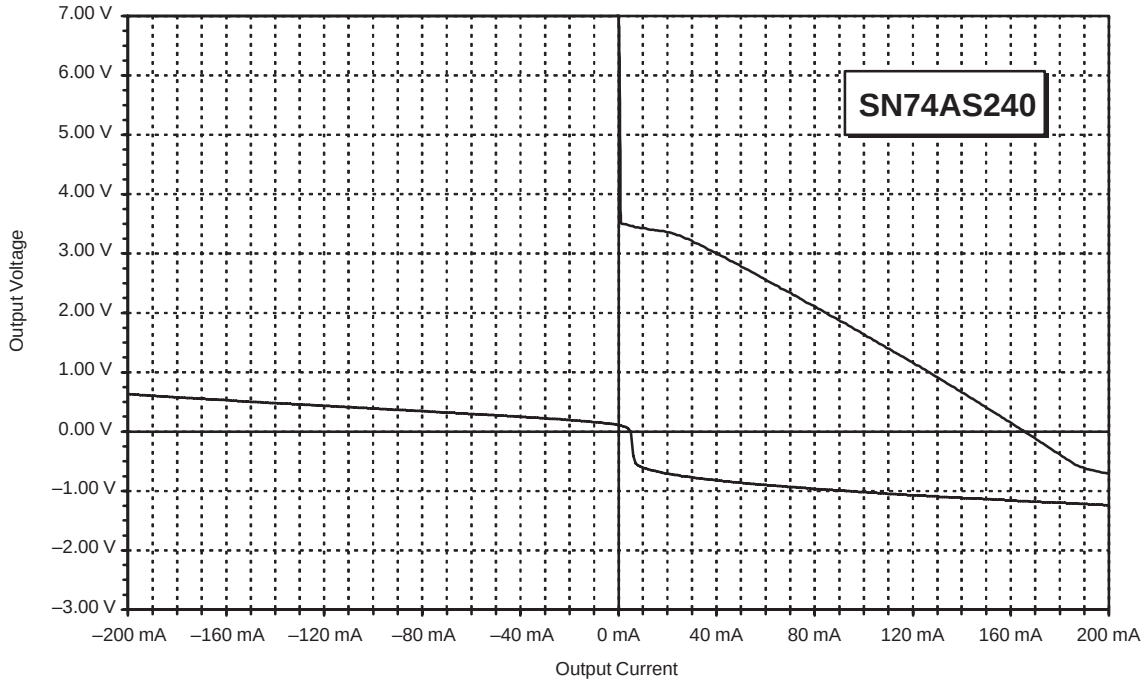


Figure 25. Output Characteristic of the SN74AS00



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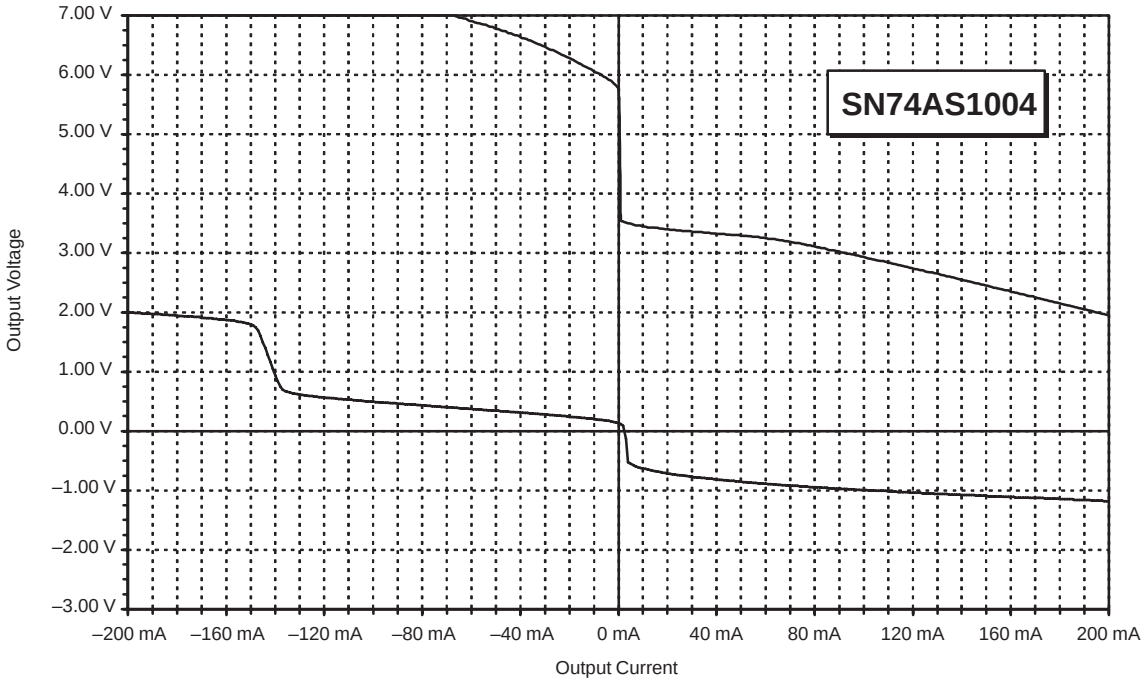


Figure 27. Output Characteristic of the SN74AS1004

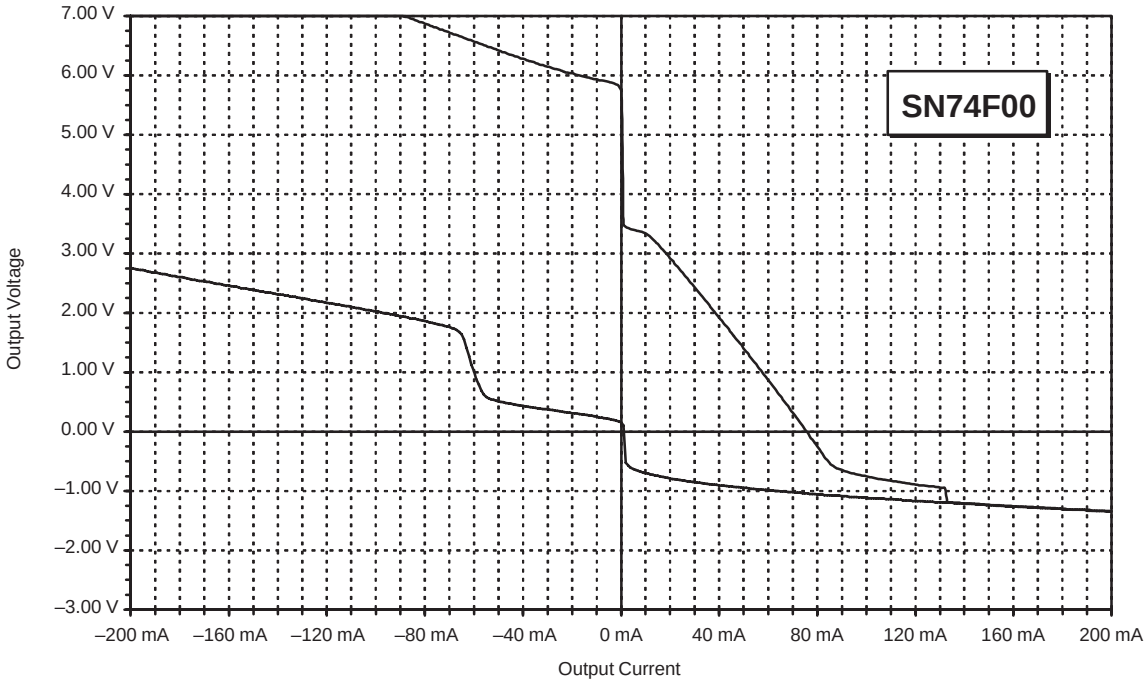


Figure 28. Output Characteristic of the SN74F00

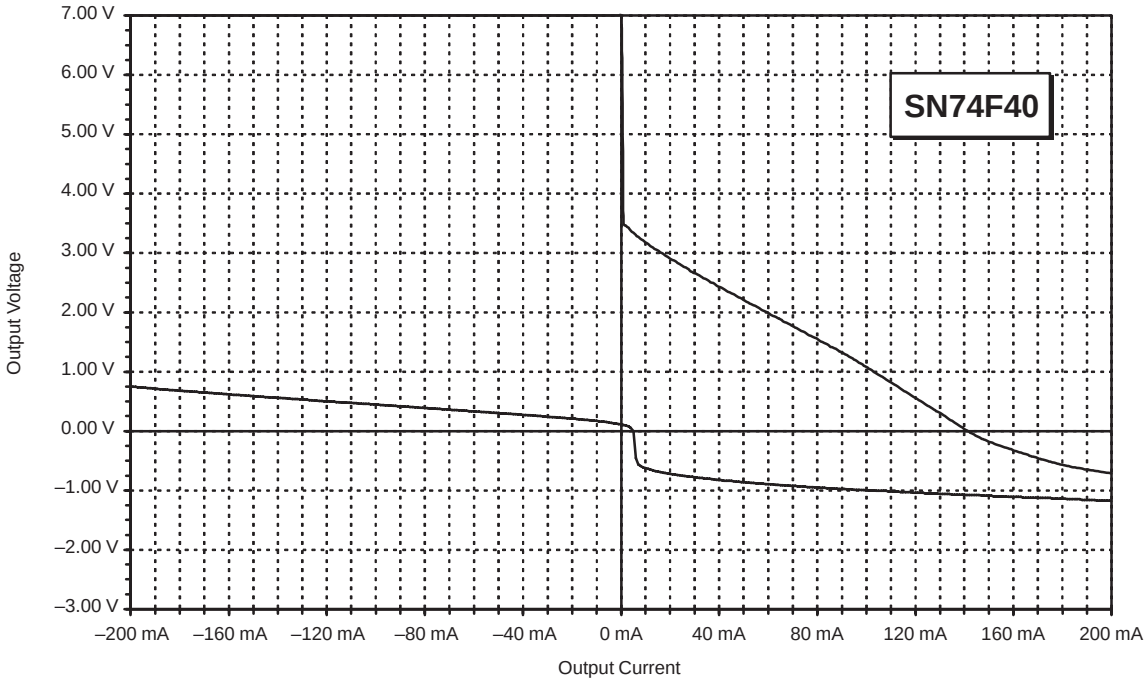


Figure 29. Output Characteristic of the SN74F40

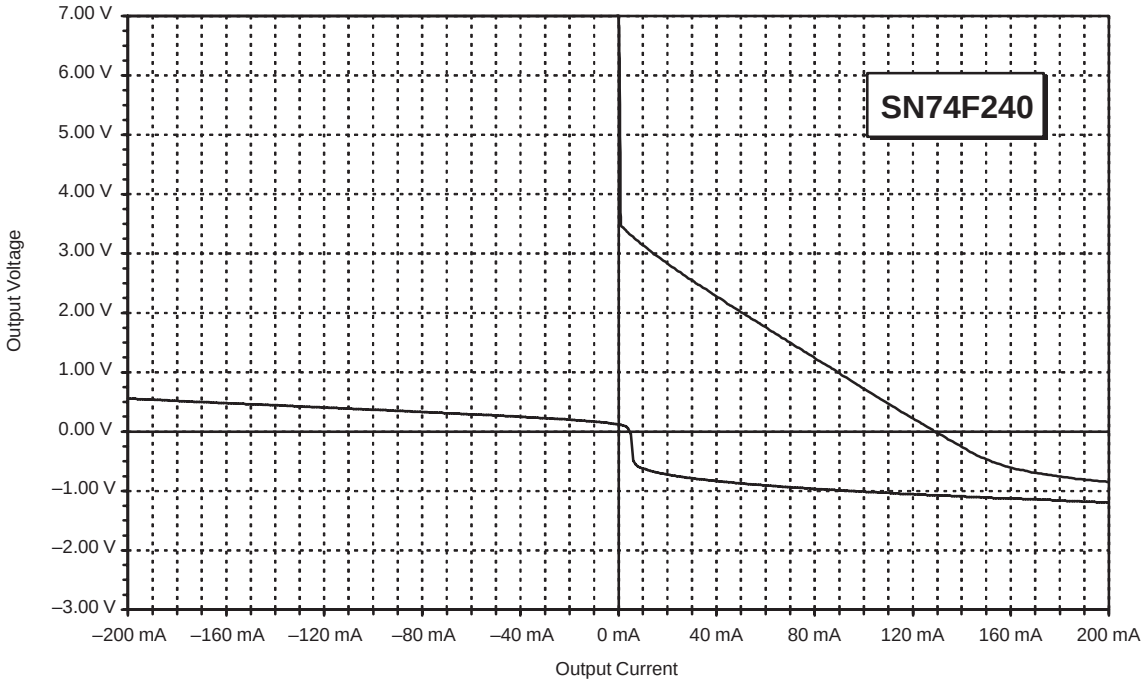


Figure 30. Output Characteristic of the SN74F240

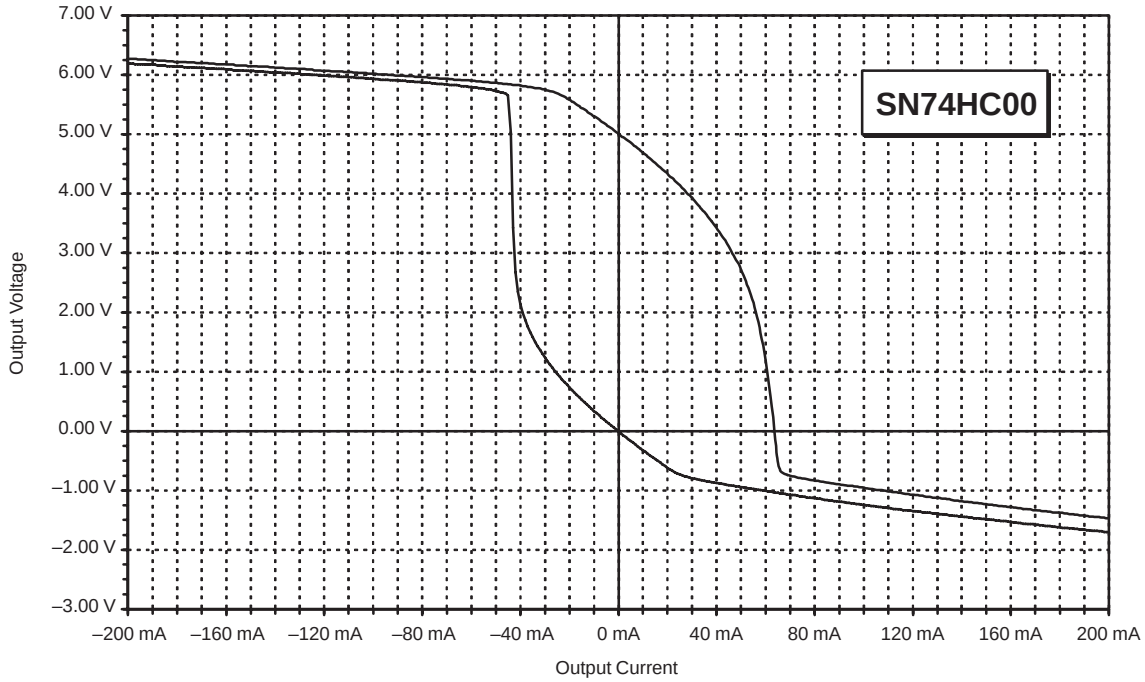


Figure 31. Output Characteristic of the SN74HC00

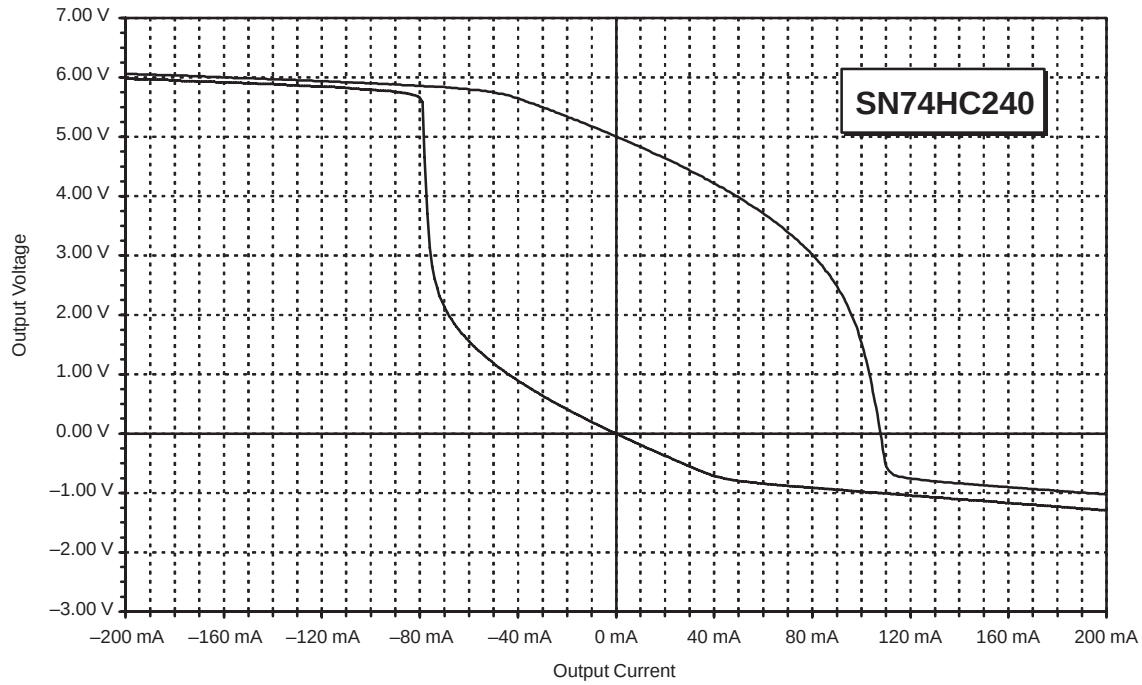


Figure 32. Output Characteristic of the SN74HC240

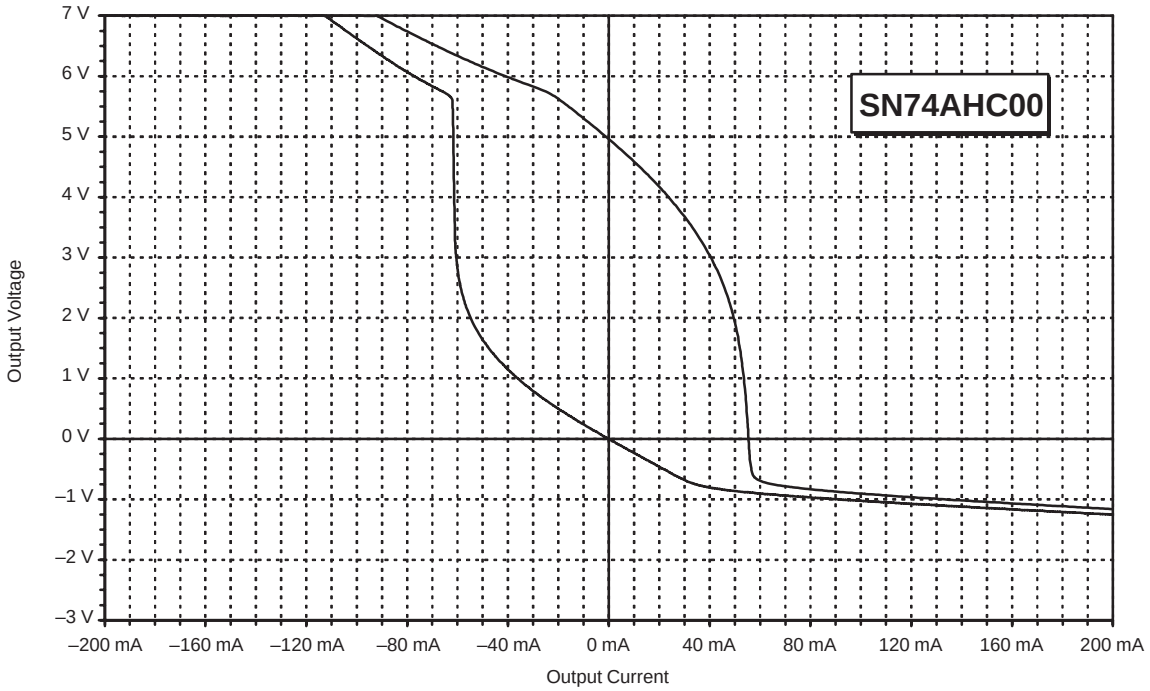


Figure 33. Output Characteristic of the SN74AHC00

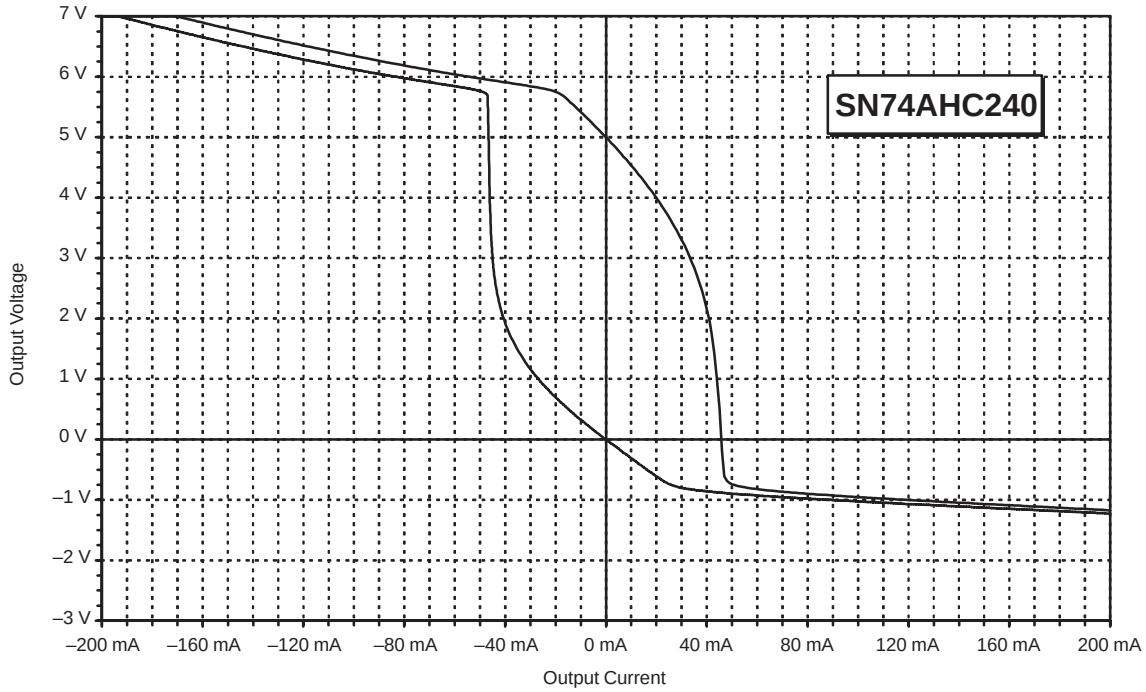
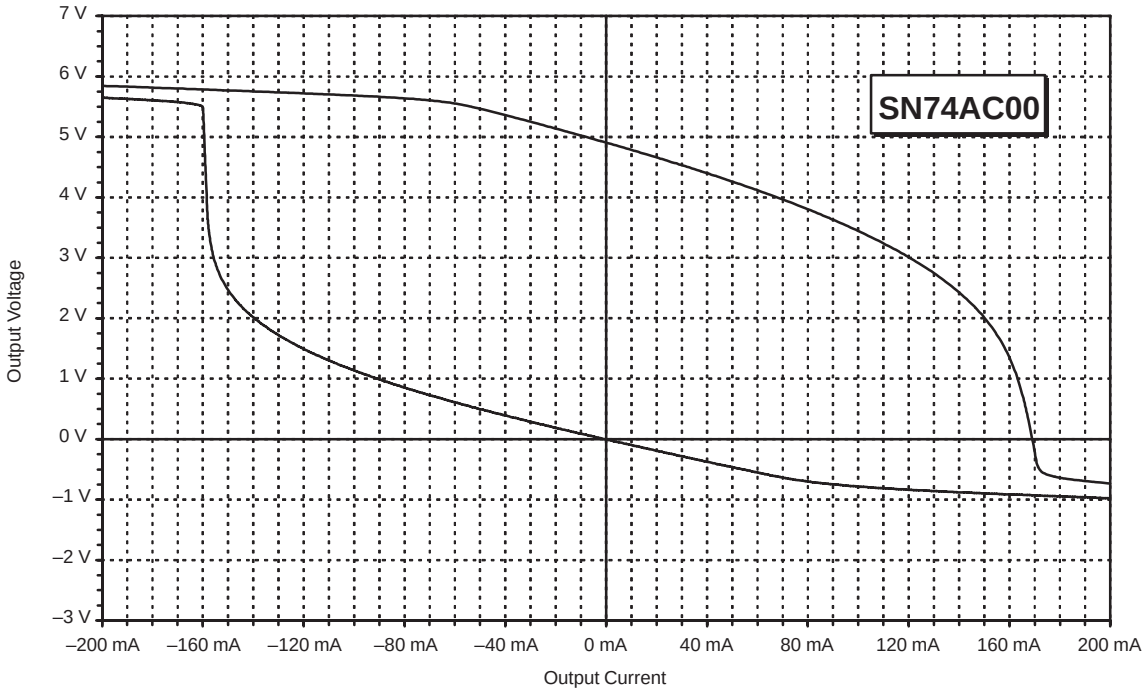


Figure 34. Output Characteristic of the SN74AHC240



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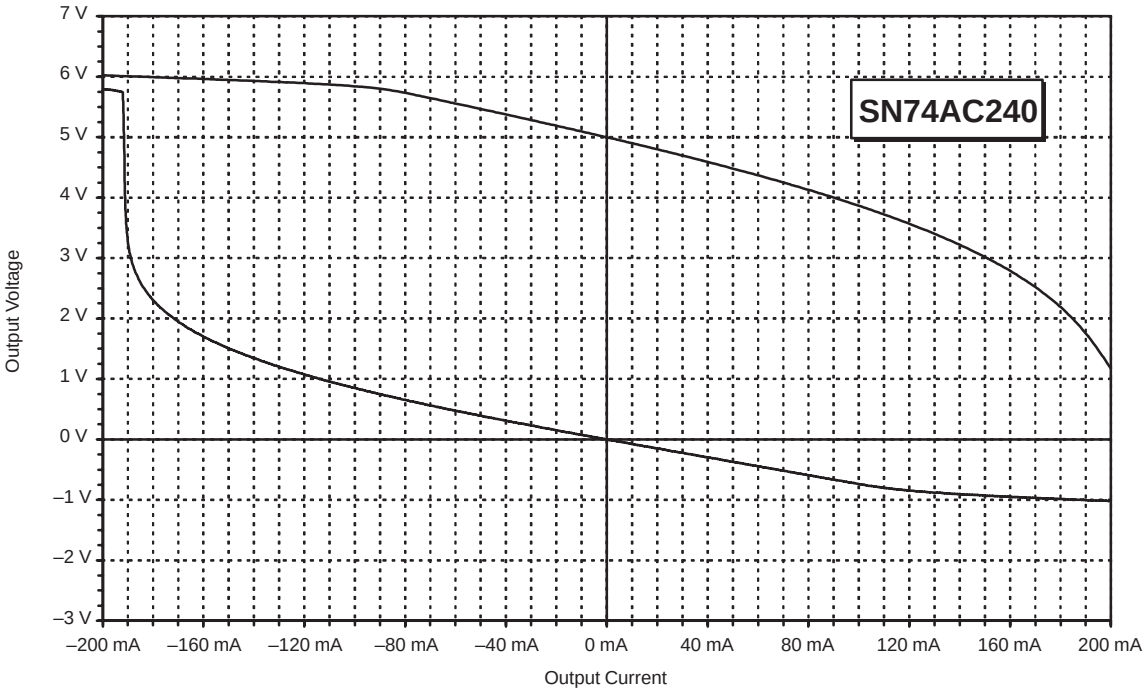

Figure 36. Output Characteristic of the SN74AC240

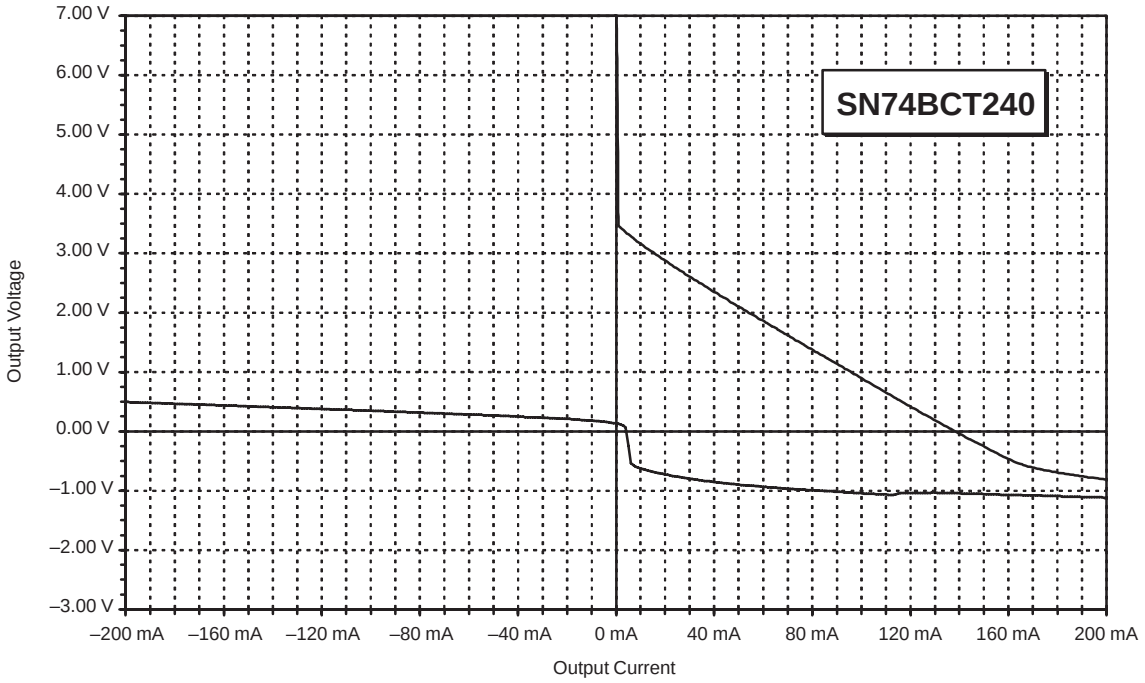

Figure 37. Output Characteristic of the SN74BCT240

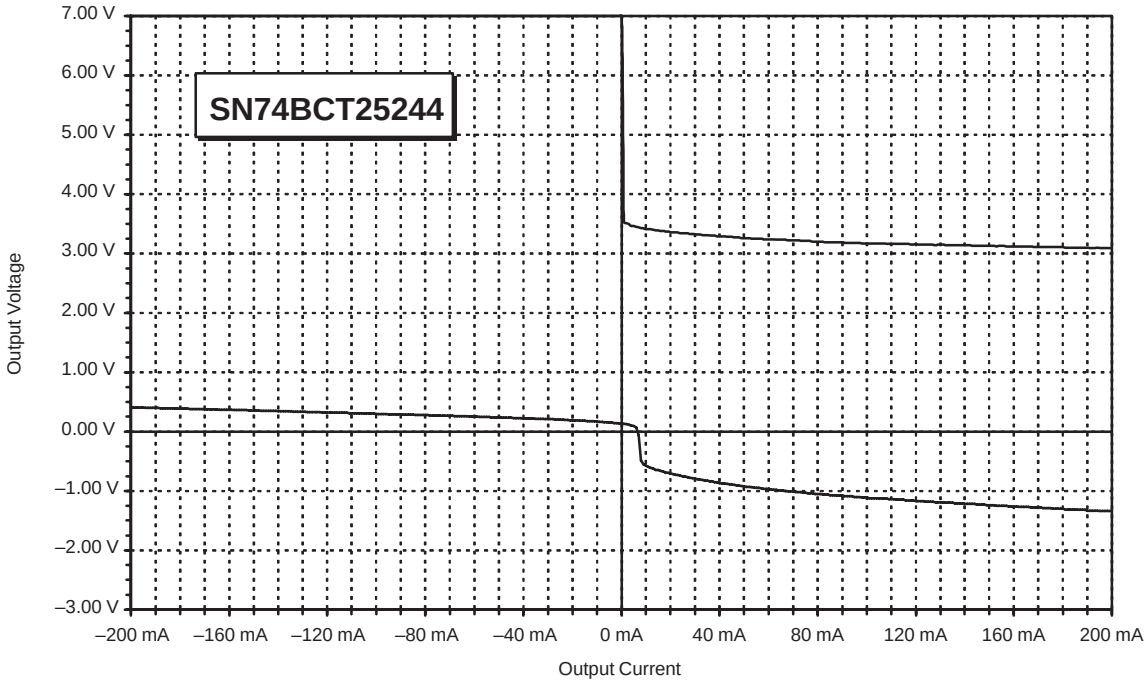

Figure 38. Output Characteristic of the SN74BCT25240

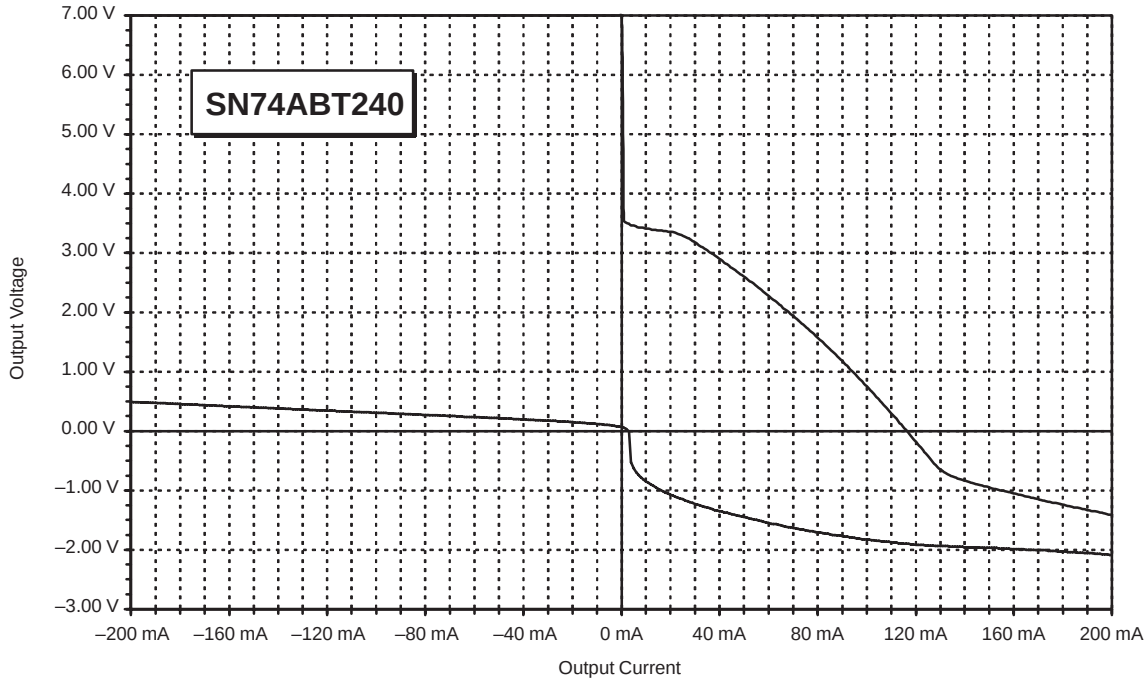

Figure 39. Output Characteristic of the SN74ABT240

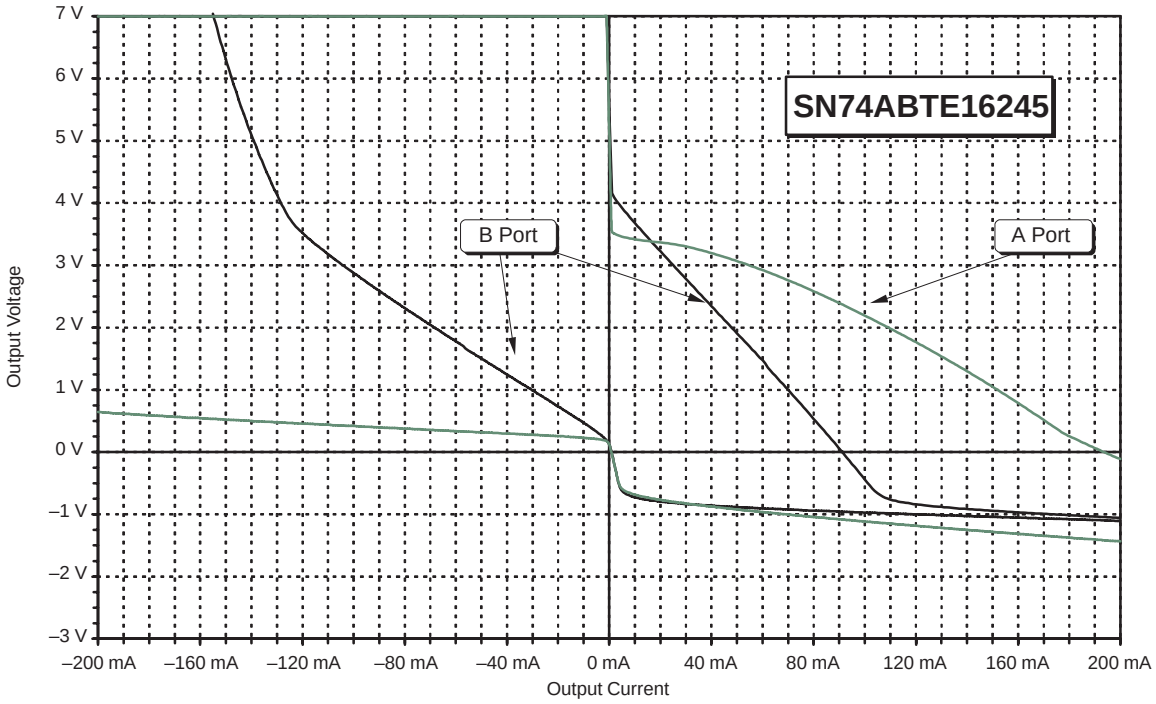

Figure 40. Output Characteristic of the SN7ABTE16245

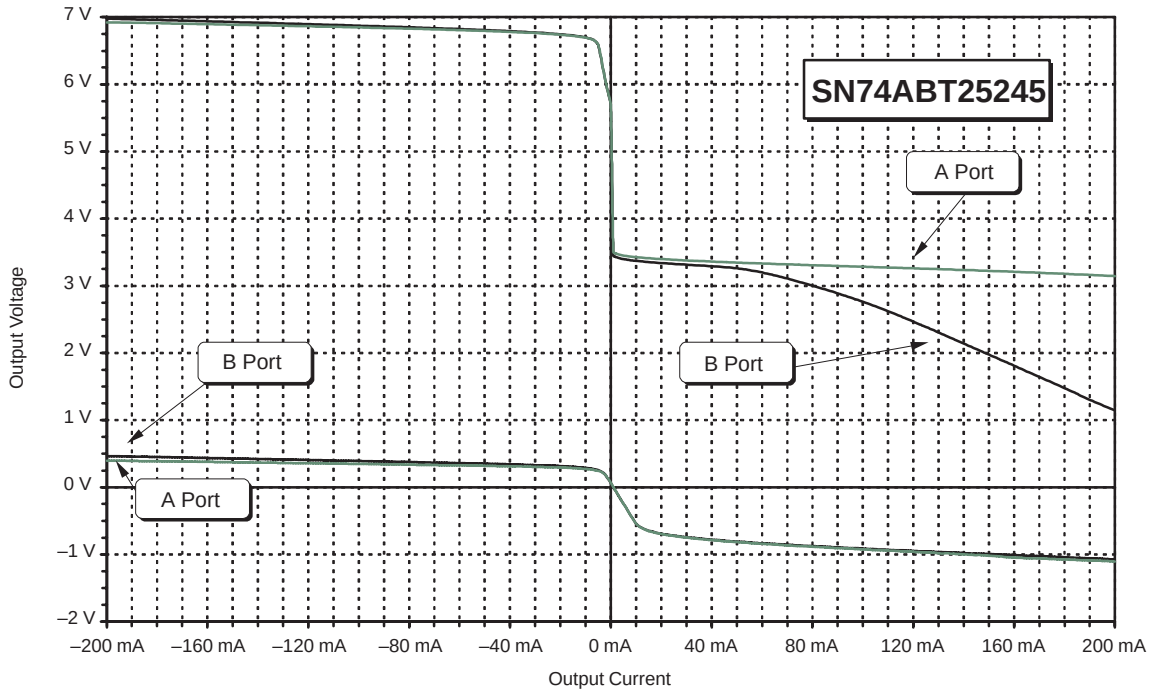

Figure 41. Output Characteristic of the SN74ABT25245

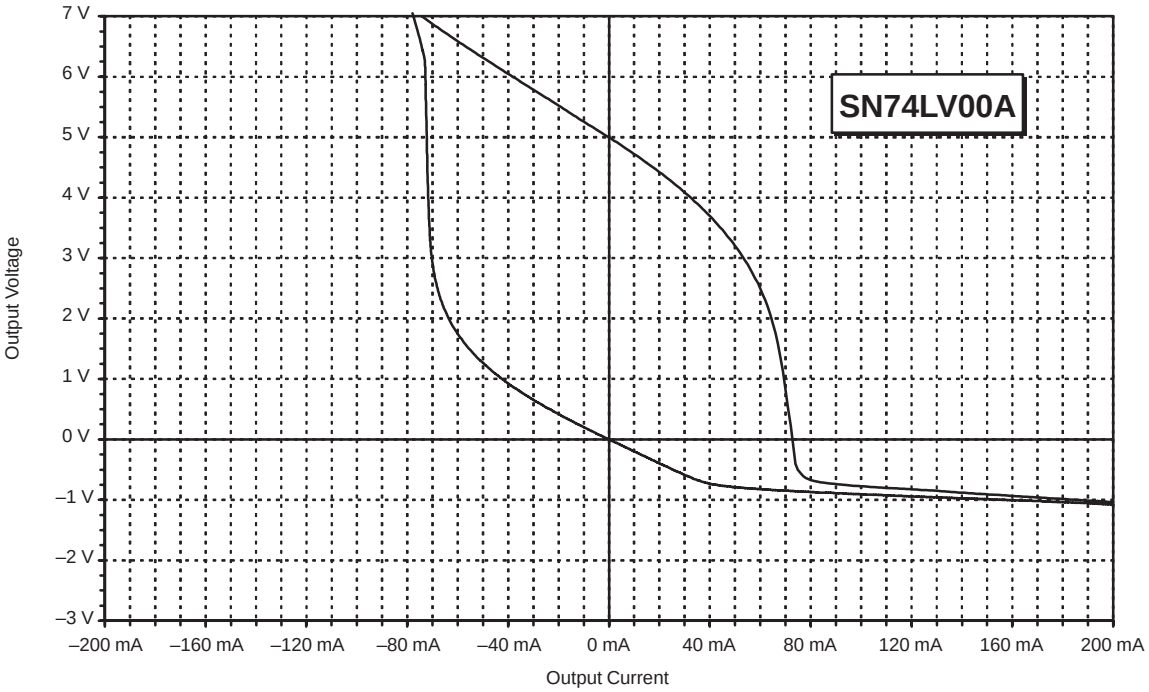

Figure 42. Output Characteristic of the SN74LV00A

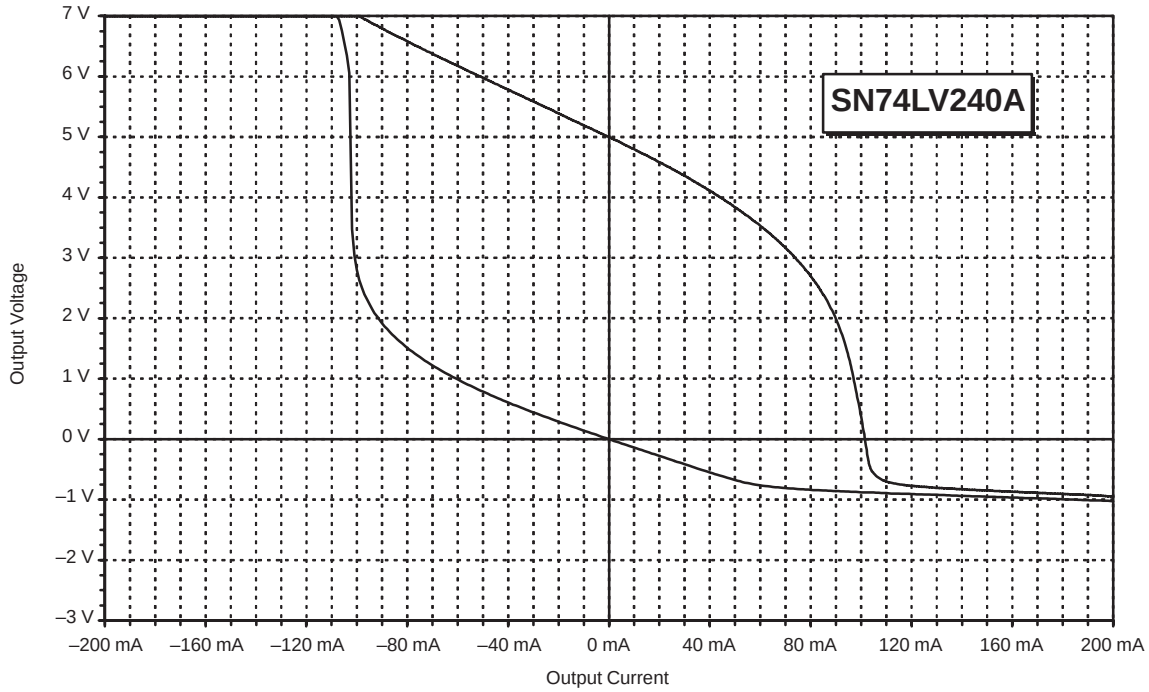

Figure 43. Output Characteristic of the SN74LV240A

4 Bergeron Method Applied to the SN74AHC240

The input and output characteristics, shown in Section 1, *Introduction*, and Section 3, *Output Characteristics*, can be used to determine the signal reflections within a certain application using a graphical procedure known as the Bergeron method.

The prerequisite to using the Bergeron method is that the lines must exceed a certain length. There is a simple rule:

> *If the rise time or the fall time of a signal is shorter than twice the propagation delay on the line, the line theories must be applied.*

Practically, this means that for a line with a signal propagation time of 5 ns/m and a signal with a rising or falling edge of 2 ns, starting with a line length that exceeds 20 cm [2 ns / (5ns/m × 2)], the line theory must be applied.

For a bus line, the signal propagation delay increases to 25 ns/m, so that, in this case, the line theory must be applied for a line that exceeds 4 cm [2 ns / (25 ns/m × 2)]

In the example, the SN74AHC240 device was tested. The Bergeron method was used to determine the signal shape in advance. The measurement setup is shown in Figure 44.

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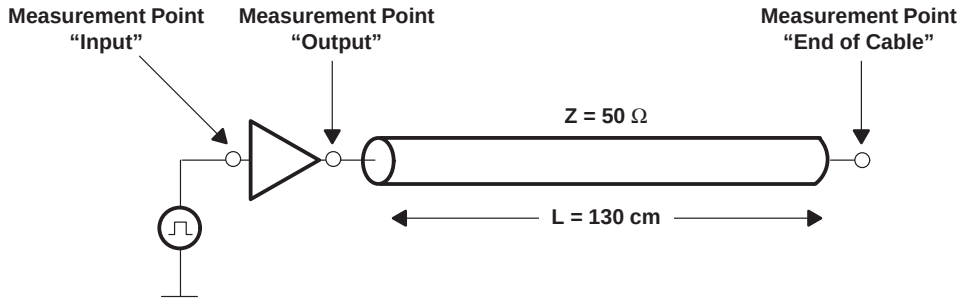

Figure 44. Measurement Setup for the Bergeron Method

The first step in doing the graphical solution using the Bergeron method is to draw the output and load characteristics in a voltage-versus-current diagram:

- Output characteristic of the device SN74AHC240
- Load characteristic at the end of the line

The output characteristic is taken directly from Figure 45. The load characteristic equals the Y-axis for the investigated case, because no resistor is connected to the end of the line ($R_L = \infty$).

The intersection between the load characteristic and the output characteristic represents the steady states and the current and voltage values at the line start and the end of the line at the time $t < 0$, respectively.

4.1 Voltage Value at the Output of the Driver

For the low-to-high transition, a straight line is drawn, starting at the intersection of the output low characteristic and the load characteristic. For the high-to-low transition, the straight line starts at the cross point of output high characteristic and the load characteristic.

The line impedance, Z_O, determines the steepness of this line. In the example, the line impedance is 50 Ω.

The intersection of this straight line and the output characteristics gives the voltage and current values at the beginning of the line at the time t = 0.

4.2 Voltage Value at End of the Line

Now, a straight line with the steepness $–Z_O$ is drawn through this point. The intersection between this line and the load characteristic gives the voltage values at the end of the line after one propagation delay time of the line, that is after time t = 1.

Afterwards, the procedure will be repeated, applying straight lines to the output characteristic and the load characteristic.

The steepness of the straight line is:

- Z_O from the output characteristic to the load characteristic and
- $–Z_O$ from the load characteristic to the output characteristic.

In this way, the current/voltage values are determined:

- at the end of the line, at the times t = 1, 3, 5 . . .
- at the beginning of the line, at the times t = 2, 4, 6 . . .

The Bergeron diagram is shown in Figure 45. The related diagram, which shows the line reflections, is shown in Figure 46.

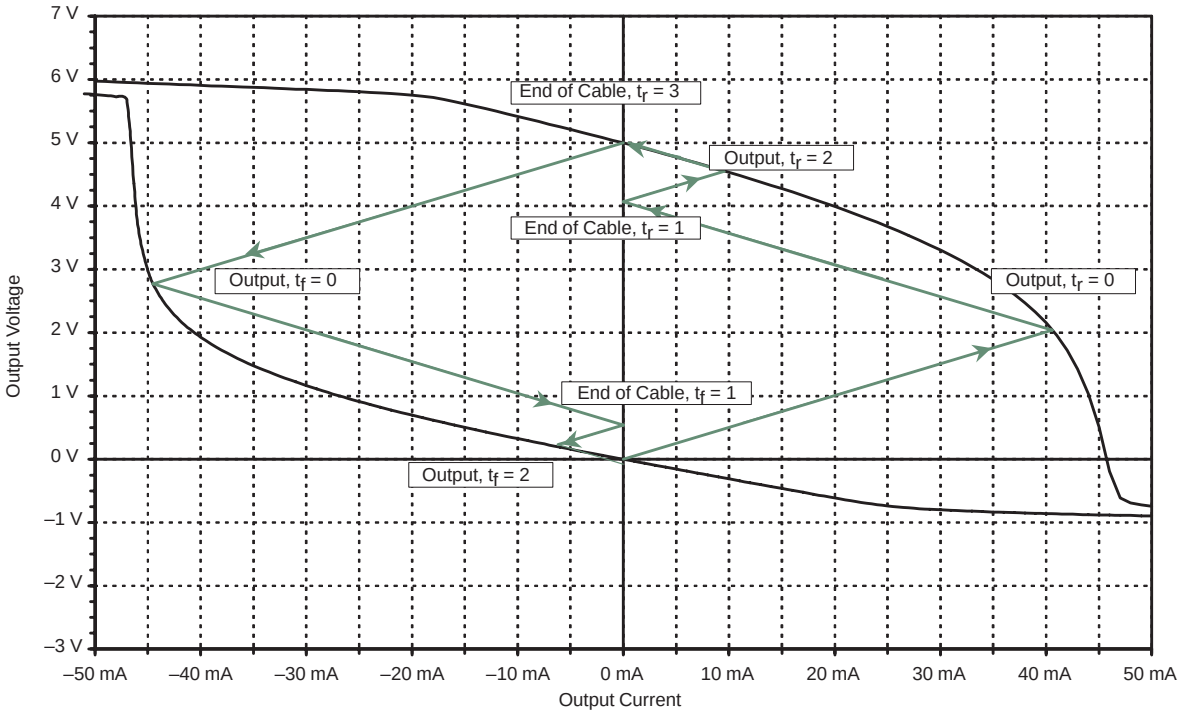

Figure 45. Bergeron Diagram for the SN74AHC240

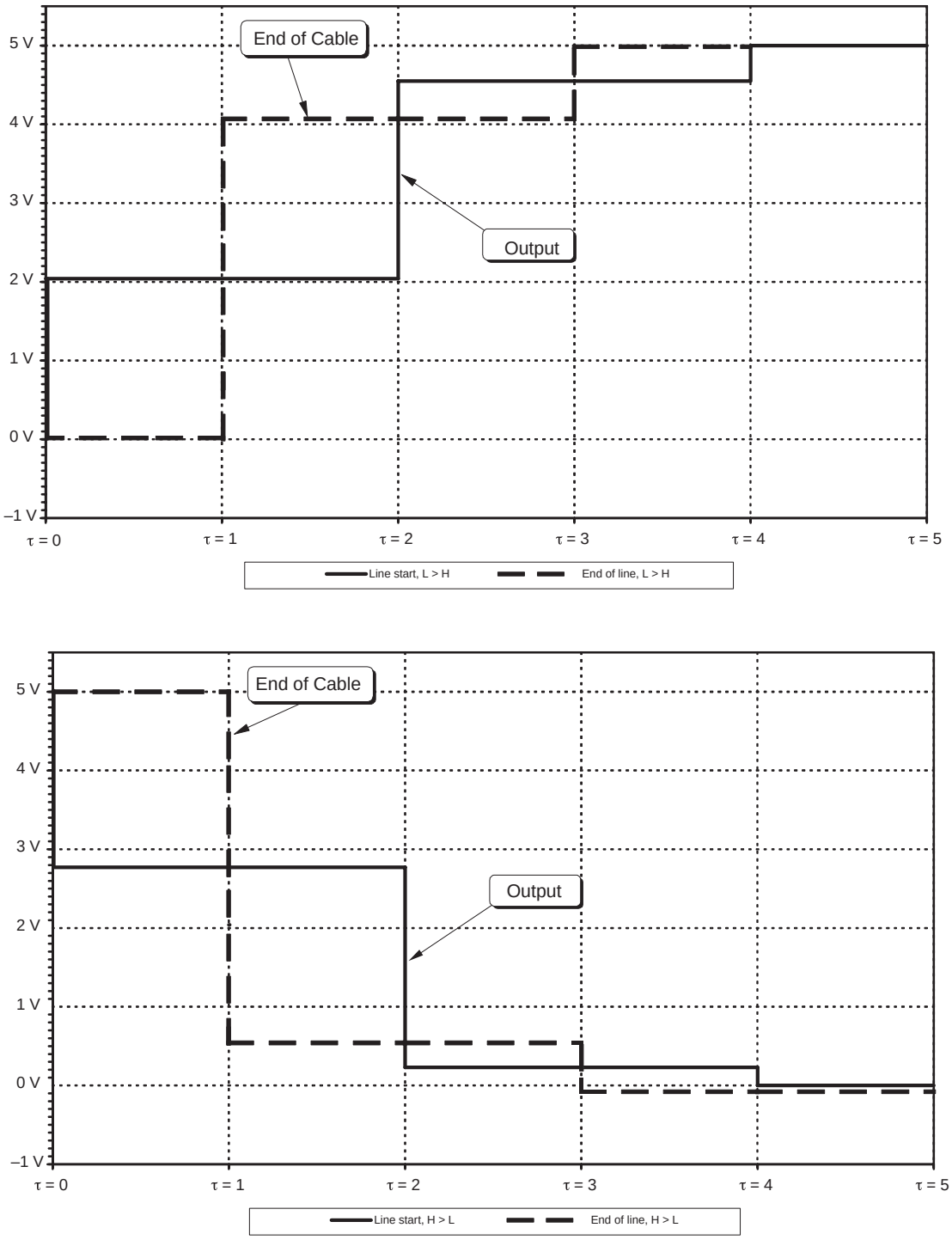

Figure 46. Diagram of Line Reflections for the SN74AHC240

Figure 47 shows the line-reflection measurement results for the SN74AHC240.

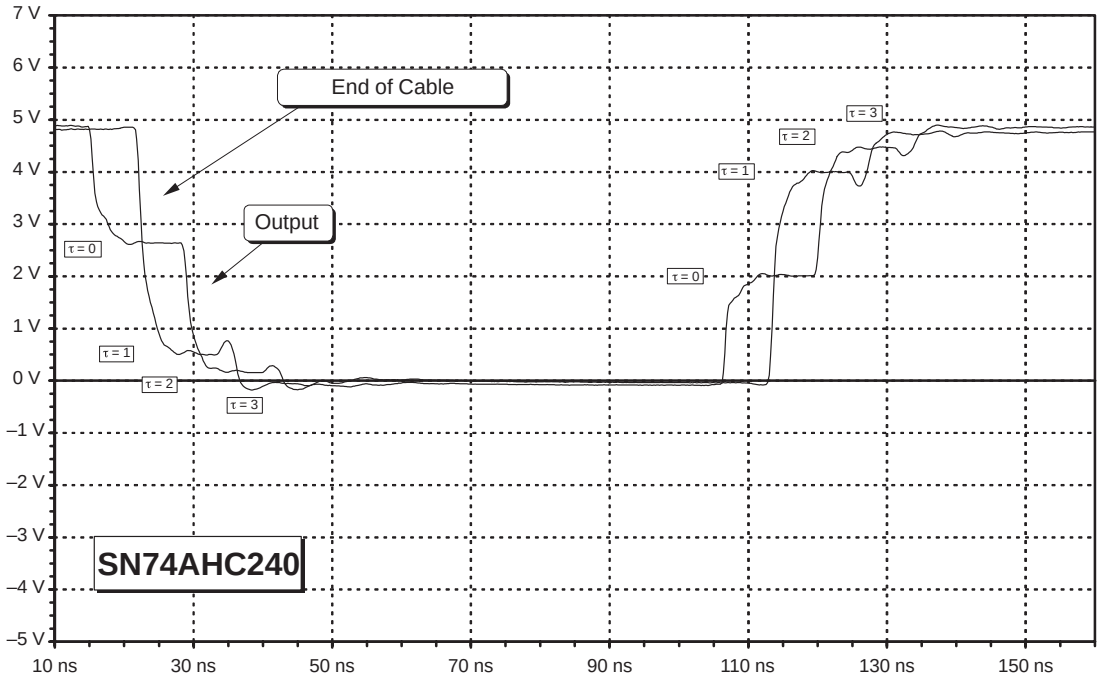

Figure 47. Signal Shape of the SN74AHC240

The calculated values using the Bergeron procedure match very well with the measurement of the signal shapes. The TI application report, *The Bergeron Method: A Graphic Method for Determining Line Reflections in Transient Phenomena*, literature number SDYA014, describes the graphic procedure in more detail.

5 Output Waveforms

The measurement setup shown in Figure 48 is used to obtain the voltage waveforms of typical output stages (see Figures 49 through 77).

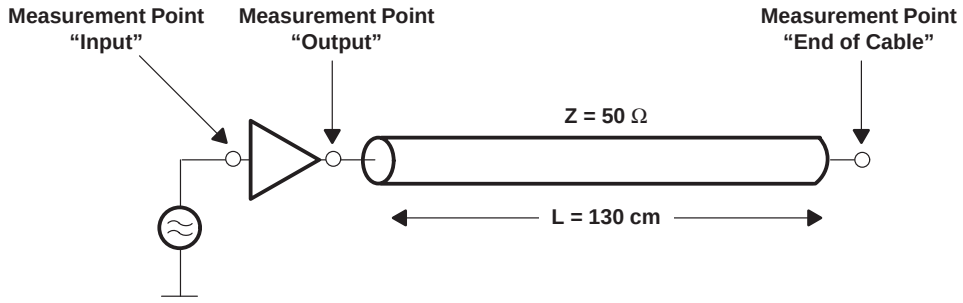

Figure 48. Measurement Setup for the Bergeron Method

For these measurements, the devices under test were loaded with a 1.3-m-long coaxial cable having a characteristic impedance of 50 Ω. The end of the line was not connected, i.e., open circuit.

These waveforms provide good insight into the dynamic behavior of the components. In particular, the oscillograms provide information regarding drive capability with a low-resistance load, together with an indication of the line reflections that can be expected.

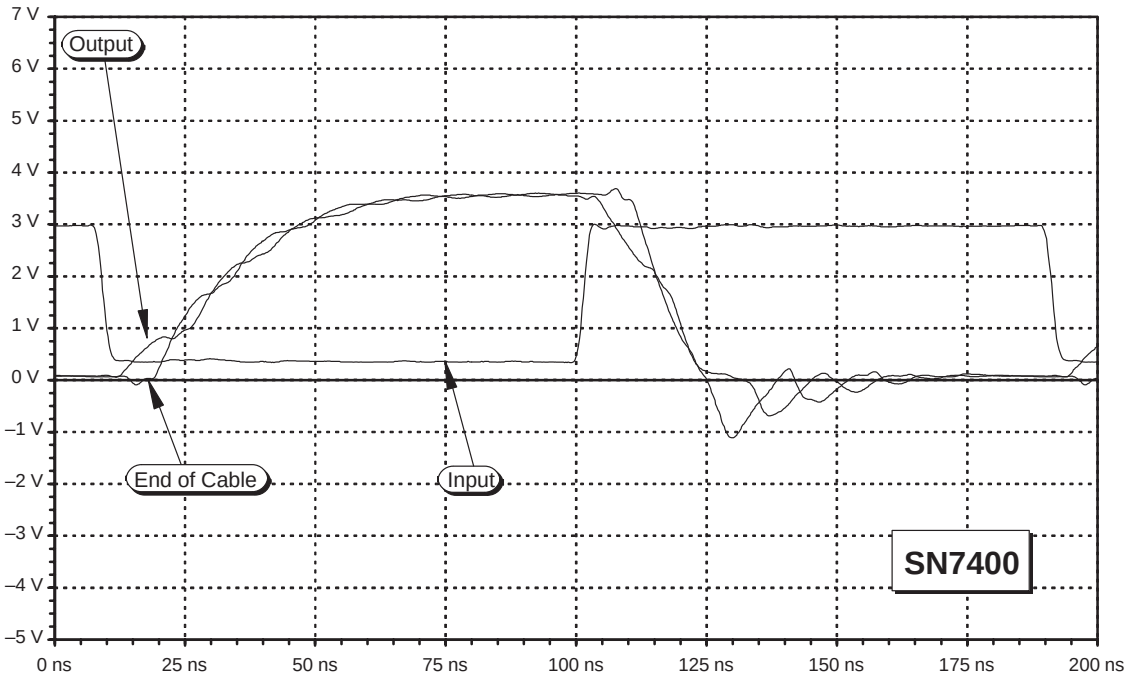

Figure 49. Output Waveforms of the SN7400

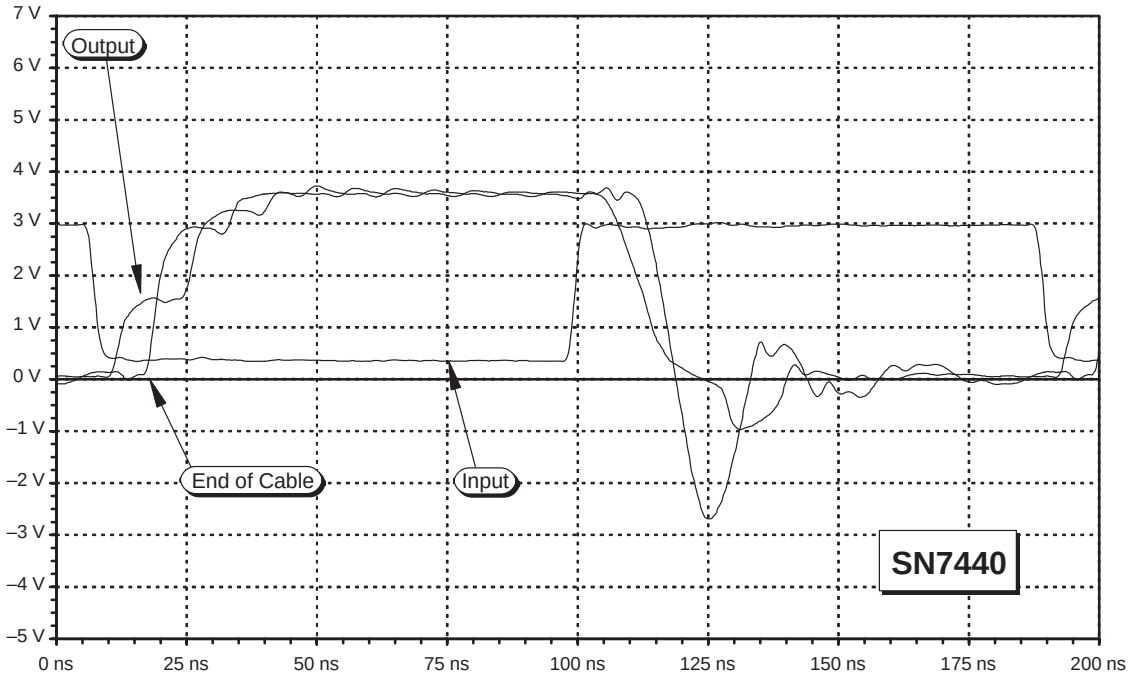

Figure 50. Output Waveforms of the SN7440

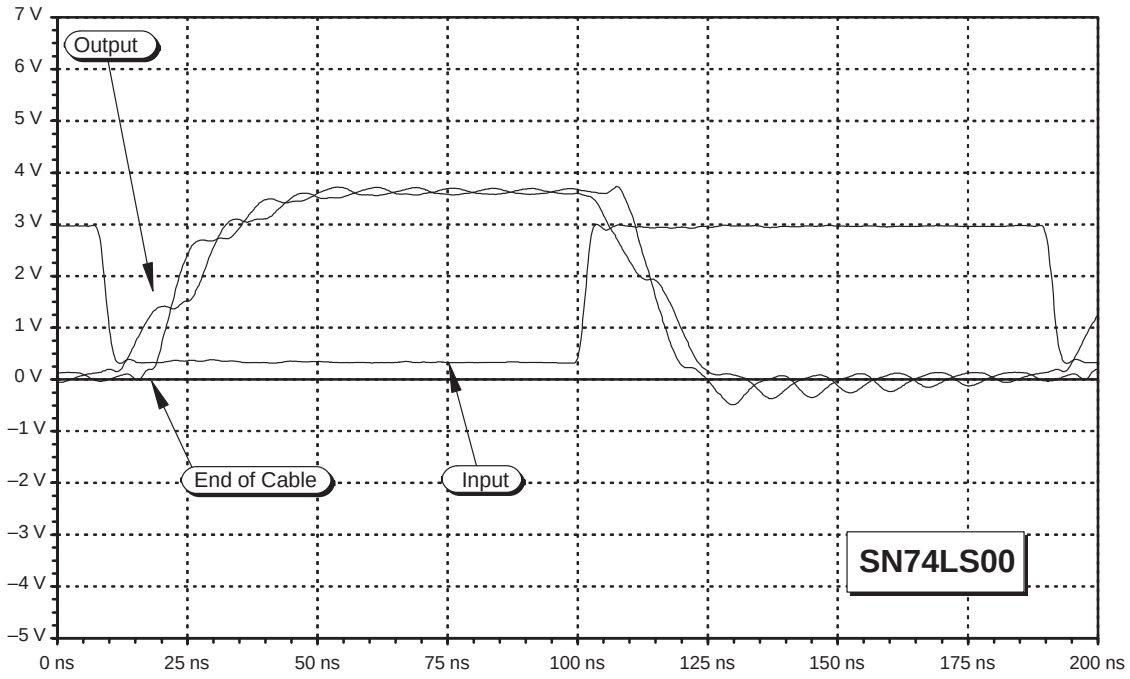

Figure 51. Output Waveforms of the SN74LS00

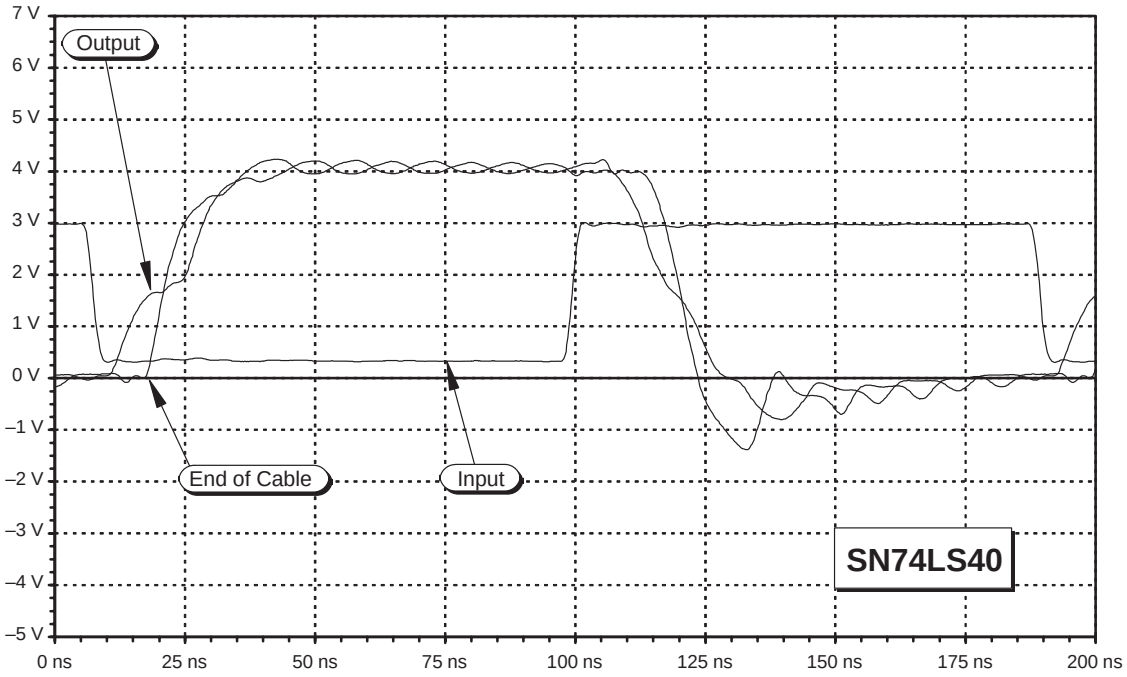

Figure 52. Output Waveforms of the SN74LS40

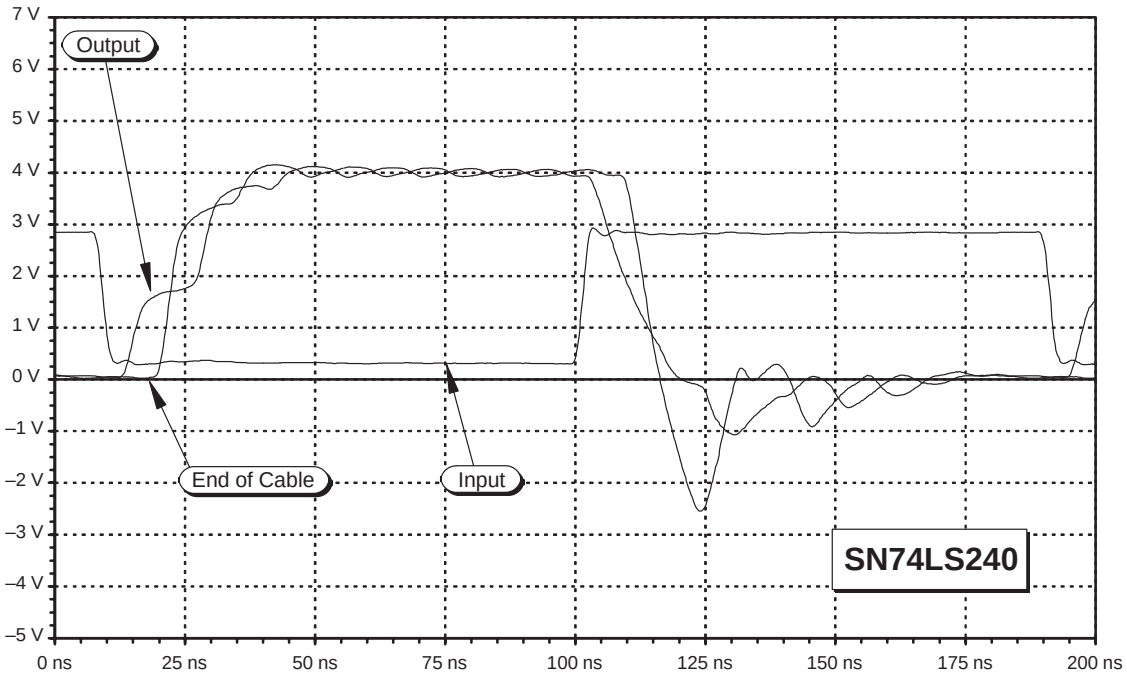

Figure 53. Output Waveforms of the SN74LS240

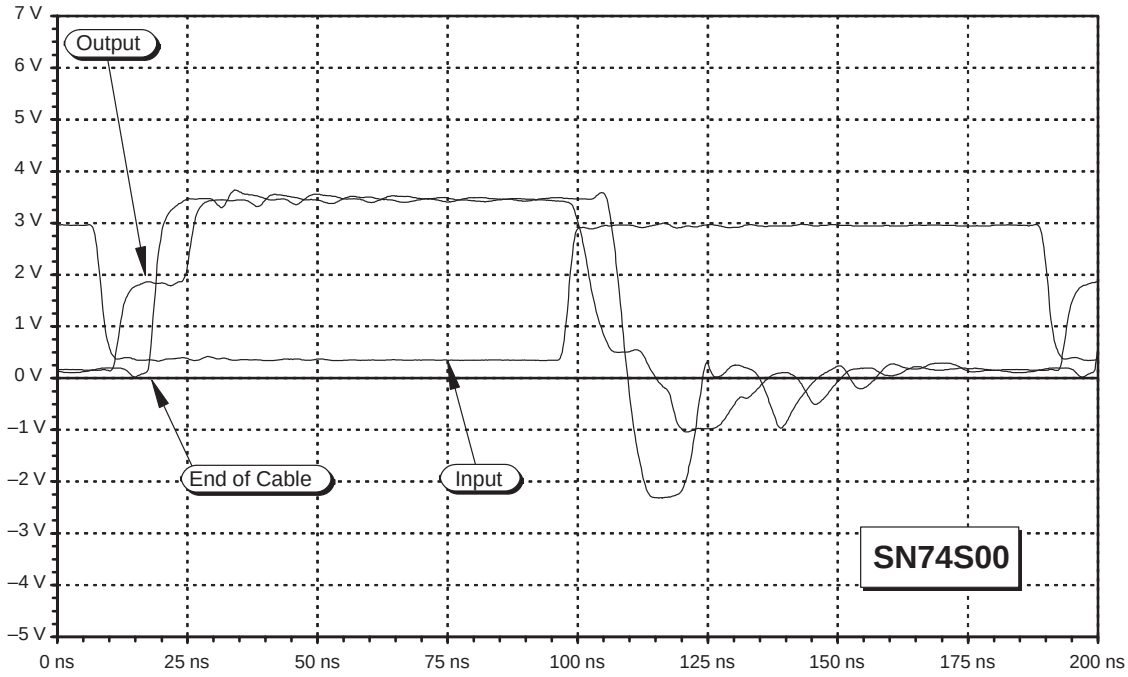

Figure 54. Output Waveforms of the SN74S00

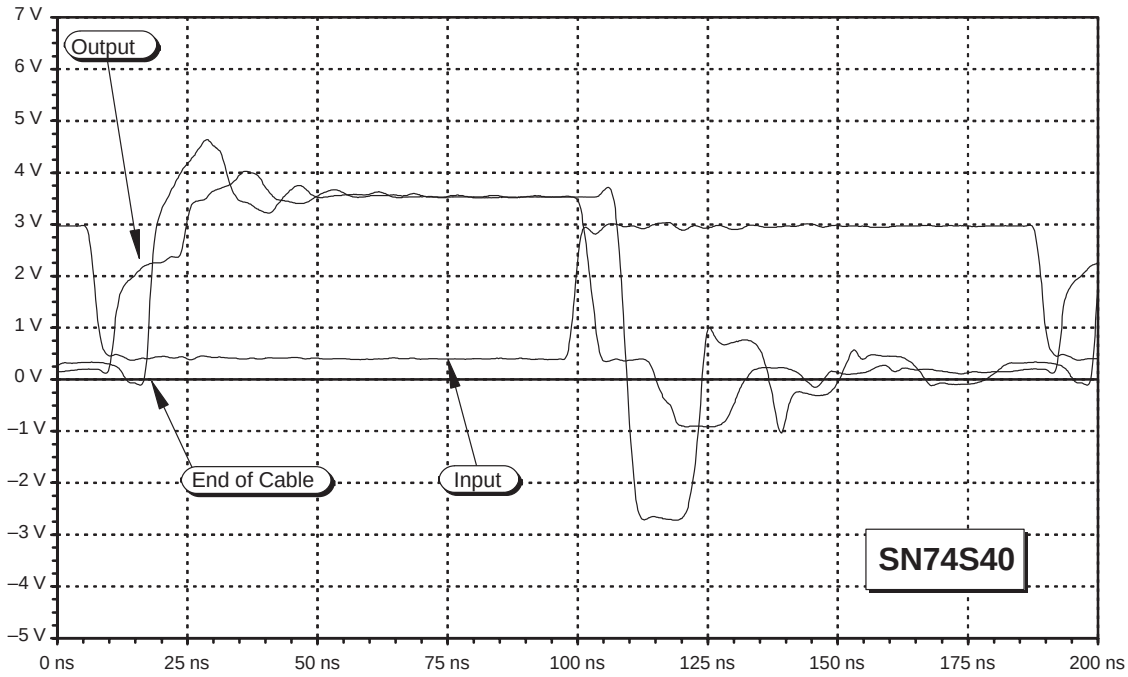

Figure 55. Output Waveforms of the SN74S40

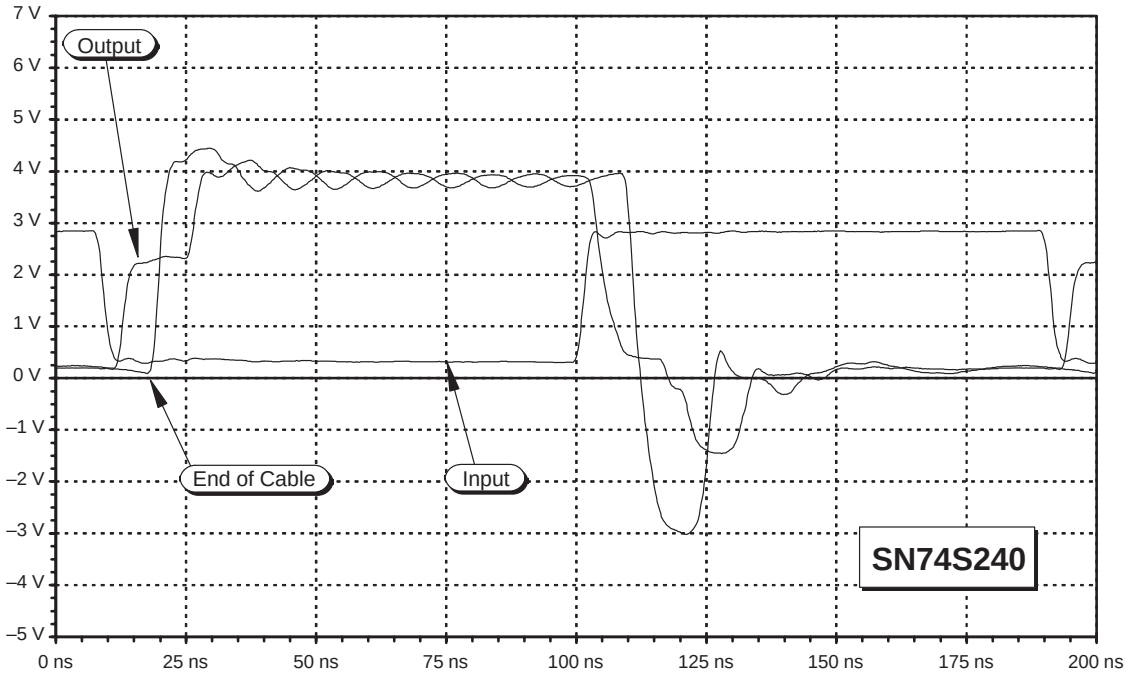

Figure 56. Output Waveforms of the SN74S240

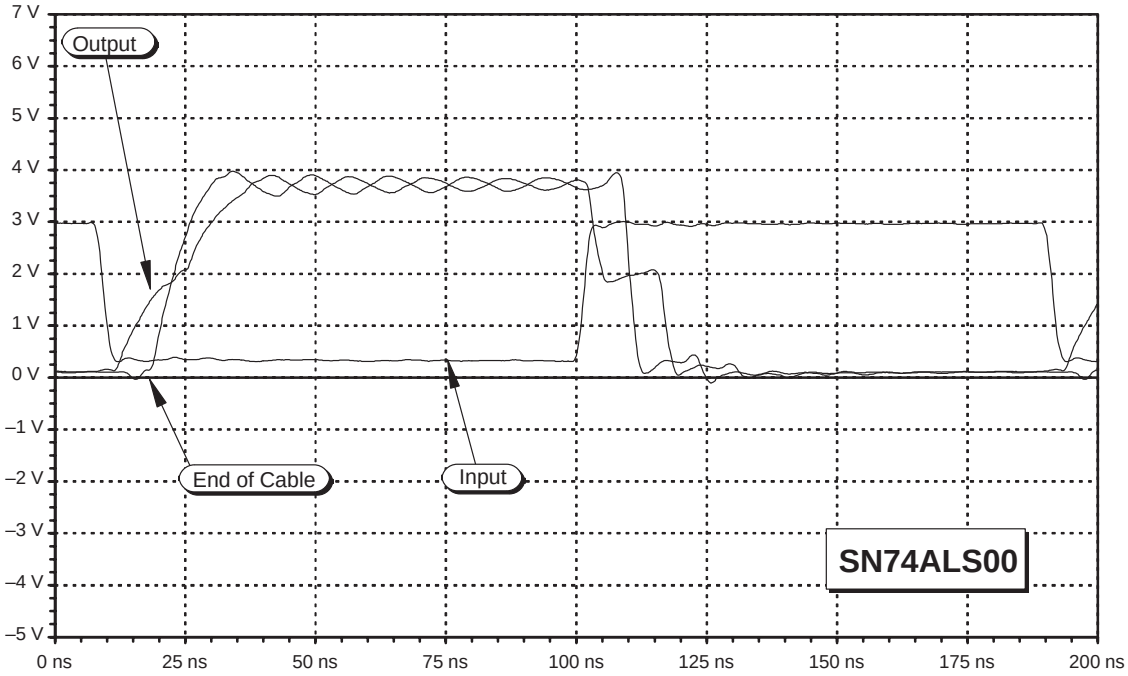

Figure 57. Output Waveforms of the SN74ALS00

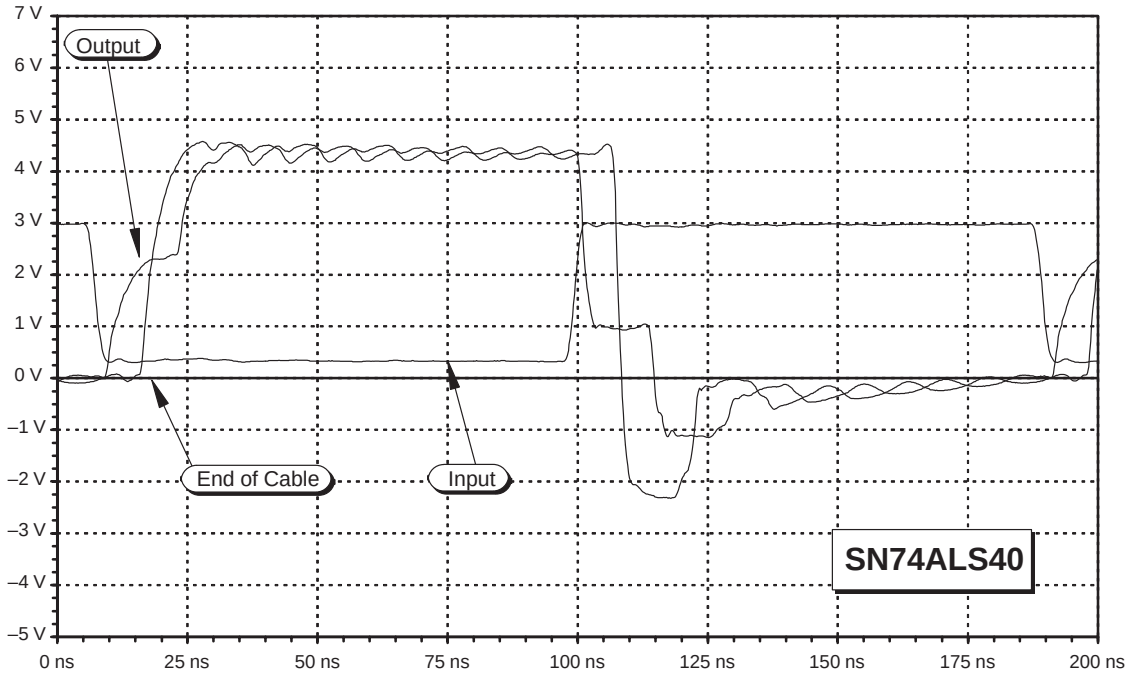

Figure 58. Output Waveforms of the SN74ALS40

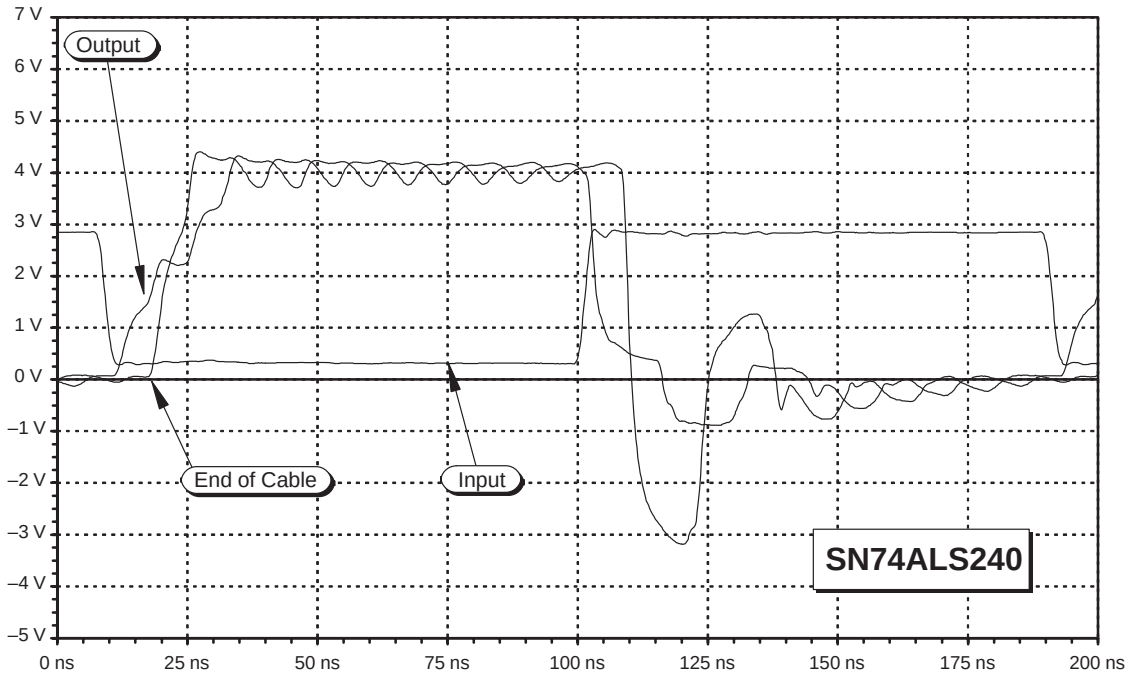

Figure 59. Output Waveforms of the SN74ALS240

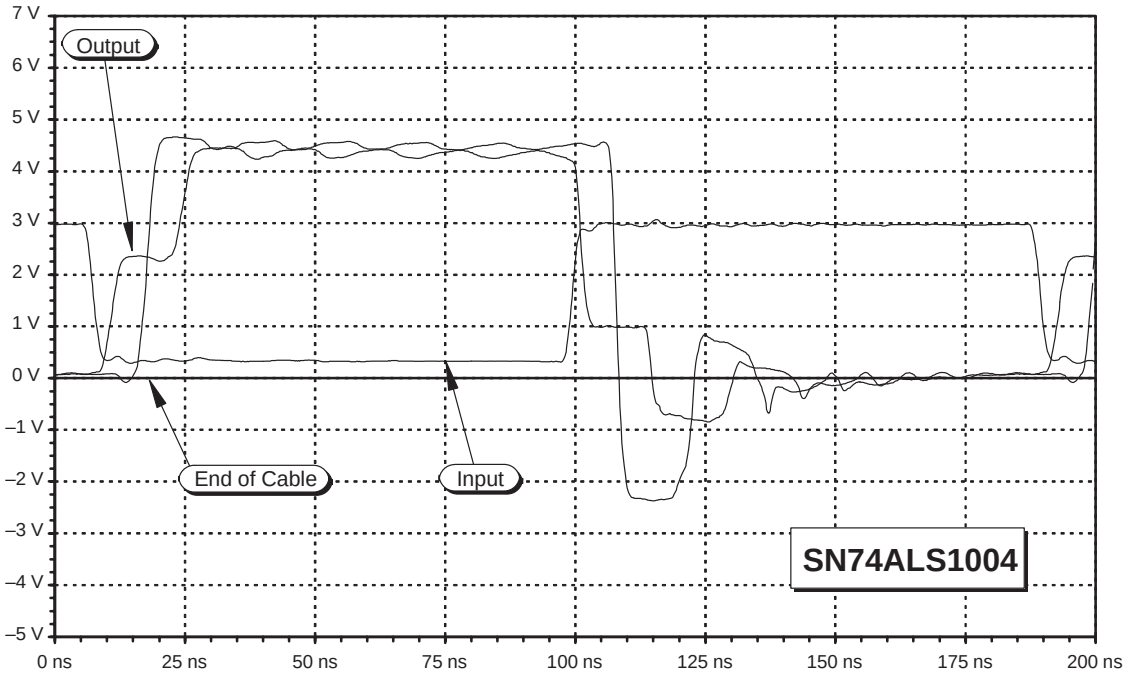

Figure 60. Output Waveforms of the SN74ALS1004

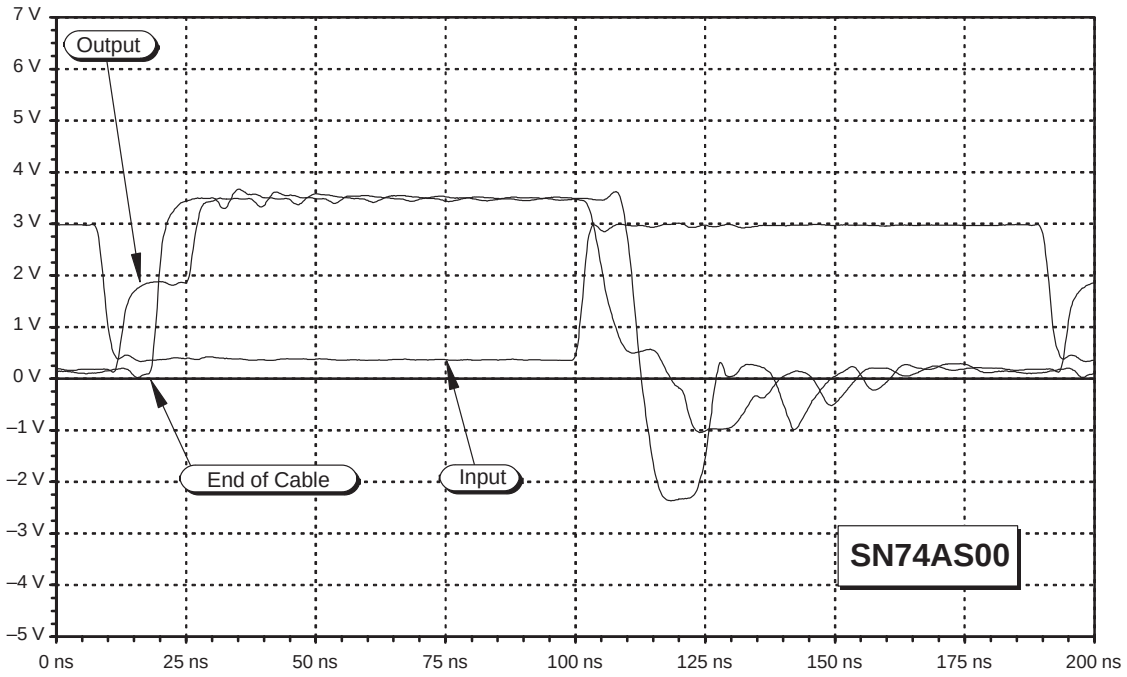

Figure 61. Output Waveforms of the SN74AS00

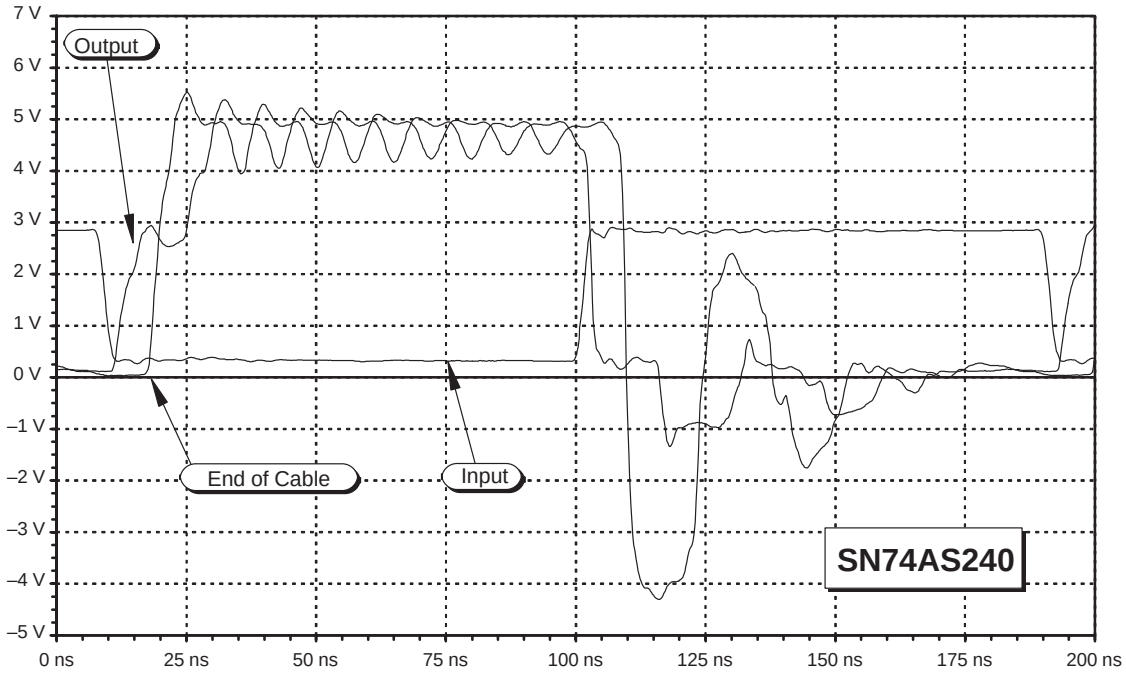

Figure 62. Output Waveforms of the SN74AS240

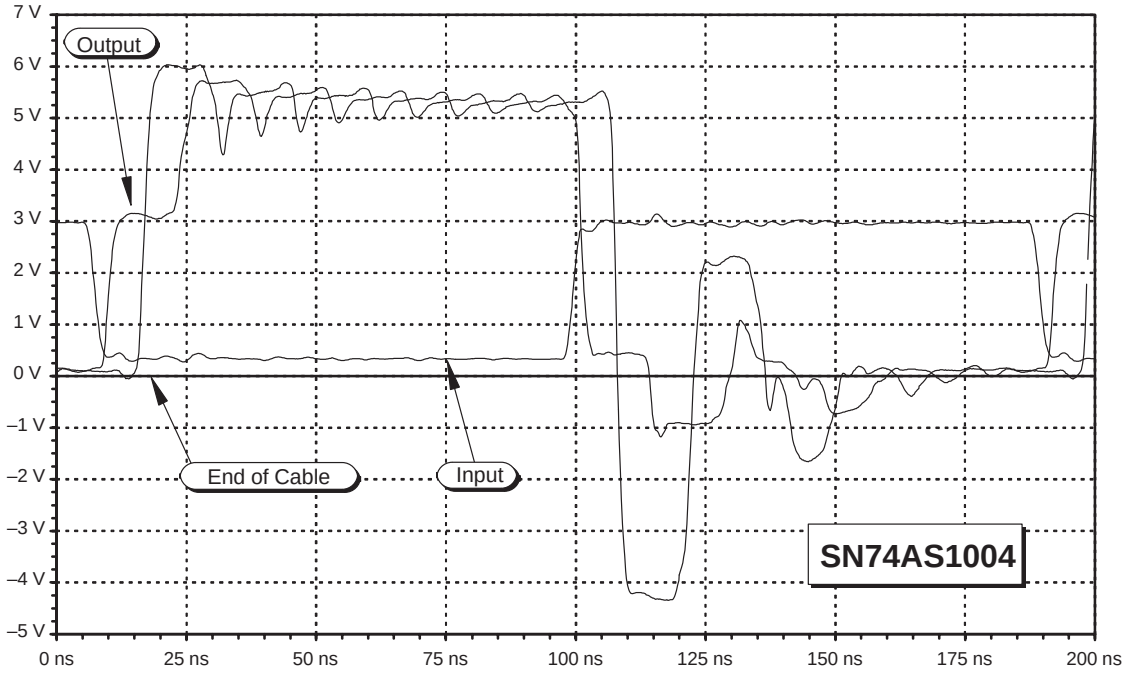

Figure 63. Output Waveforms of the SN74AS1004

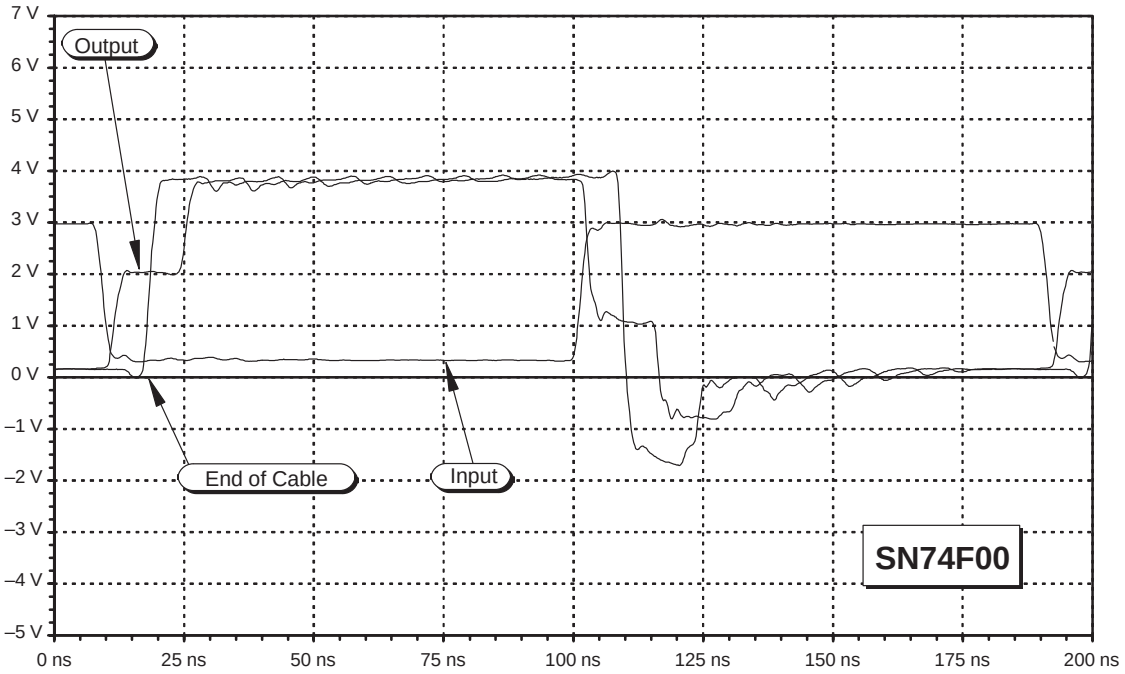

Figure 64. Output Waveforms of the SN74F00

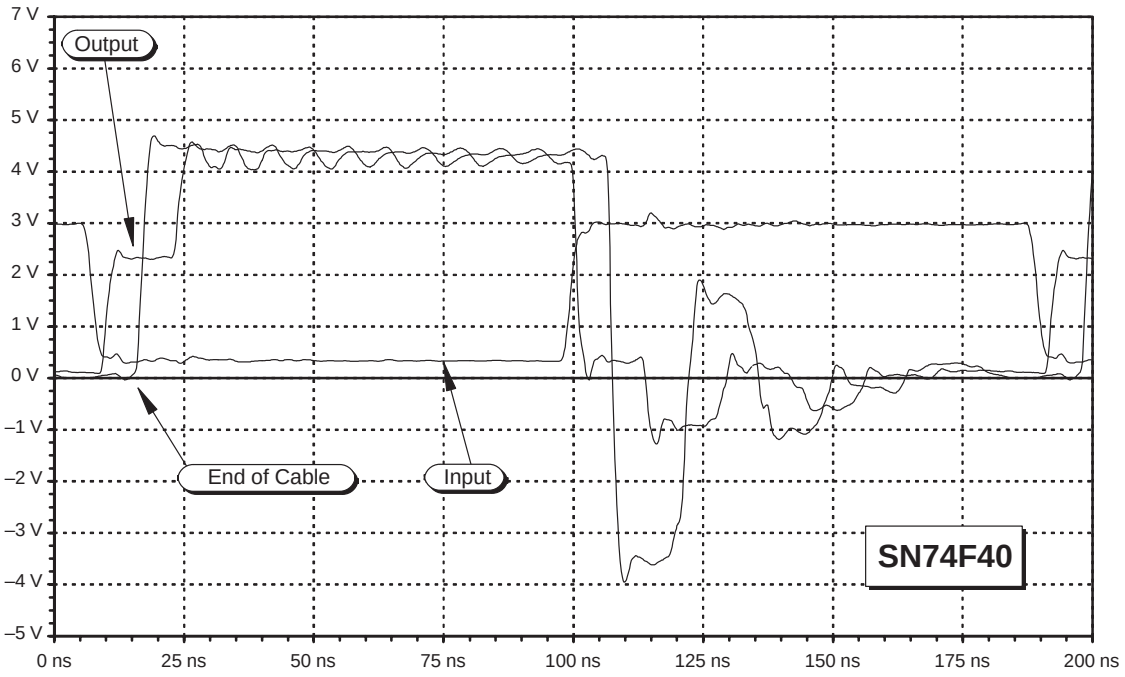

Figure 65. Output Waveforms of the SN74F40

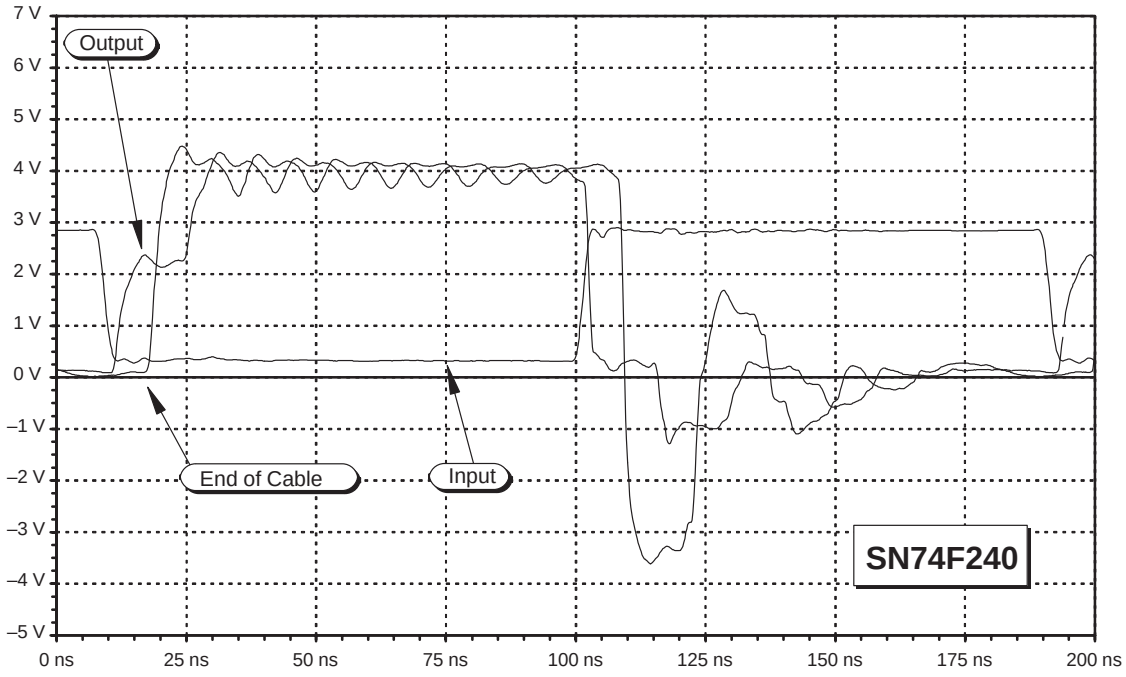

Figure 66. Output Waveforms of the SN74F240

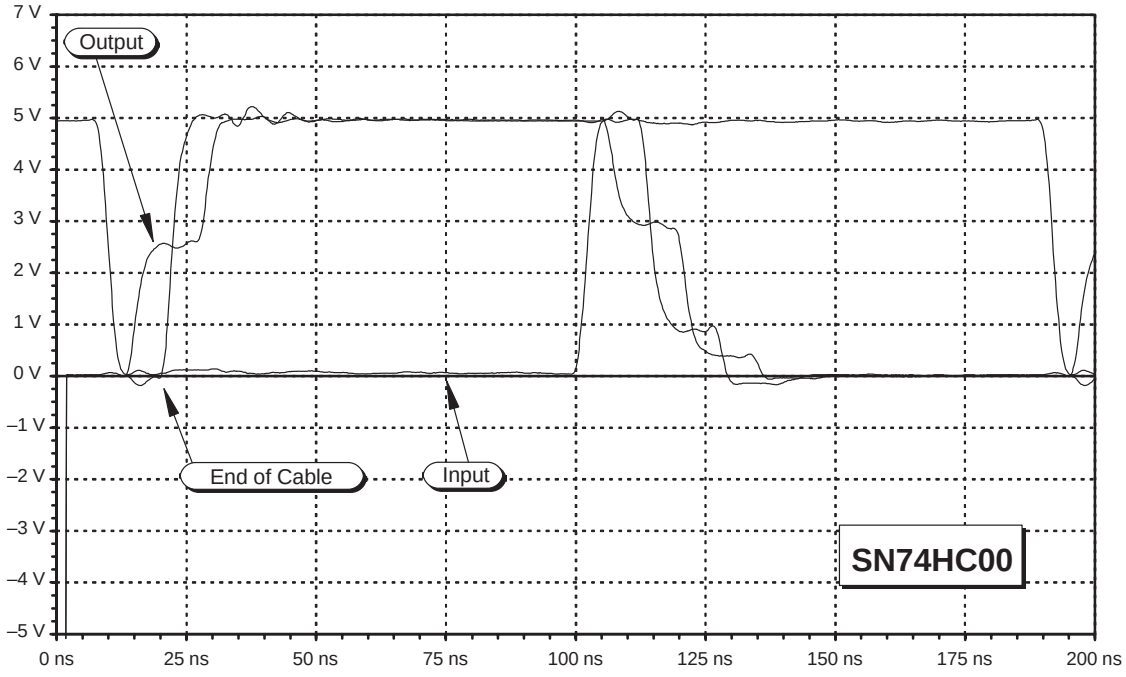

Figure 67. Output Waveforms of the SN74HC00

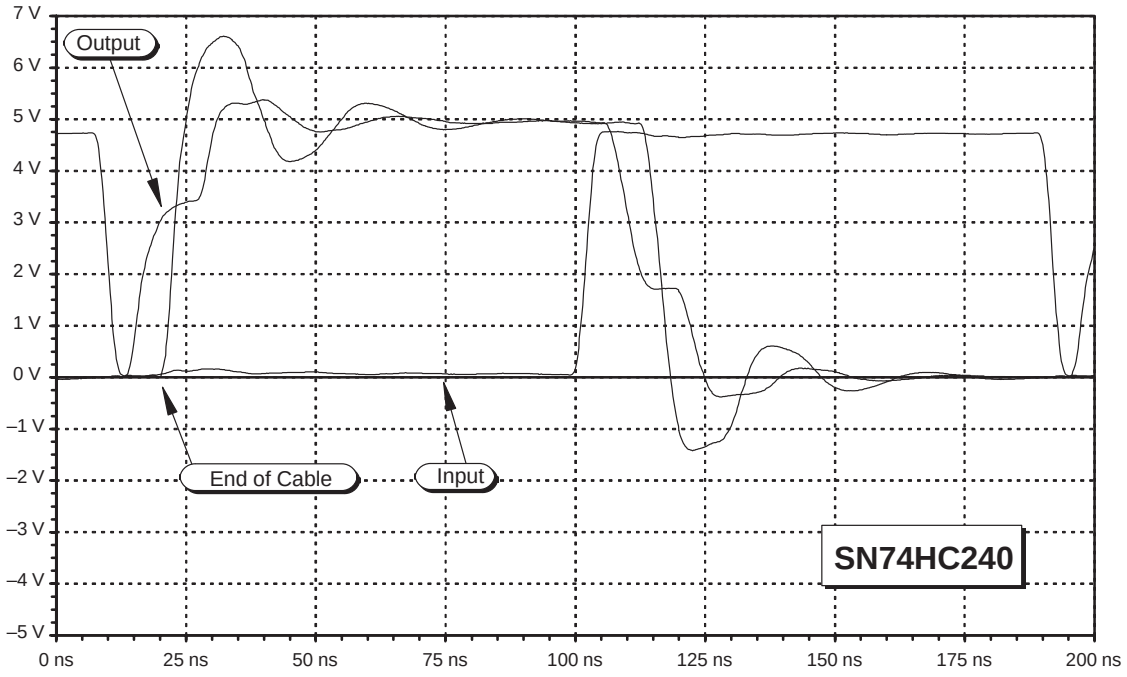

Figure 68. Output Waveforms of the SN74HC240

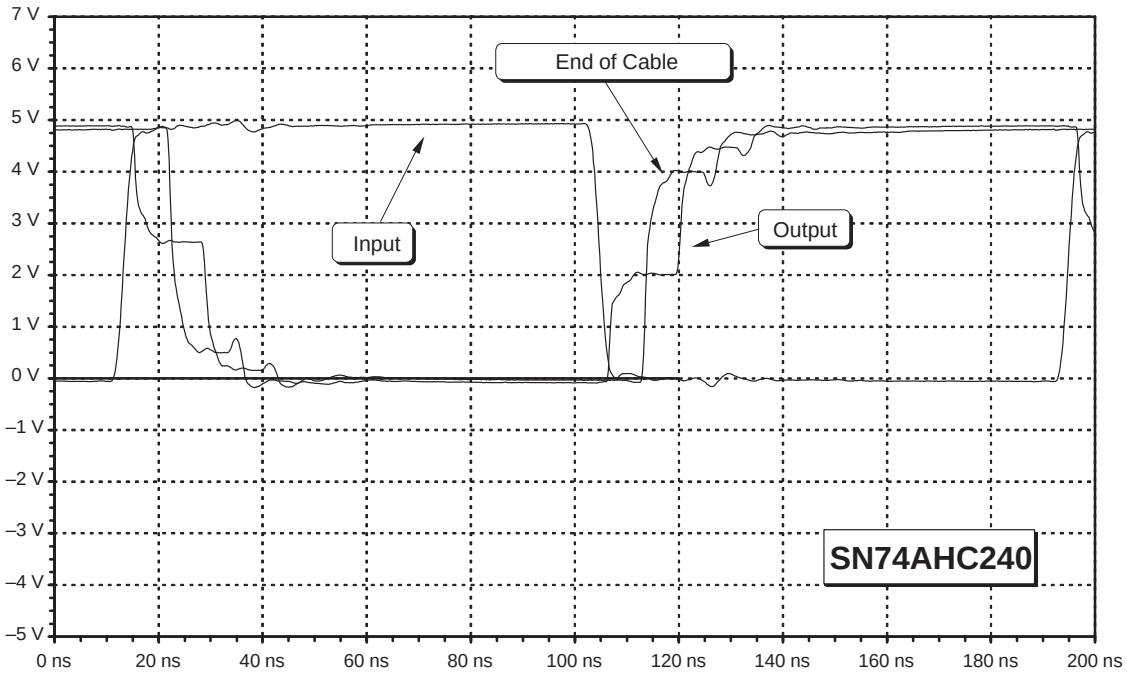

Figure 69. Output Waveforms of the SN74AHC240

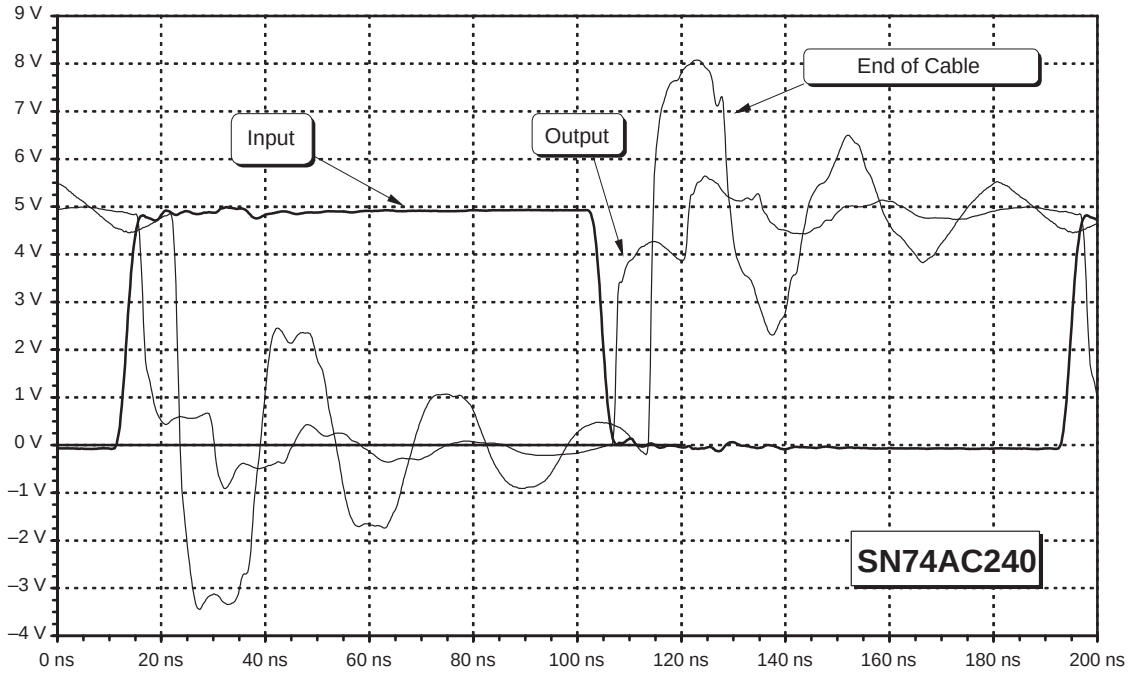

Figure 70. Output Waveforms of the SN74AC240

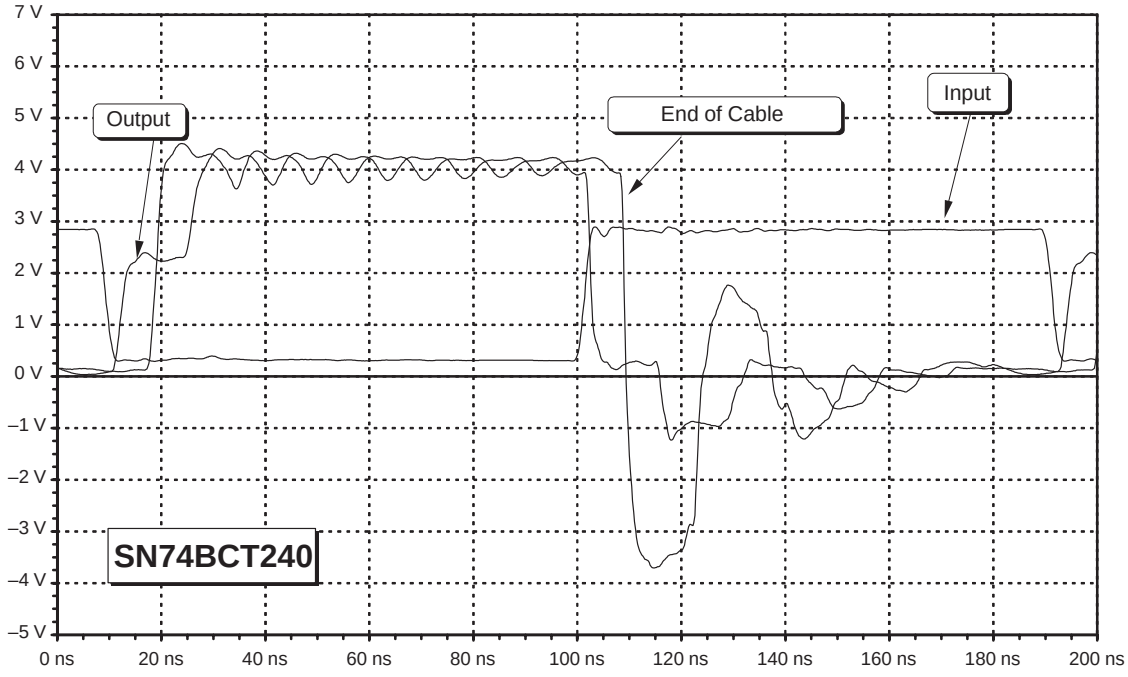

Figure 71. Output Waveforms of the SN74BCT240

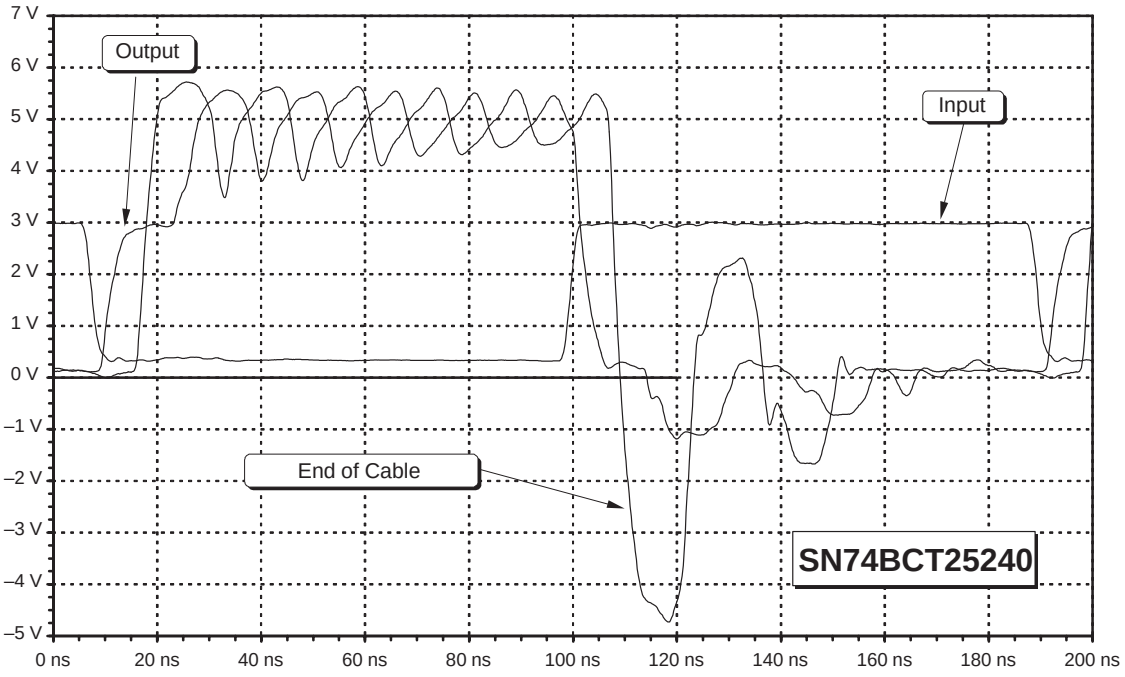

Figure 72. Output Waveforms of the SN74BCT25240

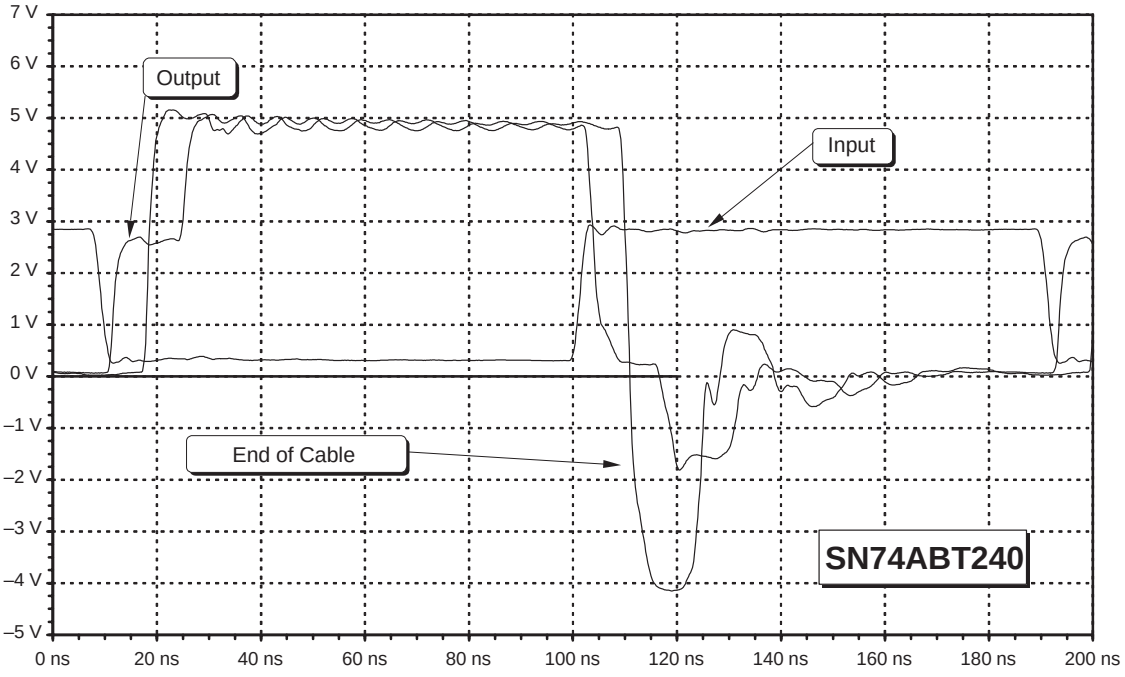

Figure 73. Output Waveforms of the SN74ABT240

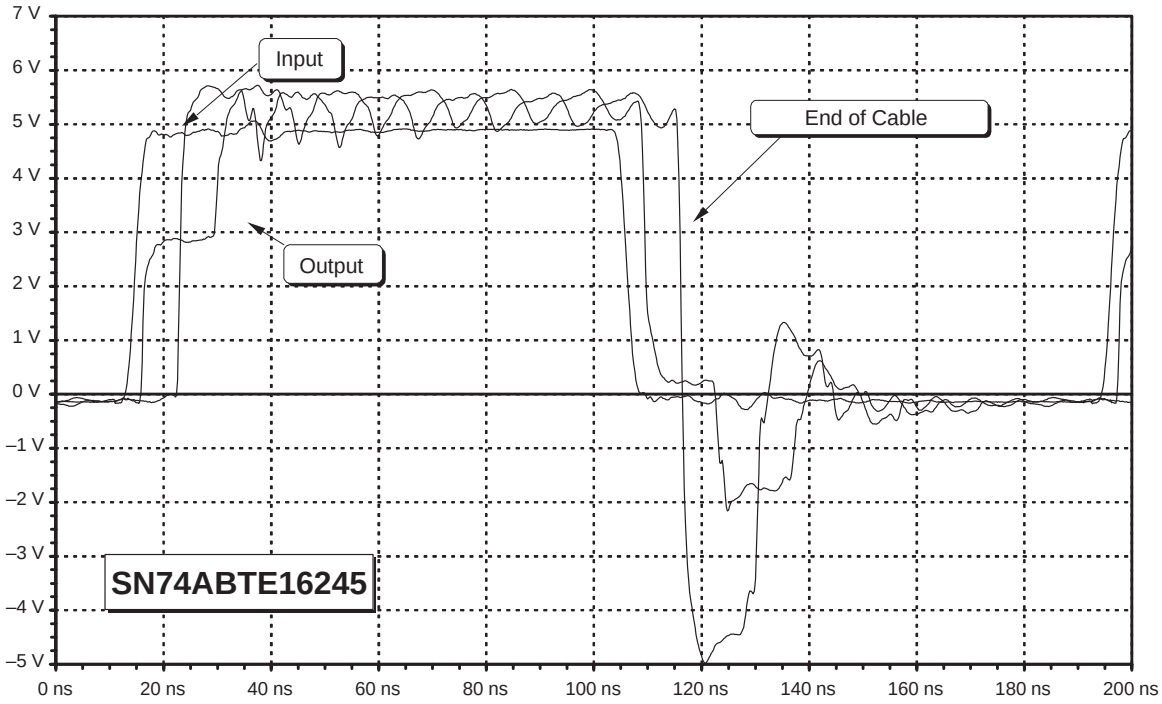

Figure 74. Output Waveforms of the SN74ABTE16245

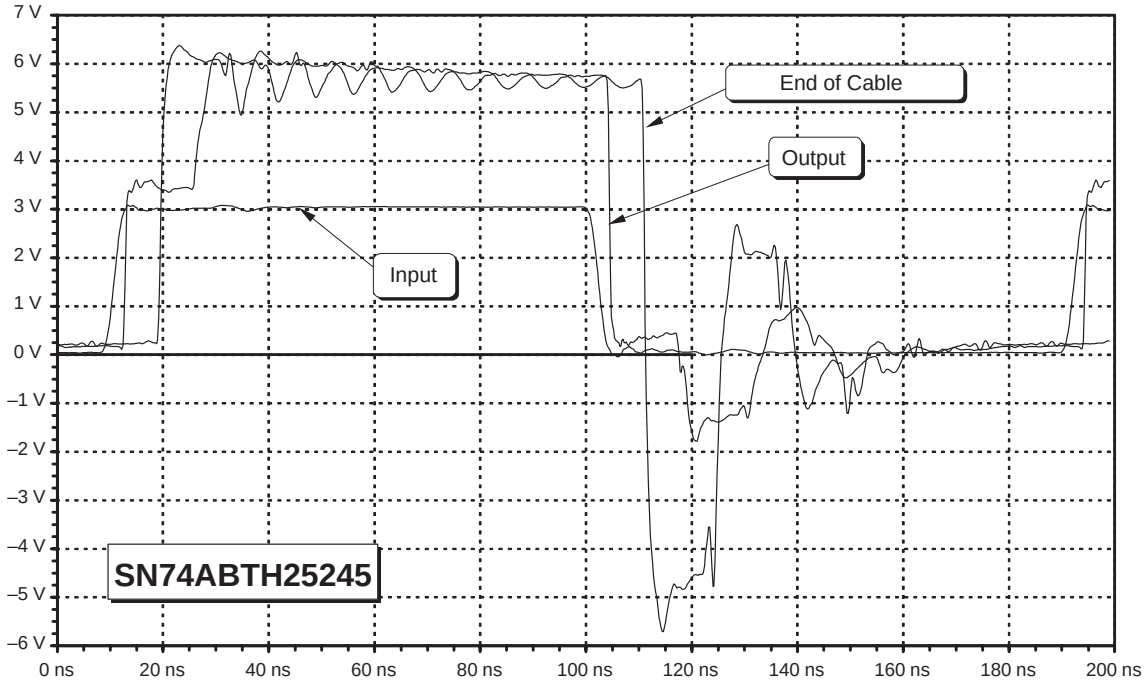

Figure 75. Output Waveforms of the SN74ABTH25245

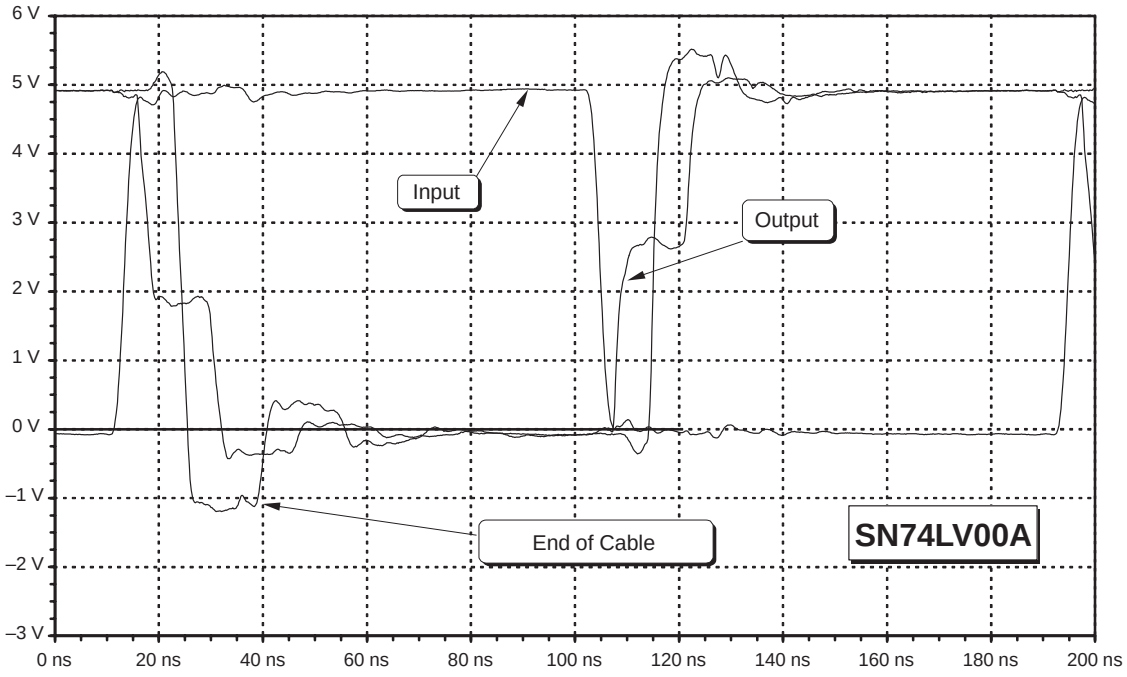

Figure 76. Output Waveforms of the SN74LV00A

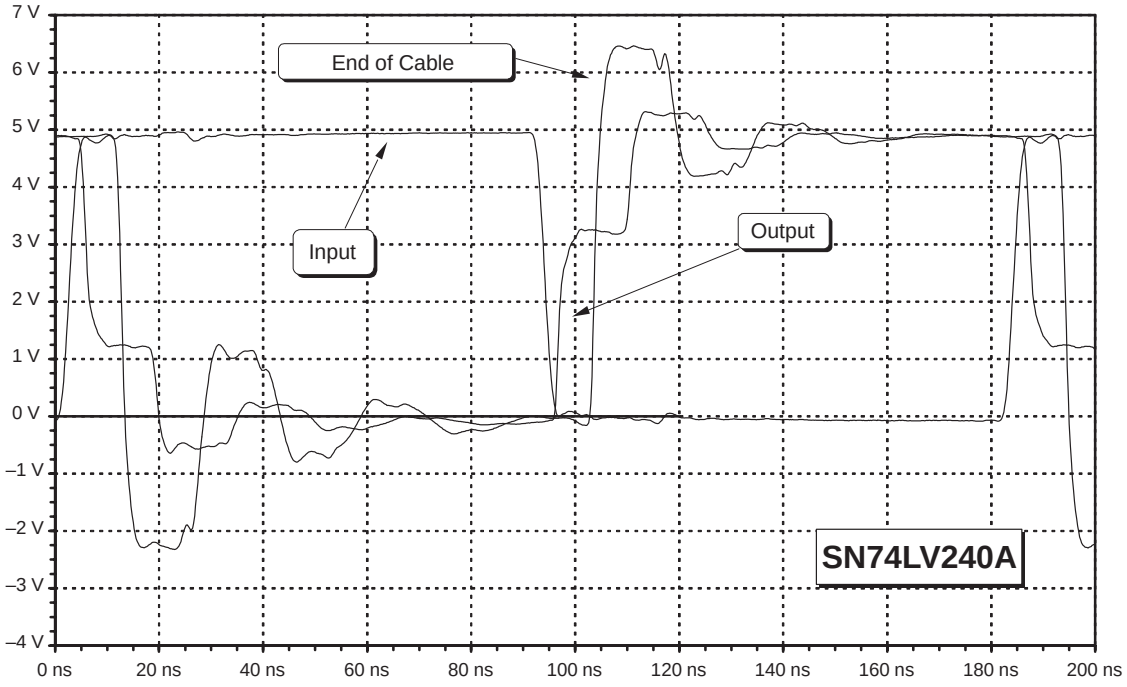

Figure 77. Output Waveforms of the SN74LV240A

6 Abbreviations and Glossary

A

SN74AC	Advanced CMOS
SN74ABT	Advanced BiCMOS Technology
SN74AHC	Advanced High-Speed CMOS
SN74ALS	Advanced Low-Power Schottky
SN74AS	Advanced Schottky

B

SN74BCT	BiCMOS Technology
BiCMOS	Combination of Bipolar and CMOS process (CMOS input structure, bipolar output structure)

G

GND	Ground

H

HC	High-speed CMOS

I

I/O	Input/Output

L

SN74LS	Low-power Schottky
SN74LV	Low-Voltage CMOS, originally designed for V_{CC} = 3.3-V, also specified at 5 V

R

R_L	Load resistor

S

SN74S Schottky

SPICE Simulation Program with Integrated Circuit Emphasis

T

TTL 5-V, Transistor-Transistor Logic

V

V_{CC} Supply voltage

7 References

7.1 Documents Published by TI

ABT Logic Advanced BiCMOS Technology, Data Book, 1998, literature number SCBD002C.

Advanced CMOS Logic, Data Book, 1996, literature number SCADE02.

Logic Selection Guide and Data Book, CD-ROM, April 1998, literature number SCBC001B.

AHC/AHCT Logic Advanced High-Speed CMOS, Data Book, 1997, literature number SCLD003A.

Design Considerations for Logic, 1997, literature number SDYA002.

Digital Design Seminar, Reference Manual, 1998, literature number SDYDE01B.

Designing With Logic, March 1997, literature number SDYA009B.

The Bergeron Method: A Graphic Method for Determining Line Reflections in Transient Phenomena, October 1996, literature number SDYA014.

Bus-Interface Devices With Output-Damping Resistors or Reduced-Drive Outputs, August 1997, literature number SCBA012A.

Live Insertion, October 1996, literature number SDYA012.

Thin Very Small-Outline Package (TVSOP), March 1997, literature number SCBA009C.

Low-Voltage Logic Families, April 1997, literature number SCVAE01A.

Bus-Hold Circuit, July 1992, literature number SDZAE15.

Electromagnetic Emission from Logic Circuits, November 1998, literature number SZZA007.

PCB Design Guidelines for Reduced EMI, November 1998, literature number SZZA009.

Input and Output Characteristics of Digital Integrated Circuits at 3.3-V Supply Voltage, literature number SZZA010.

Input and Output Characteristics of Digital Integrated Circuits at 2.5-V Supply Voltage, literature number SZZA012.

7.2 Internet Information Sources

TI Semiconductor Home Page

http://www.ti.com/sc

TI Distributors

http://www.ti.com/sc/docs/distmenu.htm

TI Logic Home Page

http://www.ti.com.sc/docs/asl/lit/lit.htm

TI Logic Literature

http://www.ti.com/sc/docs/asl/lit/lit.htm

TI Product Information and Document Search

http://www.ti.com/sc/docs/msp/download.htm

8 Acknowledgment

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