

Test Report: PMP22557

# High-Voltage Buck Converter Reference Design for E-Motorcycle BMS Applications



## Description

This non-isolated buck converter provides a fixed output of 12 V at 400 mA for BMS applications. It operates over an input voltage range of 50 V<sub>DC</sub>–150 V<sub>DC</sub> after a start-up greater than 40 V. Operating in Discontinuous Conduction Mode (DCM), this converter utilizes the UCC28730 controller, which is referenced to the switch node. It offers high efficiency and low cost in a compact form factor.

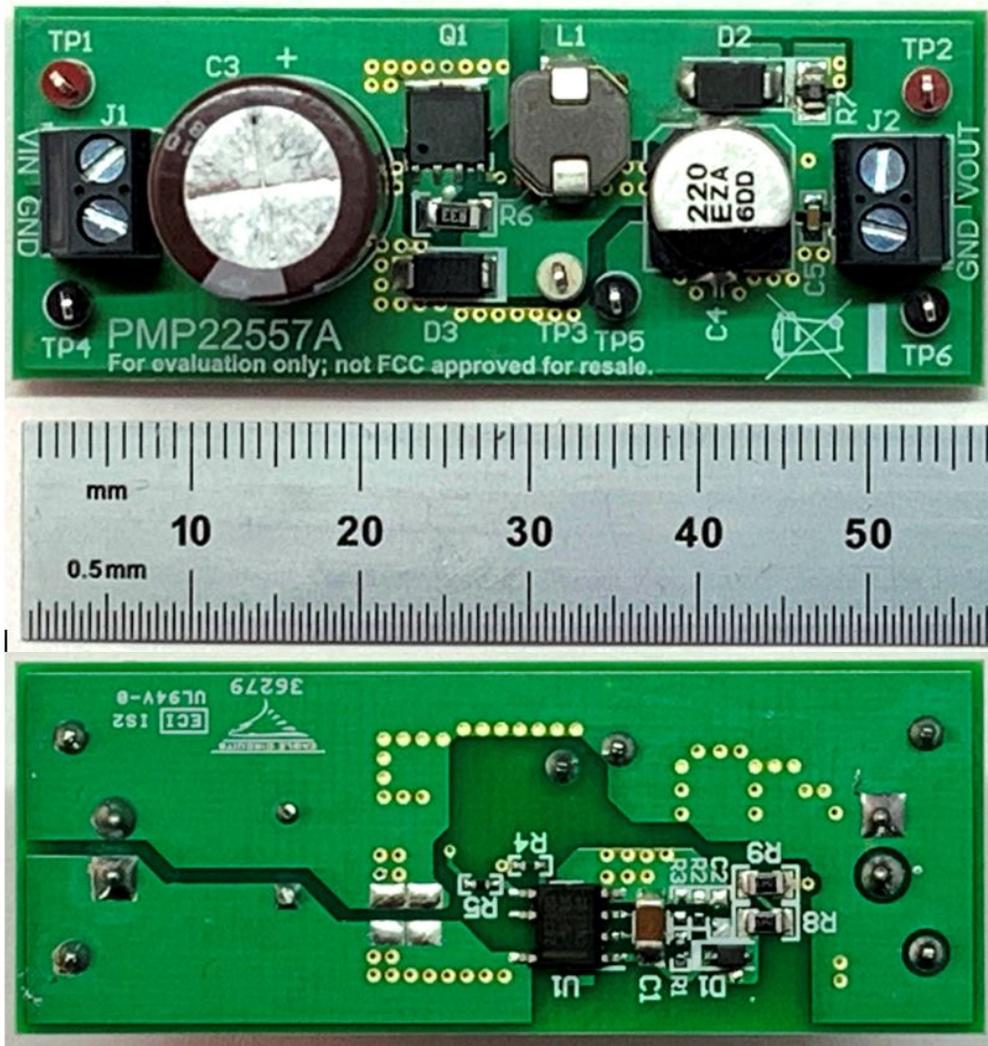


Figure 1-1. Board Photos, Top and Bottom Views

## 1 Test Prerequisites

### 1.1 Voltage and Current Requirements

**Table 1-1. Voltage and Current Requirements**

Parameter	Specifications
Input voltage range	50 V - 150 V, after > 40 V start-up
Output voltage and current	12V $\pm$ 3%, 400 mA maximum
Switching frequency	Variable, 83 kHz max
Isolation	No
Controller features	Valley switching, frequency dithering, internal 700-V start-up switch, overcurrent and overvoltage protection

### 1.2 Required Equipment

- Resistive load (resistor decade box), 5 W minimum
- Power supply, adjustable, 0 V–200 V and 0.25 A minimum
- Oscilloscope and probes
- Digital multimeter

## 2 Testing and Results

### 2.1 Thermal Images

This thermal image shows the operating temperature of the **top** side of the board with 120 V<sub>DC</sub> input and 12 V at 400-mA output at room temperature and no air flow.

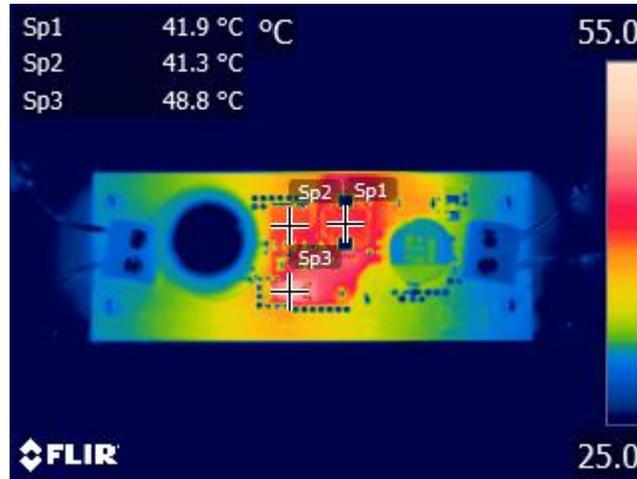


Figure 2-1. Top-Side Thermal Image, 120-V<sub>DC</sub> Input, 12 V at 400-mA Output

This thermal image shows the operating temperature of the **bottom** side of the board with 120-V<sub>DC</sub> input and 12 V at 400-mA output at room temperature and no air flow.

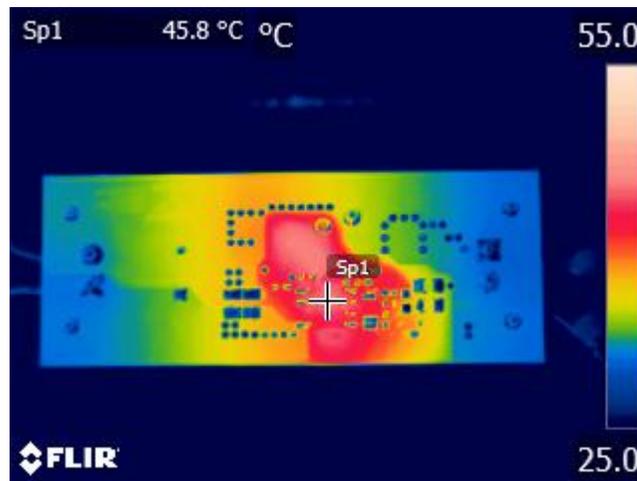


Figure 2-2. Bottom-Side Thermal Image, 120-V<sub>DC</sub> Input, 12 V at 400-mA Output

## 2.2 Efficiency and Power Dissipation Graphs

The following figure displays the efficiency and power dissipation of the converter at input voltages of 60 V<sub>DC</sub>, 90 V<sub>DC</sub>, 120 V<sub>DC</sub>, and 150 V<sub>DC</sub>.

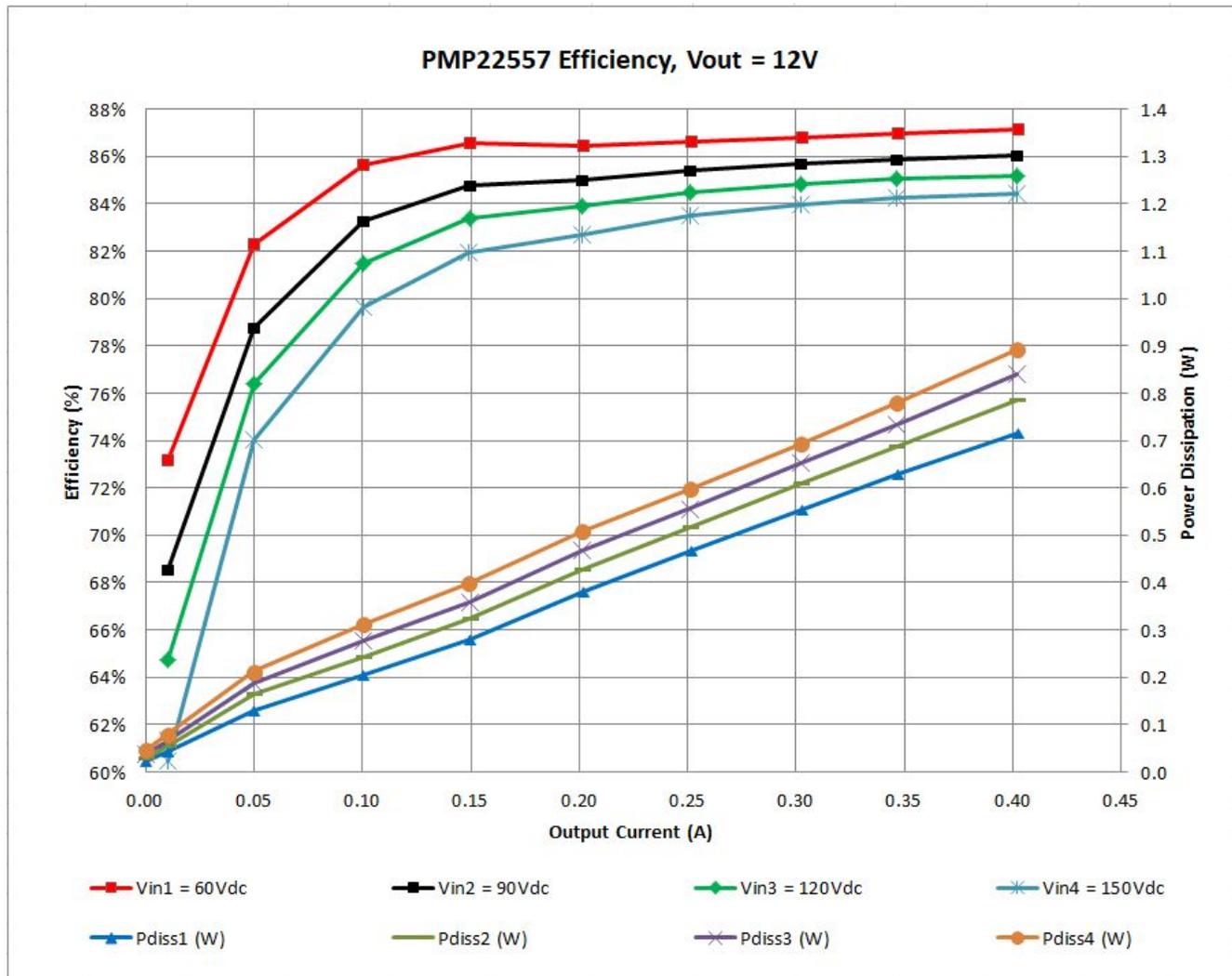


Figure 2-3. PMP22557 Efficiency, V<sub>OUT</sub> = 12 V

### 2.3 Efficiency and Power Dissipation Data

Efficiency data is shown in the following tables.

<b>PMP22557 REV B</b>						<b>Efficiency (%)</b>	<b>Power Dissipation (W)</b>
<b>V<sub>in</sub></b>	<b>I<sub>in</sub></b>	<b>V<sub>out</sub></b>	<b>I<sub>out</sub></b>	<b>P<sub>out</sub></b>	<b>P<sub>in</sub></b>	<b>V<sub>in1</sub> = 60Vdc</b>	<b>P<sub>diss1</sub> (W)</b>
60.0390	0.0004	12.215	0.000000	0.000	0.023	0.0%	0.023
60.0820	0.0028	12.145	0.010000	0.121	0.166	73.2%	0.044
60.0640	0.0123	12.150	0.050000	0.608	0.738	82.3%	0.131
60.0990	0.0236	12.097	0.100400	1.215	1.418	85.6%	0.204
60.0780	0.0347	12.082	0.149400	1.805	2.086	86.5%	0.281
60.0540	0.0469	12.069	0.201800	2.436	2.817	86.5%	0.381
60.0320	0.0584	12.064	0.251700	3.037	3.505	86.6%	0.468
60.0100	0.0700	12.047	0.302700	3.647	4.201	86.8%	0.554
60.0380	0.0801	12.051	0.347000	4.182	4.810	86.9%	0.628
60.0140	0.0926	12.038	0.402200	4.842	5.557	87.1%	0.716
<b>V<sub>in</sub></b>	<b>I<sub>in</sub></b>	<b>V<sub>out</sub></b>	<b>I<sub>out</sub></b>	<b>P<sub>out</sub></b>	<b>P<sub>in</sub></b>	<b>V<sub>in2</sub> = 90Vdc</b>	<b>P<sub>diss2</sub> (W)</b>
90.1090	0.0003	12.210	0.000000	0.000	0.029	0.0%	0.029
90.1060	0.0020	12.142	0.010000	0.121	0.177	68.5%	0.056
90.0930	0.0086	12.145	0.050000	0.607	0.771	78.8%	0.164
90.1260	0.0162	12.095	0.100400	1.214	1.458	83.3%	0.244
90.0640	0.0236	12.080	0.149300	1.804	2.127	84.8%	0.324
90.0480	0.0317	12.050	0.201400	2.427	2.855	85.0%	0.428
90.0330	0.0394	12.046	0.251300	3.027	3.545	85.4%	0.517
90.1210	0.0471	12.032	0.302300	3.637	4.246	85.7%	0.608
90.1080	0.0539	12.038	0.346500	4.171	4.859	85.9%	0.687
90.0910	0.0624	12.029	0.401900	4.834	5.619	86.0%	0.785

**Figure 2-4. Efficiency Data for V<sub>IN</sub> = 60 V, 90 V**

<b>PMP22557 REV B</b>						<b>Efficiency (%)</b>	<b>Power Dissipation (W)</b>
<b>Vin</b>	<b>Iin</b>	<b>Vout</b>	<b>Iout1</b>	<b>Pout</b>	<b>Pin</b>	<b>Vin3 = 120Vdc</b>	<b>Pdiss3 (W)</b>
120.1420	0.0003	12.203	0.000000	0.000	0.037	0.0%	0.037
120.0390	0.0016	12.158	0.010000	0.122	0.188	64.7%	0.066
120.0820	0.0066	12.124	0.049900	0.605	0.792	76.4%	0.187
120.0170	0.0124	12.095	0.100400	1.214	1.491	81.5%	0.276
120.1570	0.0180	12.076	0.149300	1.803	2.162	83.4%	0.359
120.0470	0.0241	12.050	0.201400	2.427	2.893	83.9%	0.466
120.0360	0.0298	12.042	0.251200	3.025	3.581	84.5%	0.556
120.0730	0.0357	12.032	0.302300	3.637	4.289	84.8%	0.652
120.0150	0.0408	12.033	0.346400	4.168	4.900	85.1%	0.732
120.1480	0.0472	12.026	0.401900	4.833	5.673	85.2%	0.840
<b>Vin</b>	<b>Iin</b>	<b>Vout</b>	<b>Iout1</b>	<b>Pout</b>	<b>Pin</b>	<b>Vin4 = 150Vdc</b>	<b>Pdiss4 (W)</b>
150.0120	0.0003	12.199	0.000000	0.000	0.047	0.0%	0.047
150.0600	0.0013	12.130	0.010000	0.121	0.201	60.5%	0.079
150.0520	0.0054	12.104	0.049900	0.604	0.816	74.0%	0.212
150.0910	0.0102	12.094	0.100400	1.214	1.525	79.6%	0.311
150.0820	0.0146	12.070	0.149200	1.801	2.198	81.9%	0.397
150.0720	0.0196	12.053	0.201400	2.427	2.936	82.7%	0.508
150.1160	0.0241	12.037	0.251000	3.021	3.619	83.5%	0.598
150.1070	0.0289	12.035	0.302400	3.639	4.334	84.0%	0.694
150.0460	0.0329	12.027	0.346100	4.163	4.941	84.2%	0.778
150.0890	0.0382	12.027	0.402000	4.835	5.727	84.4%	0.893

**Figure 2-5. Efficiency Data for  $V_{IN} = 120\text{ V}, 150\text{ V}$**

## 2.4 Voltage Regulation

The following graph displays the measured output voltage at input voltages of 50 V<sub>DC</sub> and 150 V<sub>DC</sub>.

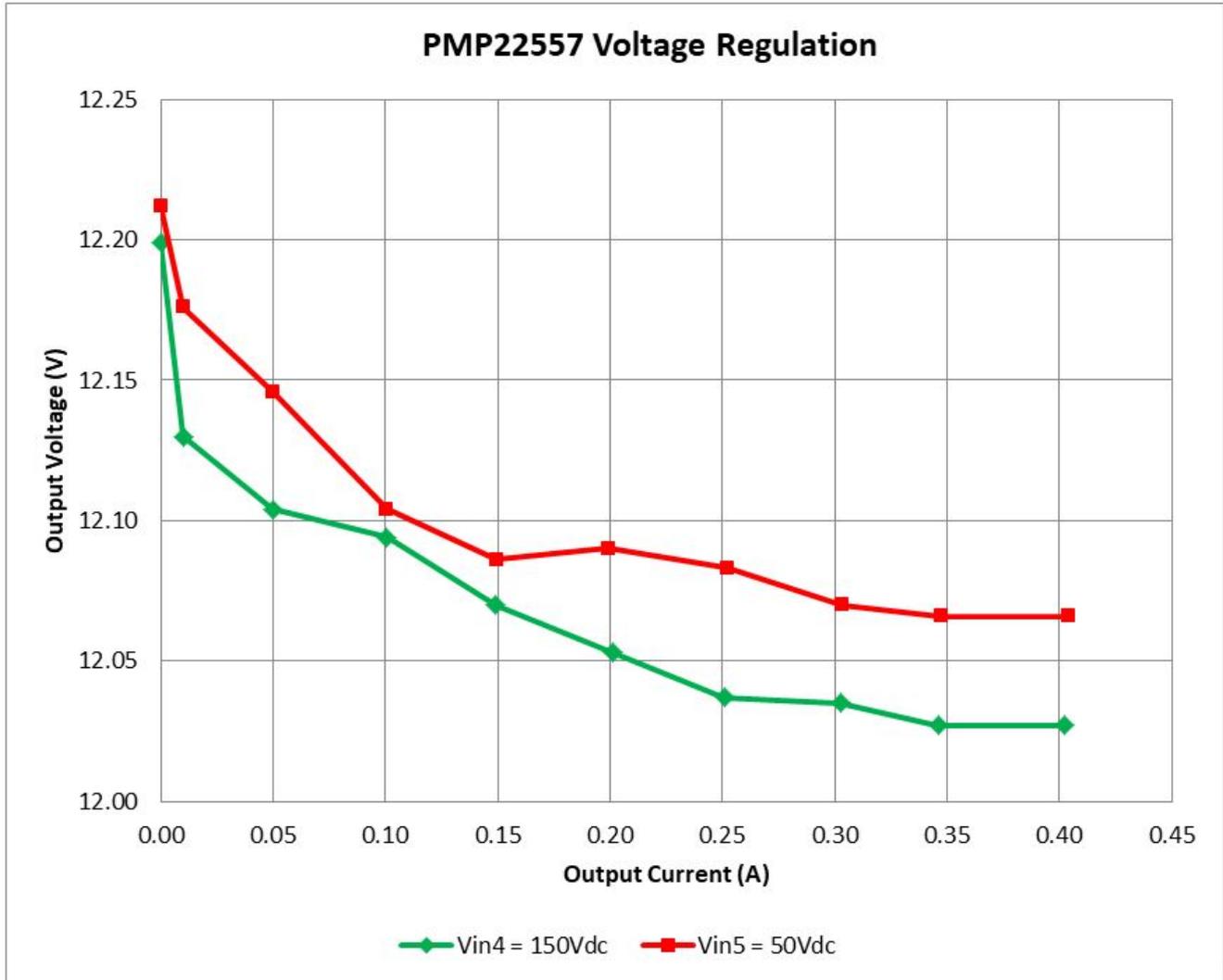


Figure 2-6. PMP22557 Voltage Regulation

### 3 Waveforms

#### 3.1 Start-up

The following image shows the output voltage start-up waveform (RED) after the application of 60-V input (BLUE) with the 12-V output loaded to 400 mA.



Figure 3-1. Output Voltage Start-up Waveform ( $V_{IN}$ : 10 V/div,  $V_{OUT}$ : 5 V/div, 50 ms/div)

The following image shows the output voltage start-up waveform (RED) after the application of 60-V input (BLUE) with the 12-V output loaded to 0 mA.

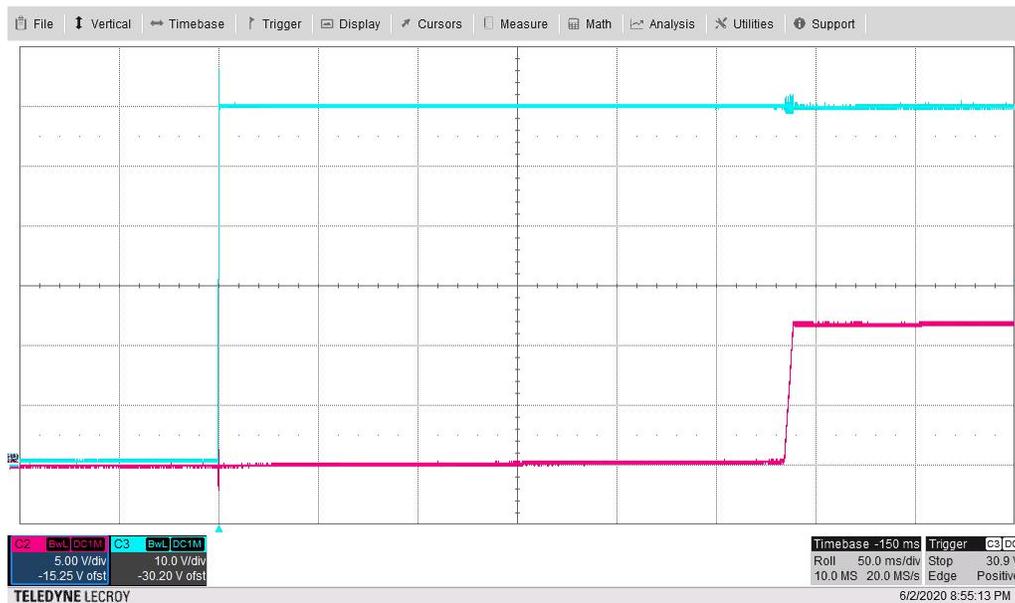


Figure 3-2. Output Voltage Start-up Waveform ( $V_{IN}$ : 10 V/div,  $V_{OUT}$ : 5 V/div, 50 ms/div)

The following image shows the output voltage start-up waveform (RED) after the application of 150-V input (BLUE) with the 12-V output loaded to 400 mA.

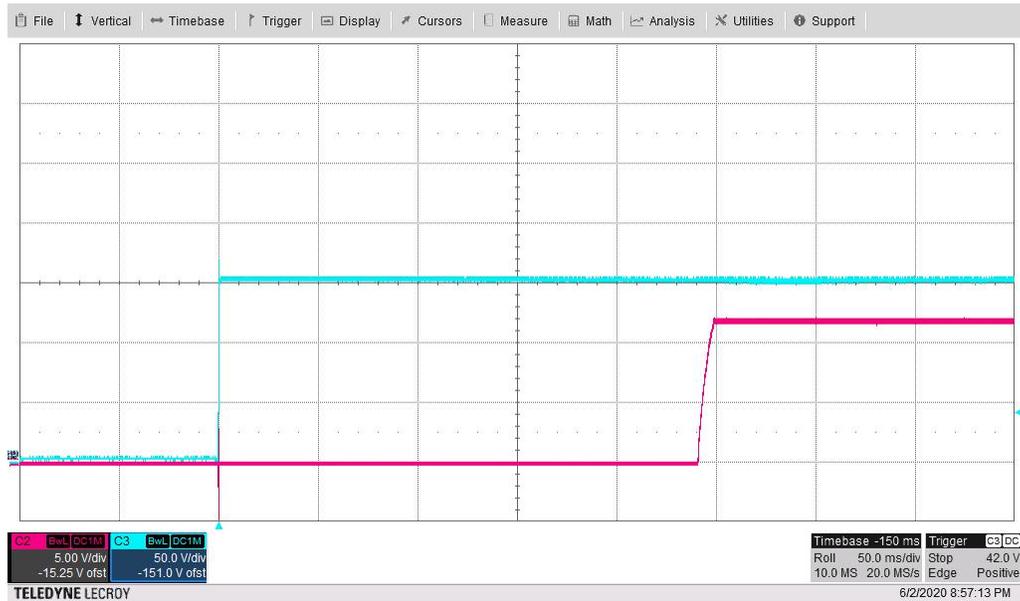


Figure 3-3. Output Voltage Start-up Waveform ( $V_{IN}$ : 50 V/div,  $V_{OUT}$ : 5V/div, 50 ms/div)

The following image shows the output voltage start-up waveform (RED) after the application of 150-V input (BLUE) with the 12-V output loaded to 0 mA.

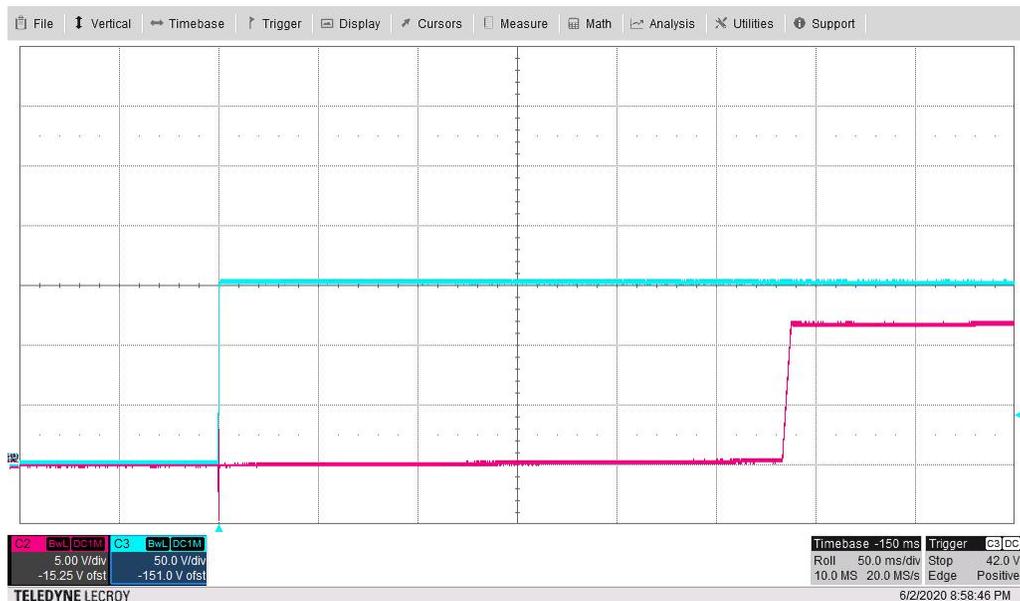
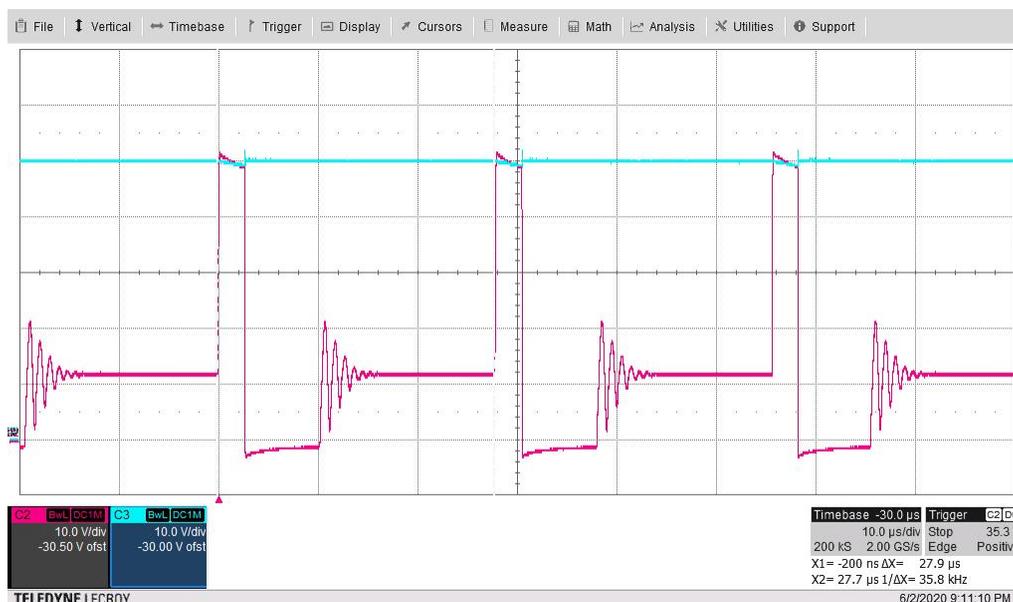


Figure 3-4. Output Voltage Start-up Waveform ( $V_{IN}$ : 50 V/div,  $V_{OUT}$ : 5 V/div, 50 ms/div)

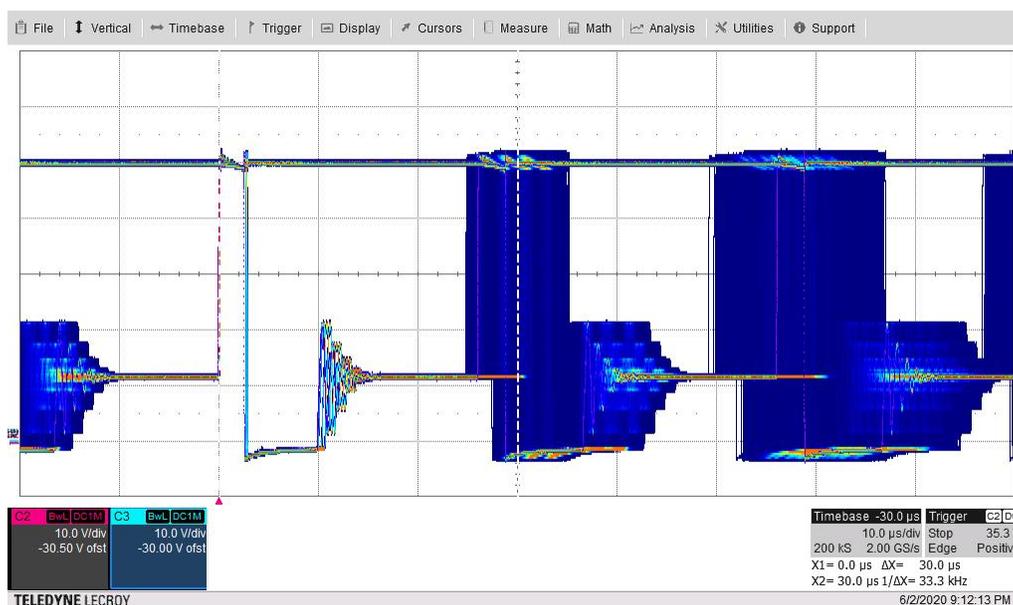
### 3.2 Switch Node

The following image shows the FET switch node voltage (RED) at TP3 and the input voltage (BLUE). The input voltage is 50 V and the 12-V output is loaded to 400 mA.



**Figure 3-5. FET Switch Node Voltage ( $V_{\text{snode}}$ : 10 V/div,  $V_{\text{IN}}$ : 10 V/div, 10  $\mu\text{s}/\text{div}$ )**

The following image (scope persistence on) shows the FET switch node voltage (RED) and the input voltage (BLUE). The input voltage is 50 V and the 12-V output is loaded to 400 mA. This shows the effects of frequency dithering and valley switching on the switch node waveform.



**Figure 3-6. FET Switch Node Voltage ( $V_{\text{snode}}$ : 10 V/div,  $V_{\text{IN}}$ : 10 V/div, 10  $\mu\text{s}/\text{div}$ )**

The following image shows the FET switch node voltage (RED) at TP3 and the input voltage (BLUE). The input voltage is 50 V and the 12-V output is loaded to 10 mA.

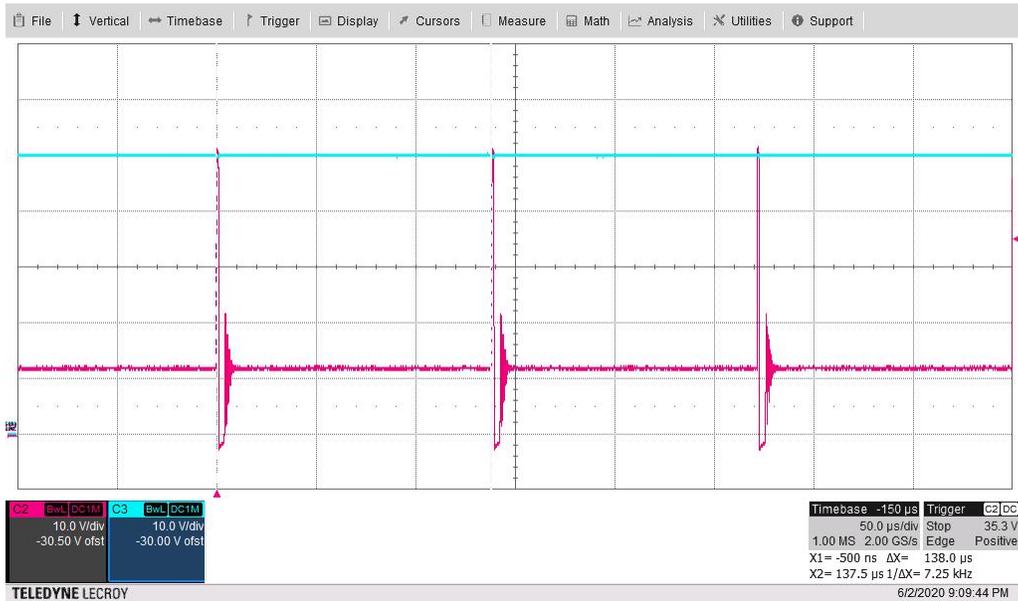


Figure 3-7. FET Switch Node Voltage ( $V_{\text{snode}}$ : 10 V/div,  $V_{\text{IN}}$ : 10 V/div, 50  $\mu\text{s}/\text{div}$ )

The following image shows the FET switch node voltage (RED) at TP3 and the input voltage (BLUE). The input voltage is 150 V and the 12-V output is loaded to 400 mA.

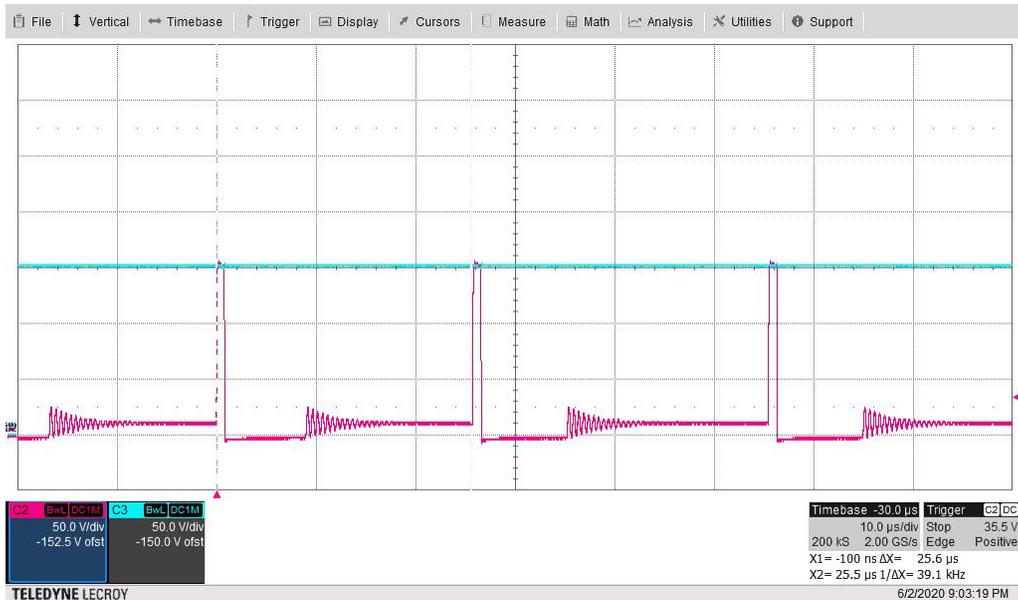


Figure 3-8. FET Switch Node Voltage ( $V_{\text{snode}}$ : 50 V/div,  $V_{\text{IN}}$ : 50 V/div, 10  $\mu\text{s}/\text{div}$ )

The following image (scope persistence on) shows the FET switch node voltage (RED) at TP3 and the input voltage (BLUE). The input voltage is 150 V and the 12-V output is loaded to 400 mA. This shows the effects of frequency dithering and valley switching on the switch node waveform.

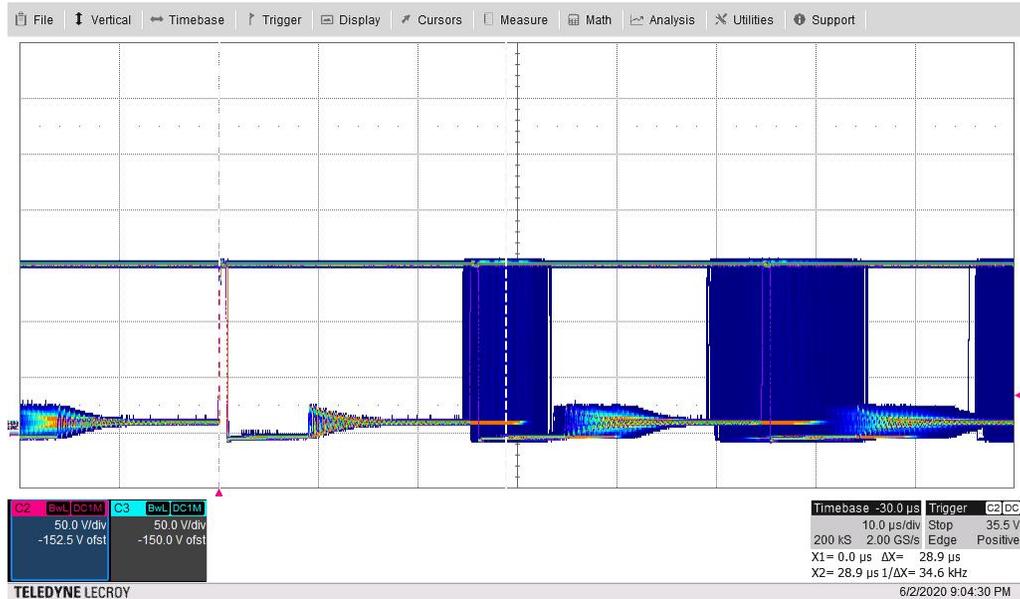


Figure 3-9. FET Switch Node Voltage (Vsnode: 50 V/div,  $V_{IN}$ : 50 V/div, 10  $\mu$ s/div)

The following image shows the FET switch node voltage (RED) at TP3 and the input voltage (BLUE). The input voltage is 150 V and the 12-V output is loaded to 10 mA.



Figure 3-10. FET Switch Node Voltage (Vsnode: 50 V/div,  $V_{IN}$ : 50 V/div, 50  $\mu$ s/div)

The following image shows the switching voltages on each side of C1. The waveforms show the switch node voltage at TP3 (RED) and D1 cathode voltage (BLUE). The input voltage is 50 V and the 12-V output is loaded to 400 mA.

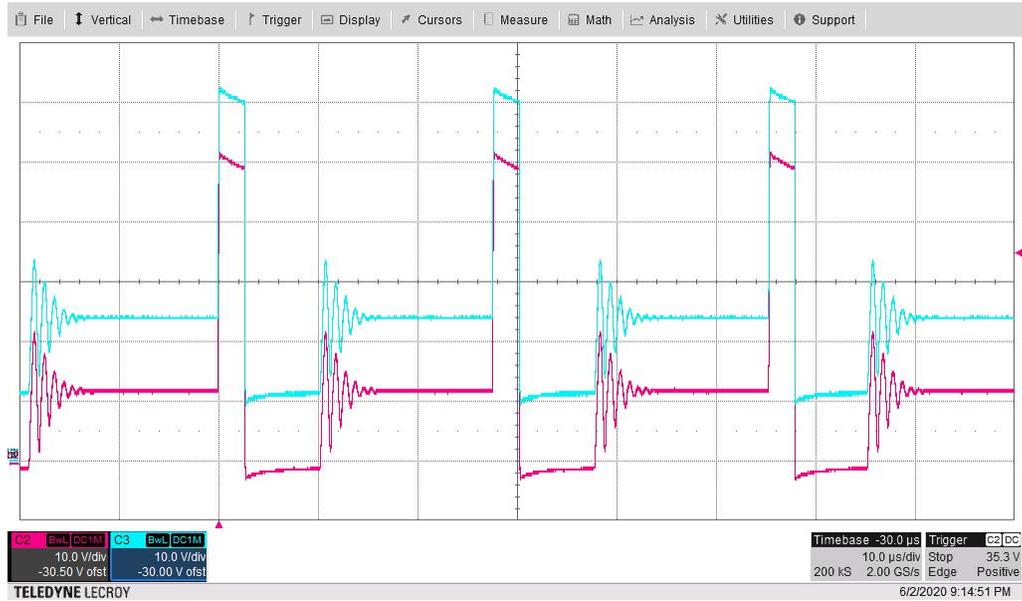


Figure 3-11. FET Switch Node Voltage (Vsnod: 10 V/div, D1-Cathode: 10 V/div, 10 μs/div)

The following image shows the switching voltages on each side of resistor divider R1/R2. The waveforms show the switch node voltage at TP3 (RED) and the voltage at R1 (side connected to D2) (BLUE). The input voltage is 50 V and the 12-V output is loaded to 400 mA.

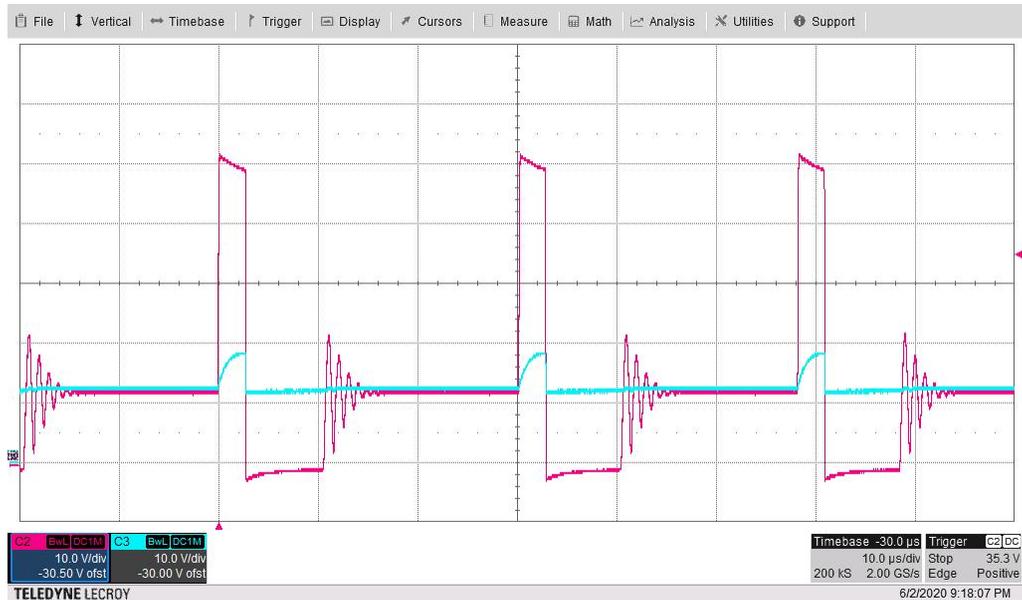
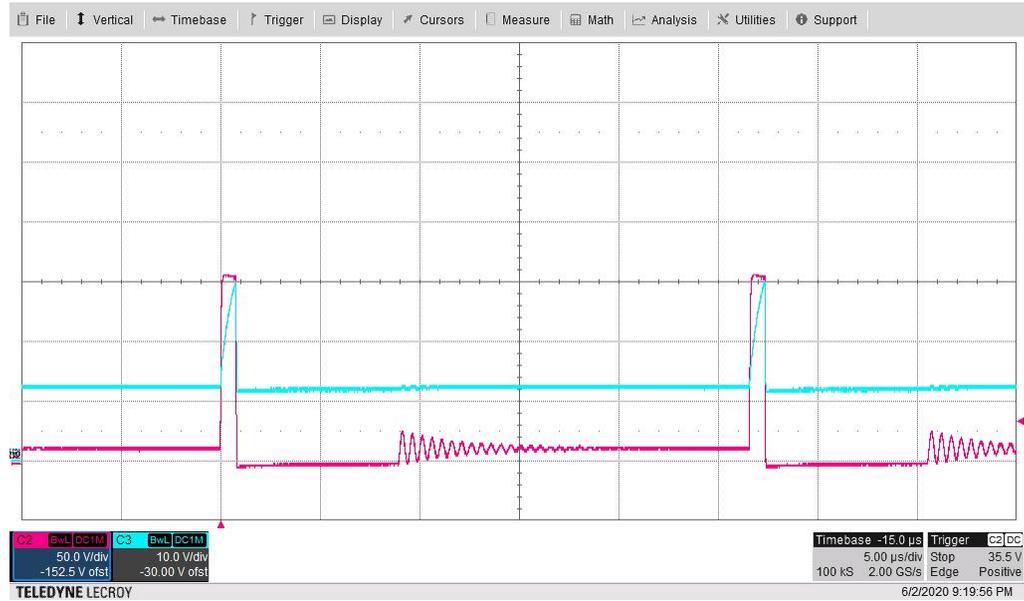


Figure 3-12. Switching Voltages (Vsnod: 10 V/div, D2-Cathode: 10 V/div, 10 μs/div)

The following image shows the switching voltages on each side of resistor divider R1/R2. The waveforms show the switch node voltage at TP3 (RED) and the voltage at R1 (side connected to D2) (BLUE). The input voltage is 150 V and the 12-V output is loaded to 400 mA.



**Figure 3-13. Switching Voltages (Vsnod: 50 V/div, D2-Cathode: 10 V/div, 5 μs/div)**

### 3.3 Output Voltage Ripple

The output ripple voltage (AC coupled) is shown in the following image. The input voltage is 50 V and the 12-V output is loaded to 400 mA.



Figure 3-14. Output Voltage Ripple (AC Coupled) ( $V_{OUT}$ : 50 mV/div, 100 µs/div)

The output ripple voltage (AC coupled and scope persistence on) is shown in the following image. The input voltage is 50 V and the 12-V output is loaded to 400 mA. This shows the effects of frequency dithering and valley switching on the switch node waveform.

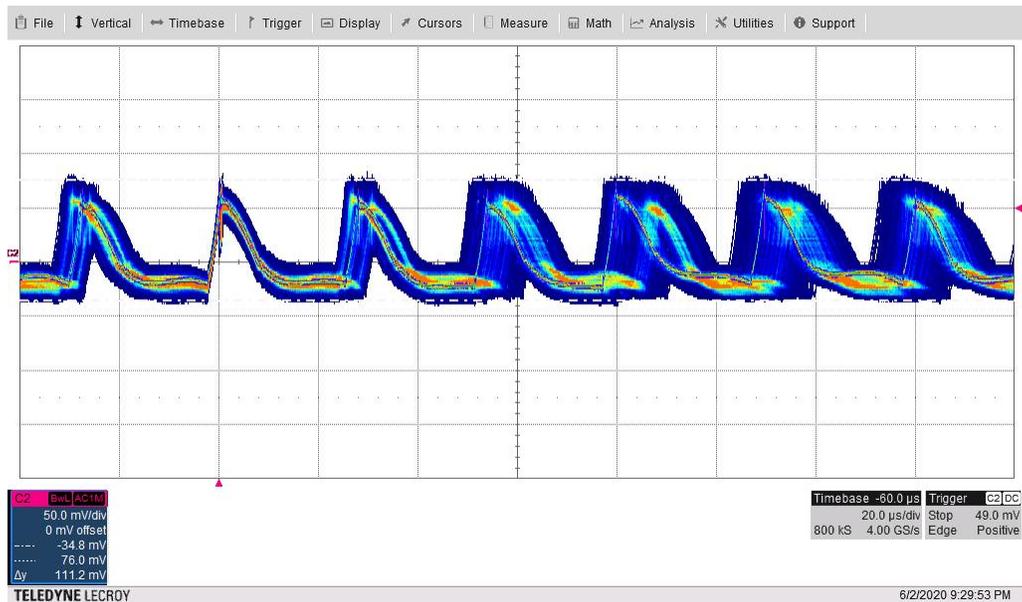
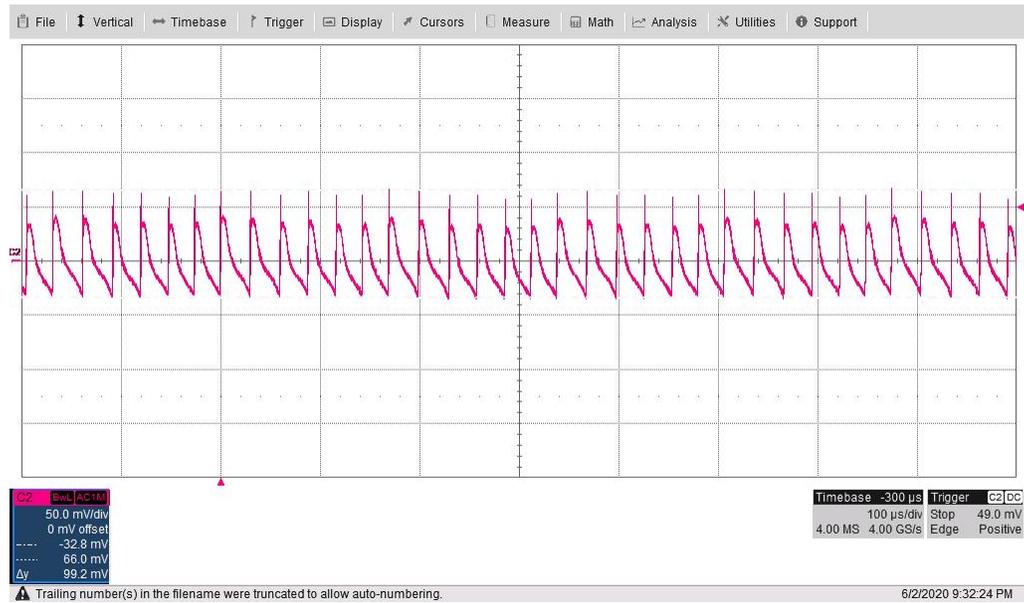


Figure 3-15. Output Voltage Ripple (AC Coupled) ( $V_{OUT}$ : 50 mV/div, 20 µs/div)

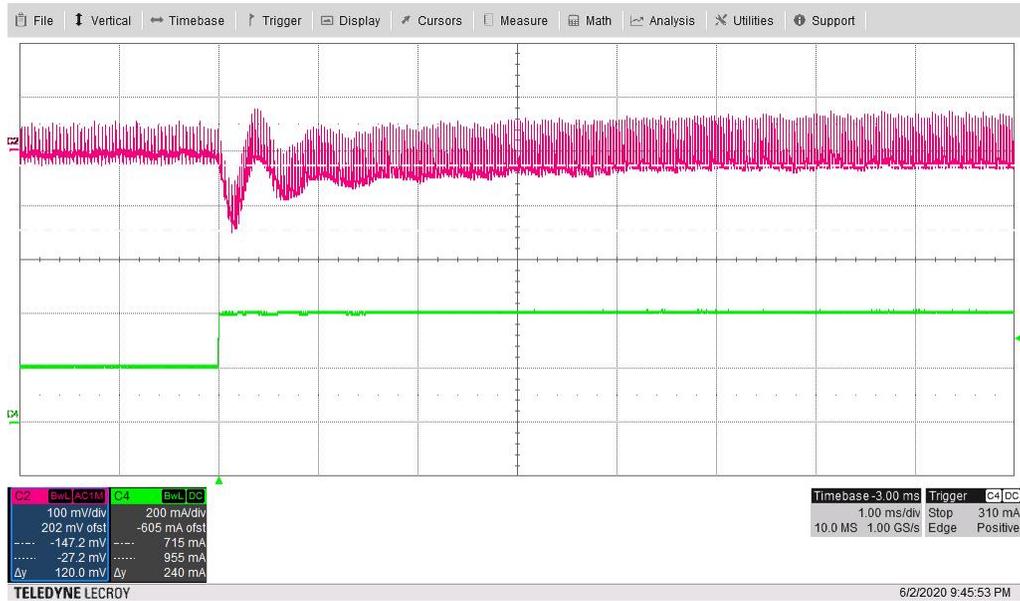
The output ripple voltage (AC coupled) is shown in the following image. The input voltage is 150 V and the 12-V output is loaded to 400 mA.



**Figure 3-16. Output Voltage Ripple (AC Coupled) ( $V_{OUT}$ : 50 mV/div, 100  $\mu$ s/div)**

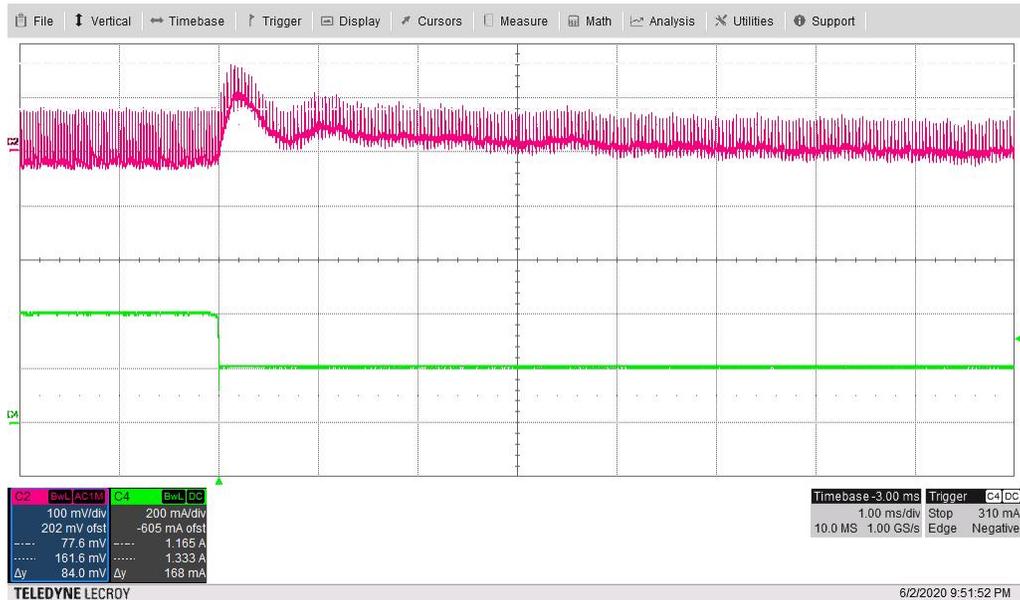
### 3.4 Load Transients

The following image shows the 12-V output voltage (AC coupled) when the load current is stepped between 200 mA and 400 mA (50% load step).  $V_{IN} = 50\text{ V}$ .



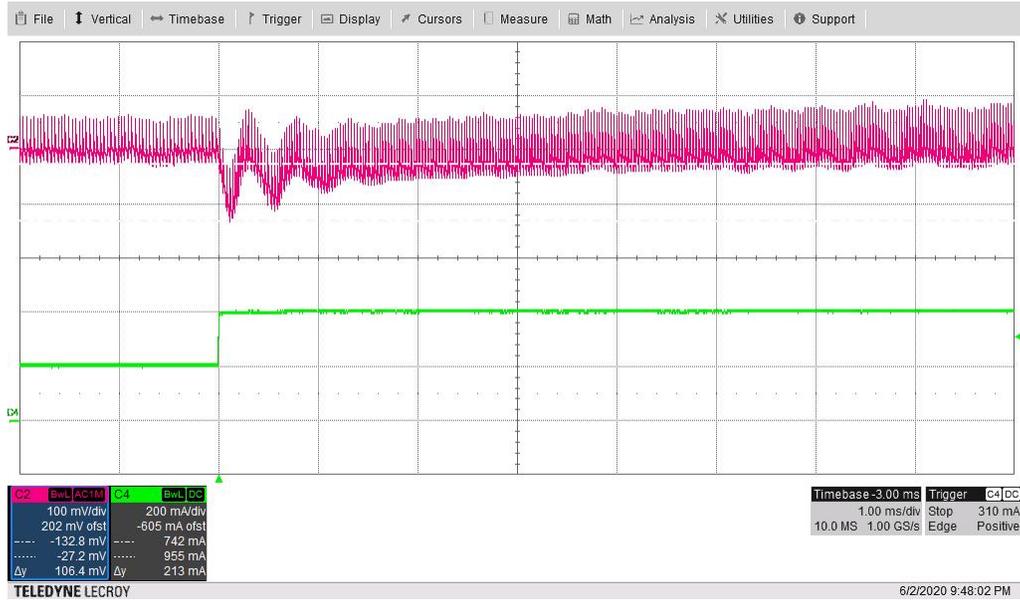
**Figure 3-17. Load Transient, 12-V Output Voltage (AC Coupled)**  
 $(V_{OUT}: 100\text{ mV/div}, I_{OUT}: 200\text{ mA/div}, 1\text{ ms/div})$

The following image shows the 12-V output voltage (AC coupled) when the load current is stepped between 400 mA and 200 mA (50% load step).  $V_{IN} = 50\text{ V}$ .



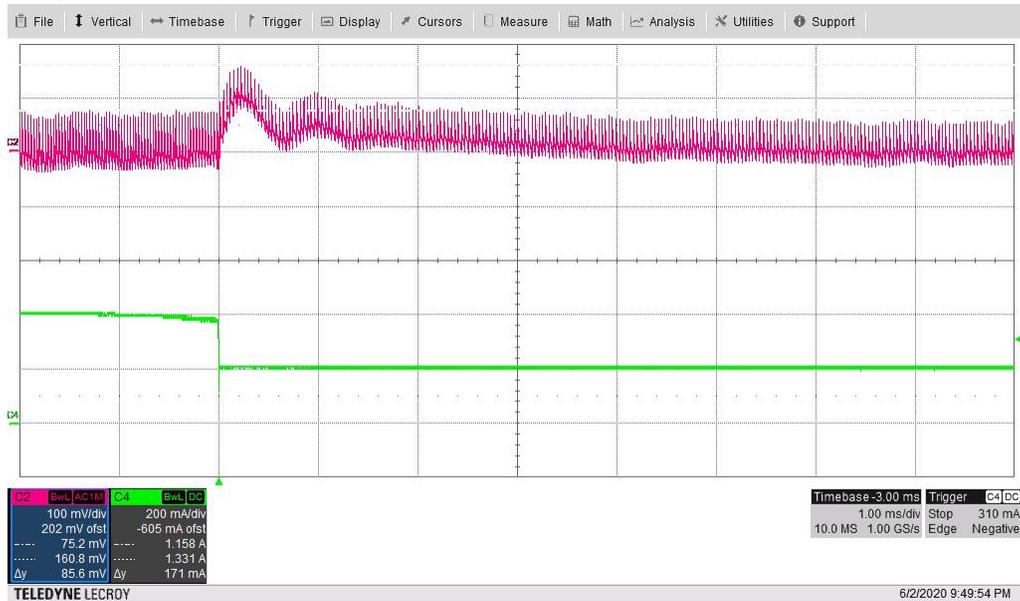
**Figure 3-18. Load Transient, 12-V Output Voltage (AC Coupled)**  
 $(V_{OUT}: 100\text{ mV/div}, I_{OUT}: 200\text{ mA/div}, 1\text{ ms/div})$

The following image shows the 12-V output voltage (AC coupled) when the load current is stepped between 200 mA and 400 mA (50% load step).  $V_{IN} = 150$  V.



**Figure 3-19. Load Transient, 12-V Output Voltage (AC Coupled)**  
 $(V_{OUT}: 100$  mV/div,  $I_{OUT}: 200$  mA/div, 1 ms/div)

The following image shows the 12-V output voltage (AC coupled) when the load current is stepped between 400 mA and 200 mA (50% load step).  $V_{IN} = 150$  V.



**Figure 3-20. Load Transient, 12-V Output Voltage (AC Coupled)**  
 $(V_{OUT}: 100$  mV/div,  $I_{OUT}: 200$  mA/div, 1 ms/div)

### 3.5 Short-Circuit Recovery Response

The following image shows the output voltage (RED) recover from a short to ground and the output load current (GREEN).  $V_{IN} = 100\text{ V}$  and  $V_{OUT}$  is 12 V at 400 mA.



Figure 3-21. Short-Circuit Recovery ( $V_{OUT}$ : 5 V/div,  $I_{OUT}$ : 500 mA/div, 50 ms/div)

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2022, Texas Instruments Incorporated