

Fluid-level sensing using 77-GHz millimeter wave



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Abstract

The IWR1443 millimeter wave (mmWave) sensor is a highly integrated 77-GHz radar device that serves as a single-chip CMOS mmWave sensor solution suitable for proximity sensing, entry-level industrial radar applications and ultra-high-accuracy range measurements.

The [IWR1443](#) sensor includes the entire millimeter-wave (mmWave) radio-frequency (RF) and analog baseband signal chain for up to three transmitters and four receivers, as well as a customer-programmable microcontroller (MCU) and hardware accelerator for radar signal processing.

This white paper covers the high-level architecture and features present in the device. We'll highlight a platform using TI's family of low-power industrial MSP430™ MCUs or SimpleLink™ MSP432™ MCUs and IWR1443 mmWave sensors to meet the power and interface requirements for legacy industrial sensors. We will also discuss some chirp-configuration examples illustrating a typical level-sensing application.

Introduction

The use of mmWave sensing technology in various industrial and automotive applications has grown tremendously in recent years. Industrial applications include tank-level probing radar, security systems, robotic vision and traffic monitoring. For fluid-level sensing, sensors offer high accuracy and robustness across varying environmental conditions, including dust and extreme temperatures. There is a shift in the industry toward the use of the 75-GHz–85-GHz frequency band due to its smaller size, high antenna directivity, larger bandwidth availability and performance advantages.

The requirements on a mmWave sensor in terms of radar data-cube memory, million instructions per second (MIPS) for processing and functional safety monitoring vary for different applications. This white paper introduces the IWR1443 mmWave sensor as a 77-GHz radar-on-chip solution for fluid-level sensing applications and presents the relevant features and high-level architecture.

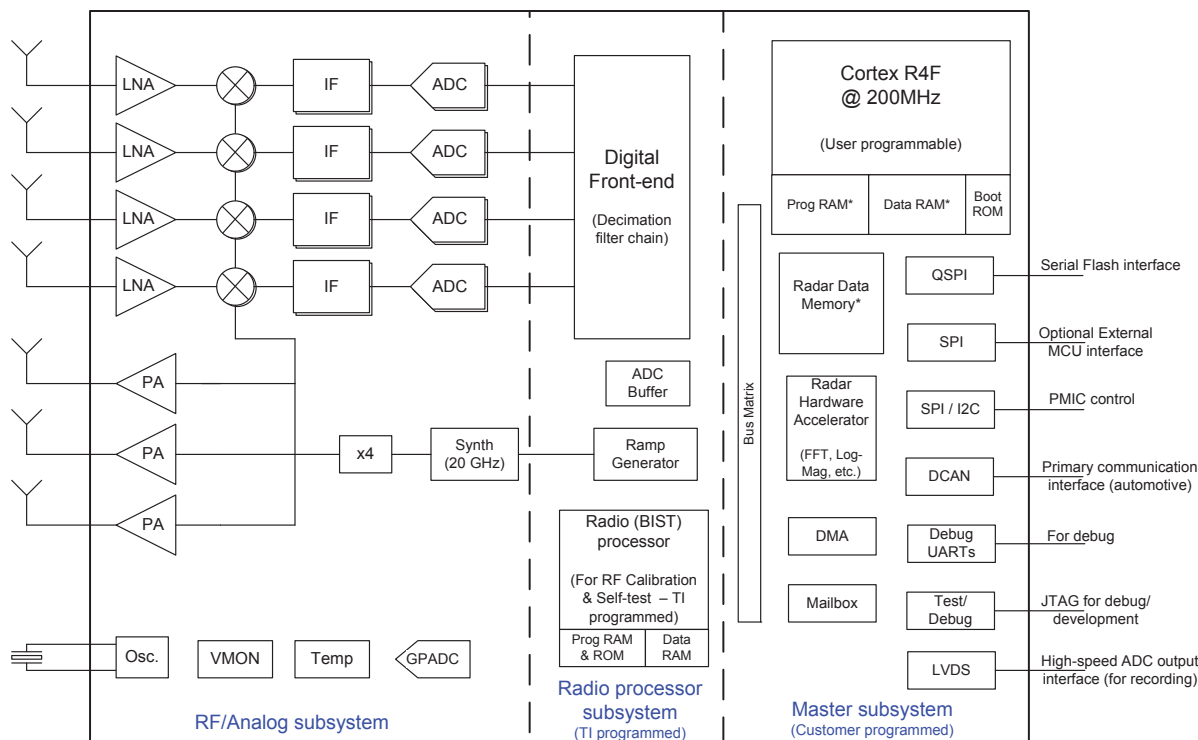


Figure 1. IWR1443 sensor high-level architecture.

The IWR1443 mmWave sensor includes the entire mmWave RF front end and analog baseband signal chain for up to three transmitters and four receivers, as well as a customer-programmable MCU and hardware accelerator for signal processing. The high-performance front end generates extremely linear high-speed ramps and supports a complex baseband with a wide intermediate frequency (IF) bandwidth for high-speed frequency-modulated continuous-wave (FMCW) radars. The [IWR1443 mmWave](#) processing subsystem supports applications with modest memory and MIPS processing requirements. This combination of a high-accuracy front

end and built-in processing is ideal for fluid-level sensing, where accuracy is paramount. The scenes are one dimensional, leading to small data cubes and reasonable computational complexity.

IWR1443 mmWave high-level architecture

Let's begin with a discussion of the high-level architecture and features of the IWR1443 mmWave sensor, as shown in the architecture diagram in **Figure 1**.

The [IWR1443 sensor](#) is a highly integrated single-chip 77-GHz mmWave sensor that includes three transmit and four receive chains, a 200-MHz user-programmable ARM® Cortex®-R4F processor, and a radar hardware accelerator. As **Figure 1** shows, the device comprises three main subsystems:

the RF/analog subsystem, the radio processor subsystem and the master subsystem.

The RF/analog subsystem includes the RF and analog circuitry: the synthesizer, power amplifier (PA), low-noise amplifier (LNA), mixer, IF amplifier and analog-to-digital converter (ADC). This subsystem also includes a crystal oscillator and temperature sensors. FMCW chirp generation occurs directly in the closed-loop 20-GHz frequency synthesizer.

The radio processor subsystem includes the digital front end, ramp generator and an internal processor for controlling and configuring low-level RF/analog and ramp generator registers based on well-defined application programming interface (API) messages from the master subsystem. (Note that this radio processor is TI-programmed and takes care of RF calibration needs and some basic built-in self-test (BIST)/monitoring functions; the radio processor is not available directly for customer use.) The digital front end takes care of filtering and decimating the raw sigma-delta ADC output and provides the final ADC data samples at a programmable sampling rate.

The master subsystem includes ARM's Cortex-R4F processor clocked at 200 MHz, which is customer programmable. This processor controls the overall operation of the device, implements the signal processing (assisted by the RF hardware accelerator) and configures the front-end transmit/receive operations via well-defined API messages, which are written to the radio processor through a mailbox interface.

The IWR1443 mmWave can function as an autonomous sensor and communicate with a private controller area network (CAN) bus through the CAN interface or using the serial peripheral interface (SPI). The device includes a quad SPI (QSPI), which can download customer code

directly from a serial Flash. Alternately, the device can operate under the control of an in-sensor host (such as an external MCU), which can communicate with the device and command it through the SPI interface, including code downloading through that interface. An additional SPI/Inter-Integrated Circuit (I²C) interface is available for power-management integrated circuit (PMIC) control when using the IWR1443 mmWave as an autonomous sensor. Although four interfaces—one CAN, one I²C and two SPIs—are present in the IWR1443 sensor for communication and PMIC control, only two of these interfaces are usable at any point in time.

The total memory available in the master subsystem is 576 KB. This is partitioned between the R4F program RAM, R4F data RAM and radar data memory. The maximum usable size for the R4F is 448 KB, partitioned between the R4F's tightly coupled memories (TCM): TCMA (320KB) and TCMB (128KB). Although the complete 448KB is unified memory and usable for programming or data, typical applications use TCMA as program memory and TCMB as data memory.

The remaining memory, starting at a minimum of 128 KB, is available as radar data memory for storing the radar data cube. It is possible to increase the radar data memory size in 64-KB increments at the cost of a corresponding reduction in R4F program or data RAM size. **Table 1** lists a couple of example supported configurations.

Option	R4F program RAM	R4F data RAM	Radar data memory
1	320 KB	128 KB	128 KB
2	256 KB	128 KB	192 KB

Table 1. Example memory configurations.

The master subsystem also includes a radar hardware accelerator to assist the R4F with frequently used radar signal-processing

computations such as fast Fourier transform (FFT) and log magnitude. Let's explore this module.

Closed-loop frequency synthesis with chirp stitching

For precise industrial process control, fluid-level sensing and tank-level probing radar require high-accuracy range measurements in order to maintain a close control over usage of the liquid and early detection of any leaks or overflow. Several factors impact range accuracy in an mmWave sensor, including RF bandwidth, signal-to-noise ratio (SNR), shape and stability of the radar target and imperfections in the radar modulation. For an FMCW radar, these latter imperfections are related to the nonlinearity of the ramp generation and the device's phase noise. The frequency-generation block then becomes the most critical block for achieving high accuracy because it typically limits all of the linearity, phase noise and RF bandwidth.

Typical FMCW radar systems use an open-loop voltage-controlled oscillator (VCO) driven by a digital-to-analog converter (DAC) to generate the radar ramps. This approach leads to significant nonlinearities and instability over time, which smears the FFT peak and leads to inaccuracy in the estimated range. This inaccuracy is only exacerbated as the sweep bandwidth increases, limiting most systems to 2 GHz of bandwidth or less.

TI's IWR1443 mmWave sensor includes a closed-loop phase-locked loop (PLL) that enables the generation of highly linear chirps, improving range accuracy. Support for the 4-GHz bandwidth without any degradation of linearity further improves the range accuracy, as the accuracy in micrometers is inversely proportional to the RF bandwidth.

Through the use of TI's mmWave complementary metal oxide semiconductor (CMOS) technology, the fractional-N PLL can be highly efficient and still suppress quantization noise, eliminating any trade-off between linearity and phase noise.

Synchronously generated mmWave waveforms enable additional freedom in a fluid-level sensing application. Specifically, you can precisely generate two ramps starting at different frequencies without any additional error over a single ramp. A 1-GHz ramp can be generated from 76 GHz–77 GHz, followed by a 4-GHz ramp at 77 GHz–81 GHz. Digitally stitching together the reflected waveforms from both ramps further improves accuracy by 25 percent.

Radar hardware accelerator

The radar hardware accelerator module enables the offloading of certain frequently used computations in FMCW radar signal processing from the R4F processor. FMCW radar signal processing involves the use of FFT and log-magnitude computations in order to obtain a radar image across range, velocity and angle dimensions. Some frequently used functions in FMCW radar signal processing occur within the radar hardware accelerator, while proprietary algorithms related to clustering or object tracking happen in the R4F processor.

The key features of the radar hardware accelerator are:

- Fast FFT computation, with programmable sizes (powers of 2) up to a 1,024-point complex FFT.
- Internal FFT bit width of 24 bits (each for I and Q) for good signal-to-quantization-noise ratio (SQNR) performance, with fully programmable butterfly scaling at every radix-2 stage for user flexibility.
- Built-in capabilities for simple pre-FFT processing: programmable windowing, basic binary phase modulation (BPM) removal and interference zeroing-out.
- Magnitude (absolute value) and log-magnitude computation capability.
- Flexible data-flow and data-sample arrangement to support efficient multi-

dimensional FFT operations and transpose accesses as required.

- Chaining and looping mechanism to sequence a set of accelerator operations with minimal intervention from the main processor.
- Constant false-alarm rate—cell averaging (CFAR-CA) detector supporting linear and logarithmic modes.
- Miscellaneous other capabilities: FFT stitching (up to 4k FFT), slow discrete Fourier transform (DFT) and complex vector-multiplication capability.

The radar hardware accelerator shown in **Figure 2** comprises four memories, each 16 KB, that send input data to and pull output data from the main accelerator engine. These memories are referred to as the radar hardware accelerator’s “local memories” and are separate from the 576 KB of total RAM described in the previous section.

The general data flow that is that the direct memory access (DMA) module brings in samples (such as FFT input samples) into the radar hardware accelerator’s local memories so that the main

accelerator engine can access and process these samples. Once the accelerator’s processing is done, the DMA module reads the output samples from these local memories and stores them back in either radar data cube memory or R4F data RAM for further processing by the R4F processor. The red arrows in **Figure 2** indicate data movement from and to radar data cube memory into and out of local memories for both the FFT and other processing steps.

The purpose behind four separate 16-KB memories inside the radar hardware accelerator is to enable a “ping-pong” mechanism, both for the input and for the output, such that DMA write (and read) operations can happen in parallel to the accelerator’s main computational processing. The presence of four memories enables such parallelism.

Two types of registers configure radar hardware accelerator operations: “parameter sets” and static (common) registers. Parameter sets enable the pre-programming of a complete sequence of accelerator operations (with appropriate source and destination memory addresses and other configurations specified for each operation in that sequence), such that the accelerator can perform them with minimal intervention from the R4F processor. A state machine built into the accelerator handles the loading of one parameter-set configuration at a time and sequences pre-programmed operations, thus reducing the need for frequent interruptions to the R4F processor.

The operating clock frequency of the radar hardware accelerator is 200 MHz. The internal architecture of the accelerator engine is such that a steady-state FFT throughput of 200 MSPS is possible—one FFT input and one FFT output every clock cycle, after an initial latency. The [IWR1443 Technical Reference Manual](#) provides further information about its capabilities and usage procedure.

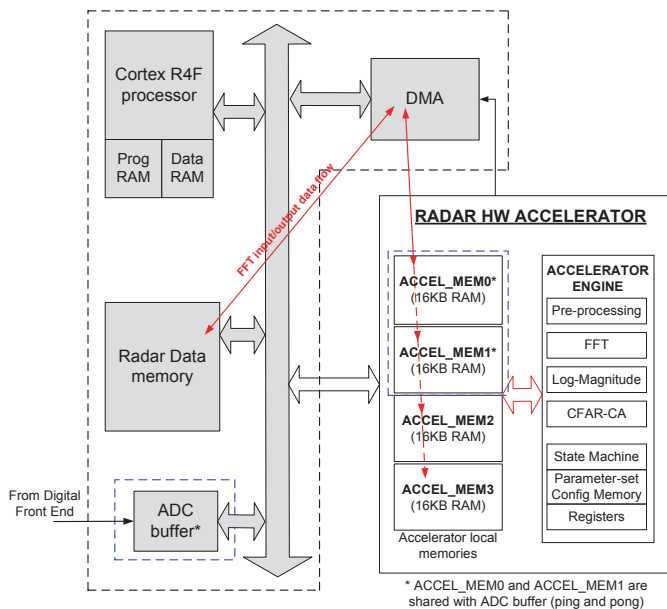


Figure 2. Radar hardware accelerator.

IWR1443 use case

The primary requirements for fluid-level sensing are extremely high distance accuracy and compatibility with loop-powered applications, which places stringent power requirements on the complete radar module to draw < 4 mA from 15 V.

The IWR1443 sensor, in combination with a low-power external MCU, can enable applications where the IWR1443 device performs the primary mmWave signal-processing computations (FFT, peak detection, range interpolation), while the external MCU handles the secondary computations and industrial-specific interfaces. Certain industrial use cases require two-wire loop-powered operation, which poses a stringent requirement on the power consumption. Since the IWR1443 sensor does not support a low-leakage sleep mode, in such cases the device needs to be powered down and brought up for every measurement cycle to reduce the average power consumption.

Figure 3 shows an example loop-powered system using the IWR1443 sensor and TI's MSP430 MCU. In this configuration, the ultra-low-power 16-bit MSP430 MCU serves as the master of the system, running the Highway Addressable Remote Transducer (HART) protocol modem to communicate over the 4 mA–20 mA interface and duty-cycling the IWR1443 sensor for each burst of chirps. For higher processing performance for local analytics or additional integrated analog needs, you can use the low-power 32-bit MSP432 MCU as well. The MSP432 MCU can also serve as an optimized

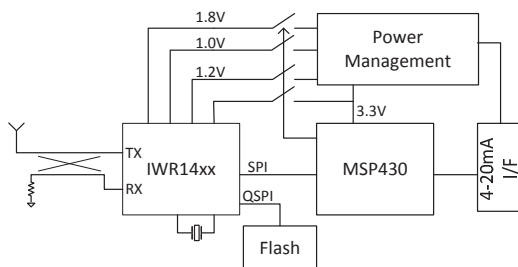


Figure 3. System diagram of IWR1443 sensor plus MSP430 MCU for loop-powered fluid-level sensing.

wireless host MCU to transmit the radar data wirelessly via a wide range of wireless communication protocols including BLE, Sub-1 GHz and Wi-Fi®.

Before each measurement, the MSP430 MCU enables the IWR1443 sensor, which then downloads any application code stored in the serial fFlash using QSPI. The application running on the Cortex-R4F configures the radar front end (BIST processor) and communicates with the MSP430 MCU over SPI. The IWR1443 triggers a burst of chirps, storing them into radar data cube memory. In the background, the radar hardware accelerator performs FFTs on each chirp and accumulates the results for improved SNR. The hardware accelerator and Cortex-R4F perform detection and post-processing, with the final level communicated to the MSP430 MCU over SPI. Alternatively, the FFT outputs could be directly output to the MSP430 MCU for final post-processing. Finally, the MSP430 MCU completely shuts down the IWR1443 sensor before the next burst.

For this example, the maximum continuous sweep bandwidth is 4,000 MHz (which gives a range resolution of 3.75 cm), with a 2,048-point complex FFT. Five chirps are taken consecutively, with the hardware accelerator combining the FFT outputs.

Table 2 summarizes the full chirp configuration.

Example chirp configuration for illustrative purposes (one TX, one RX)	
Sweep bandwidth	4,000 MHz
Range resolution	3.75 cm
Maximum unambiguous range	60 m
Ramp slope	20 MHz/μs
Chirp duration	200 μs valid (+10 μs inter-chirp)
Number of chirps	5
Maximum beat frequency	8.9 MHz
ADC sampling rate (I, Q)	10 MSPS (complex)
Frame time	5 × 210 μs = 1.1 ms
Range FFT size	2,048 (complex)
Radar data memory	2,048 × 5 × 1 RX × 4 Bytes = 40 KB

Table 2. Chirp configuration and radar performance for fluid-level sensing.

As you can see from **Table 2**, the above example uses the lowest configuration of radar data memory, starting at 128 KB.

The overall power consumed by the IWR1443 sensor includes that used during the initial configuration, including code download, the active radar period, the post-processing of the data and the transfer of outputs to the MSP432 MCU. The peak power of the IWR1443 sensor is roughly 1.3 W, which averaged over frame rates of 2 Hz–4 Hz is below 6 mW, well within the power budget of a 4 mA–20 mA link. Different strategies are available to manage the rest of the operations that trade off code download time, output transfer time, and the partitioning of computation between the IWR1443 sensor and the MSP432 MCU. Please see the [Power Optimization for IWR1443 77-GHz Level Transmitter Reference Design](#) for more details.

Summary

Given its highly linear chirp generation and high integration, the IWR1443 sensor plus MSP430/MSP432 MCU can deliver compact and high-accuracy fluid-level sensing measurements.

For more information

To learn more about the [IWR1443 portfolio](#) please visit the below links.

- [Portfolio portal page](#)
- [TI Design](#)
- [mmWave white paper overview](#)

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