TEXAS INSTRUMENTS

THS4222EVM

User's Guide

September 2002 *High Performance Linear Products*

SLOU144

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

EVM IMPORTANT NOTICE

Texas Instruments (TI) provides the enclosed product(s) under the following conditions:

This evaluation kit being sold by TI is intended for use for **ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY** and is not considered by TI to be fit for commercial use. As such, the goods being provided may not be complete in terms of required design-, marketing-, and/or manufacturing-related protective considerations, including product safety measures typically found in the end product incorporating the goods. As a prototype, this product does not fall within the scope of the European Union directive on electromagnetic compatibility and therefore may not meet the technical requirements of the directive.

Should this evaluation kit not meet the specifications indicated in the EVM User's Guide, the kit may be returned within 30 days from the date of delivery for a full refund. THE FOREGOING WARRANTY IS THE EXCLUSIVE WARRANTY MADE BY SELLER TO BUYER AND IS IN LIEU OF ALL OTHER WARRANTIES, EXPRESSED, IMPLIED, OR STATUTORY, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE.

The user assumes all responsibility and liability for proper and safe handling of the goods. Further, the user indemnifies TI from all claims arising from the handling or use of the goods. Please be aware that the products received may not be regulatory compliant or agency certified (FCC, UL, CE, etc.). Due to the open construction of the product, it is the user's responsibility to take any and all appropriate precautions with regard to electrostatic discharge.

EXCEPT TO THE EXTENT OF THE INDEMNITY SET FORTH ABOVE, NEITHER PARTY SHALL BE LIABLE TO THE OTHER FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES.

TI currently deals with a variety of customers for products, and therefore our arrangement with the user **is not exclusive**.

TI assumes **no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein**.

Please read the EVM User's Guide and, specifically, the EVM Warnings and Restrictions notice in the EVM User's Guide prior to handling the product. This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact the TI application engineer.

Persons handling the product must have electronics training and observe good laboratory practice standards.

No license is granted under any patent right or other intellectual property right of TI covering or relating to any machine, process, or combination in which such TI products or services might be or are used.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 4 V (differential) and ±7.5 V (Vs-, Vs+) when using a dual-supply power source—maximum 15 V when using a single-supply power source (Vs).

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 70°C. The EVM is designed to operate properly with certain components above 70°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Read This First

Information About Cautions and Warnings

This book may contain cautions and warnings.

This is an example of a caution statement.

A caution statement describes a situation that could potentially damage your software or equipment.

This is an example of a warning statement.

A warning statement describes a situation that could potentially cause harm to you.

The information in a caution or a warning is provided for your protection. Please read each caution and warning carefully.

FCC Warning

This equipment is intended for use in a laboratory test environment only. It generates, uses, and can radiate radio frequency energy and has not been tested for compliance with the limits of computing devices pursuant to subpart J of part 15 of FCC rules, which are designed to provide reasonable protection against radio frequency interference. Operation of this equipment in other environments may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, refer to SSYA008.

Related Documentation From Texas Instruments

The URL's below are correct as of the date of publication of this manual. Texas Instruments applications apologizes if they change over time.

- THS4222 data sheet (SLOS399)
- Application report (SLOA069), *How (Not) to Decouple High Speed Op Amp Circuits,* http://www-s.ti.com/sc/psheets/sloa069/sloa069.pdf
- Application report (SLMA002), *PowerPAD Thermally Enhanced Package*, http://www-s.ti.com/sc/psheets/slma004/slma002.pdf
- Application report (SLMA004), PowerPAD Made Easy, http://www-s.ti.com/sc/psheets/slma004/slma004.pdf
- Application report (SSYA008), Electrostatic Discharge (ESD), http://www-s.ti.com/sc/psheets/ssya008/ssya008.pdf
- High-Speed Amplifier PCB Layout Tips, http://www-s.ti.com/sc/psheets/sloa102/sloa102.pdf

Trademarks

PowerPAD is a trademark of Texas Instruments.

Contents

Figures

Tables

Chapter 1

Introduction and Description

This EVM provides a platform for testing the THS4222 in the 8-pin MSOP (DSN) package. It contains the high-speed op amp, a number of passive components, and various features and footprints that enable the user to experiment, test and verify various operational amplifier circuit implementations.

1.1 Evaluation Schematic

As delivered, the EVM has a fully functional example circuit—just add power supplies, a signal source, and monitoring instrument. See Figure 1–1 for the default schematic diagram. The user can change the gain by changing the ratios of the feedback and gain resistors (see the device data sheet for recommended resistor values). The EVM includes the following features:

- Wide operating supply voltage range: dual supply ±1.35 V to dual supply ±7.5 V operation (see the device data sheet). Single supply operation is obtained by connecting both J6 (GND) and J7 (VS–) to ground. Operating supply voltage range for single supply is 2.7 V to 15 V.
- Convenient GND test point (TP1)
- Power supply ripple rejection provided by inductors FB1 and FB2 followed by tantalum capacitors C5 and C6
- Decoupling capacitors, C7 and C8, populated with 0.1 μF and capacitors, C9 and C10, populated with 100 pF—design final decoupling in accordance with SLOA069
- Nominal 50-Ω input impedance for each of the configured inputs, V1in–, V1in+ and V2in+. Termination can be configured according to the application requirement.
- A good example of high-speed amplifier PCB design and layout. Also see High-Speed Amplifier PCB Layout Tips, SLOA102.
- 50-Ω input matching resistors (R3 and R10)
- 953-Ω and 453-Ω resistors along with the 49.9-Ω resistors to ground provide minimum load of 1 kΩ and 500 Ω on EVM channel 1 and channel 2 respectively.
- User customizable / configurable component choice
- Nominal 50-Ω signal traces for input and outputs to reduce signal reflections within this board

- Power PAD™ heatsinking capability

EVM Channel 1:

The default configuration for EVM channel 1 is designed to provide a voltage gain of +1 with the amplifier loaded with approximately 1 kΩ. This voltage gain is the ratio of the voltage at the output pin of the amplifier (pin 1) to the voltage input at J3.

R6 jumper makes EVM section 1 amplifier a unity gain buffer. R3 is 49.9 Ω to match the impedance of a 50-Ω signal generator. R5 and R4 form a voltage divider to J1, the EVM channel 1 output jack. The following equation represents the voltage gain to J1, if a measurement device with a 50-Ω input impedance is connected to J3.

$$\frac{V_O}{V_I} = \left(\frac{R4 \parallel 50\ \Omega}{R4 \parallel 50\ \Omega + R5}\right) = 0.0255 \qquad (1)$$

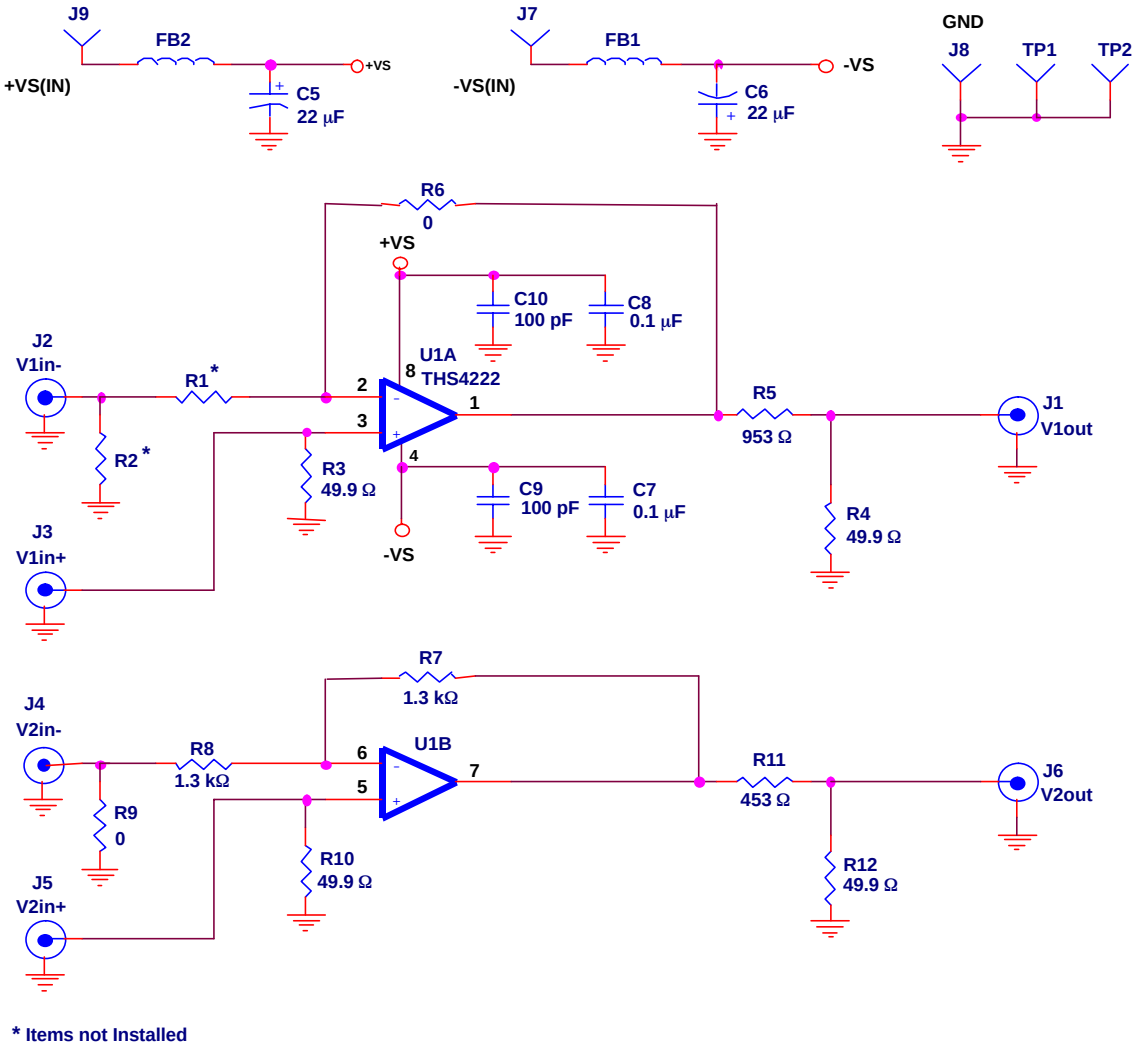
EVM Channel 2:

The default configuration design for EVM channel 2 provides a voltage gain of +2. This voltage gain is the ratio of the voltage at the output pin of the amplifier (pin 7) to the voltage at the J5 input. R7 and R8 are equal and therefore provide for a gain of +2.

The noninverting gain of the EVM channel 2 amplifier, when using the default configuration, is affected by a voltage divider similar to that in EVM channel 1 composed of R11 and R12. When using a 50-Ω signal source and 50-Ω measurement device, its voltage gain (from J5 to J6) is indicated in the following equation.

$$\frac{V_O}{V_I} = \left(1 + \frac{R7}{R8 + R9}\right)\left(\frac{R12 \parallel 50\ \Omega}{R12 \parallel 50\ \Omega + R11}\right) = 0.105 \qquad (2)$$

Figure 1-1. Schematic of the THS4222EVM



*** Items not Installed**

Chapter 2

Using the THS4222EVM

This chapter shows how to connect the THS4222EVM to test equipment. It is recommended that the user connect the EVM as shown in this chapter to avoid damage to the EVM or the THS4222 installed on the board. Figure 2-1 shows how to connect the power supplies, 50-Ω signal source and 50-Ω monitoring instrument.

Figure 2-1. THS4222EVM Connection Diagram

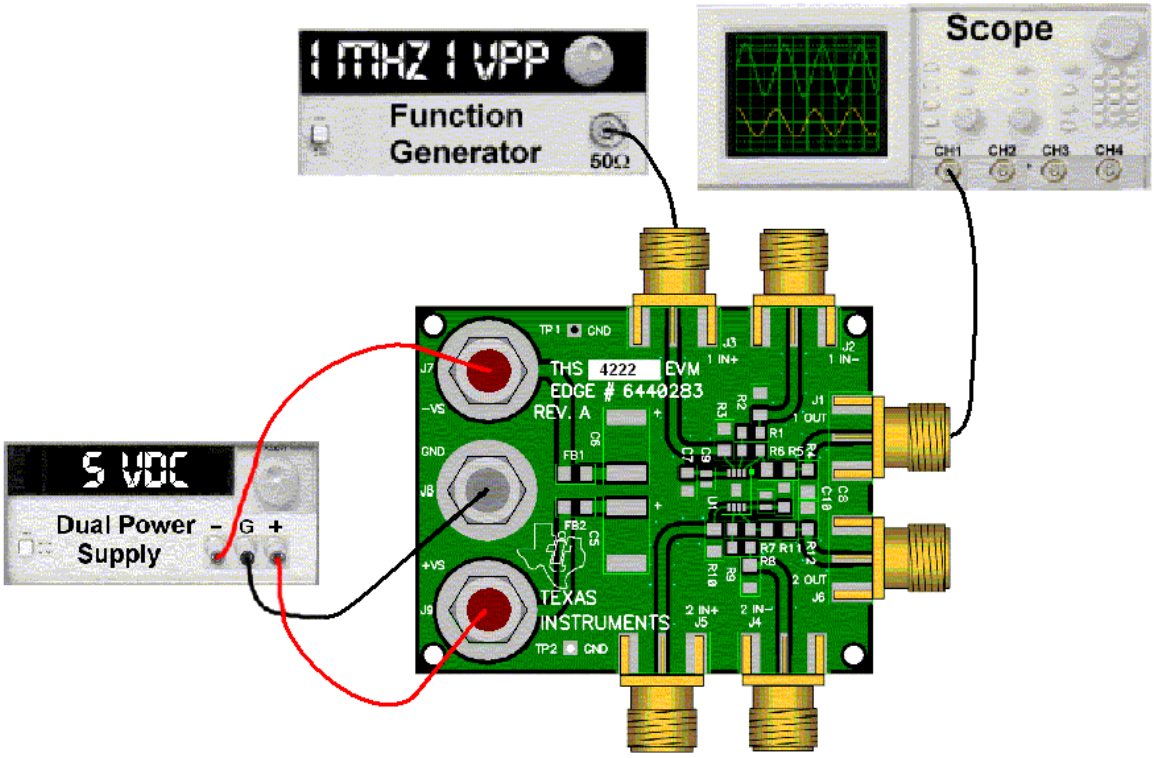


Figure 2-1 shows the connections to measure output 1 while a signal is inserted into the channel 1, noninverting input of the EVM. If the oscilloscope input is connected to J6, and the signal source is connected to J5, EVM channel 2 is also configured for a noninverting signal path.

Chapter 3

THS4222EVM Applications

Example applications are presented in this chapter. These applications are meant to demonstrate the most popular circuits to the user, but many other circuits can be constructed. The user is encouraged to experiment with different circuits, exploring new and creative design techniques. That, after all, is the function of an evaluation board.

3.1 Inverting Video Gain Stage

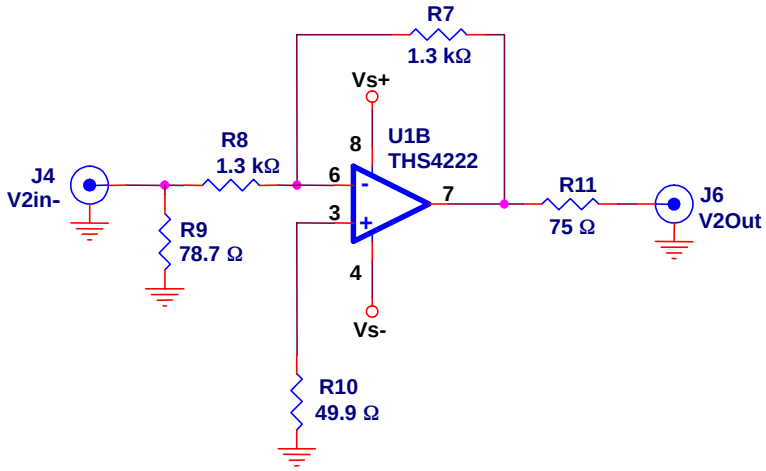
The circuit described in Chapter 1 is an inverting gain stage with a voltage divider on the output. Equation 1 indicates the gain when R9 is changed to 78.7 Ω, R11 is changed to 75 Ω and R12 is removed. Rt is the termination resistance of the measurement device. The voltage gain from J4 to J6 is simplified, as shown:

$$\frac{V_O}{V_I} = -\frac{R7}{R8}\left(\frac{Rt}{Rt + R11}\right) = 0.5 \qquad (1)$$

R11 is used to match the output impedance of the amplifier to the line being driven and the instrument taking measurements. For short transmission line length, R11 can be replaced with a jumper.

R11 can also be used to isolate the amplifier from large capacitive loads.

Figure 3-1. Inverting Video Gain Stage

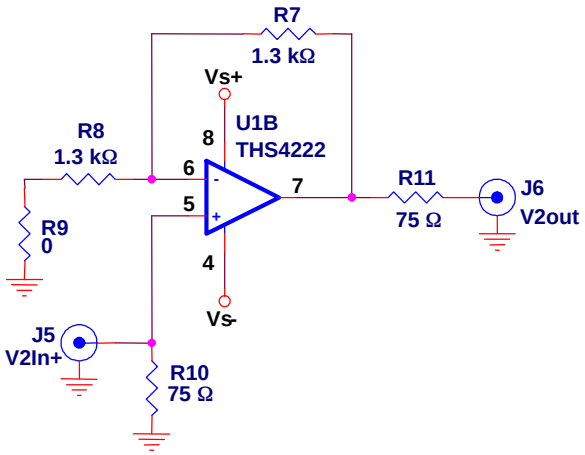


3.2 Noninverting Video Gain Stage

For a noninverting stage in EVM channel 2, the gain error imposed by R9 can be eliminated by replacing R9 with a 0-Ω resistor. Rt is the termination resistor of 75 Ω, as shown in Figure 3-2. As in the inverting gain stage example above, R12 has been removed. The following equation indicates the voltage gain from J5 to J6 when connected to a 75-Ω measurement instrument.

$$\frac{V_O}{V_I} = \left(1 + \frac{R7}{R8}\right)\left(\frac{Rt}{Rt + R11}\right) = 1 \qquad (2)$$

Figure 3-2. Noninverting Video Gain Stage



This is a common amplifier configuration used to drive transmission lines. The 75-Ω resistor in series with the output is for connection to a video instrument or circuit.

3.3 Applications for EVM Channel 2

Since the board layout of EVM Channel 1 is identical to EVM Channel 2, the applications above can be applied identically. The only physical difference is the component values installed in the default configuration for the different EVM channels. In addition, the components are labeled differently for each EVM channel. Refer to the complete schematic, and board silkscreen to locate and resolve the differences.

Chapter 4

EVM Hardware Description

This chapter describes the EVM hardware. It includes the EVM parts list, and printed circuit board layout.

Table 4-1. THS4222EVM Bill of Materials

Item	Description	SMD Size	Reference Designator	PCB	Manufacturer's Part Number	Distributor's Part Number
1	Bead, ferrite, 3A, 80 Ω	1206	FB1, FB2	2	(Steward) HI1206N800R-00	(Digi-Key) 240-1010-1-ND
2	Cap, 22 μF, tanatalum, 25 V, 10%	D	C5, C6	2	(AVX) TAJD226K025R	(Garrett) TAJD226K025R
3	Cap, 0.1 μF, ceramic, X7R, 50 V	0805	C7, C8	2	(AVX) 08055C104KAT2A	(Garrett) 08055C104KAT2A
4	Cap, 100 pF, ceramic, 5%, 150 V	AQ12	C9, C10	2	(AVX) AQ12EM101JAJME	(TTI) AQ12EM101JAJME
5	Open	0805	R1	1		
6	Resistor, 0 Ω, 1/8 W, 1%	0805	R6	1	(Phycomp) 9C08052A0R00JLHFT	(Garrett) 9C08052A0R00JLHFT
7	Resistor, 1.3 kΩ, 1/8 W, 1%	0805	R7, R8	2	(Phycomp) 9C08052A1301FKHFT	(Garrett) 9C08052A1301FKHFT
8	Open	1206	R2	1		
9	Resistor, 0 Ω, 1/4 W, 1%	1206	R9	1	(Phycomp) 9C1206A0R00JLHFT	(Garrett) 9C1206A0R00JLHFT
10	Resistor, 49.9 Ω, 1/4W, 1%	1206	R3, R4, R10, R12	4	(Phycomp) 9C12063A49R9FKRFT	(Garrett) 9C12063A49R9FKRFT
11	Resistor, 453 Ω, 1/4 W, 1%	1206	R11	1	(Phycomp) 9C12063A4530FKRFT	(Garrett) 9C12063A4530FKRFT
12	Resistor, 953 Ω, 1/4 W, 1%	1206	R5	1	(Phycomp) 9C12063A9530FKRFT	(Garrett) 9C12063A9530FKRFT
13	Jack, banana receptacle, 0.25" Dia. Hole		J7, J8, J9	3	(HH Smith) 101	(Newark) 35F865
14	Test point, black		TP1, TP2	2	(Keystone) 5001	(Allied) 839-3601
15	Connector, edge, SMA PCB Jack		J1, J2, J3, J4, J5, J6	6	(Johnson) 142-0701-801	(Allied) 528-0238
16	IC, THS4222		U1	1	(TI) THS4222DGN	
17	Printed-circuit board			1	(TI) EDGE #6440283 Rev.A	

Figure 4-1. Top View Showing Top Layer and Component Placement for THS4222EVM

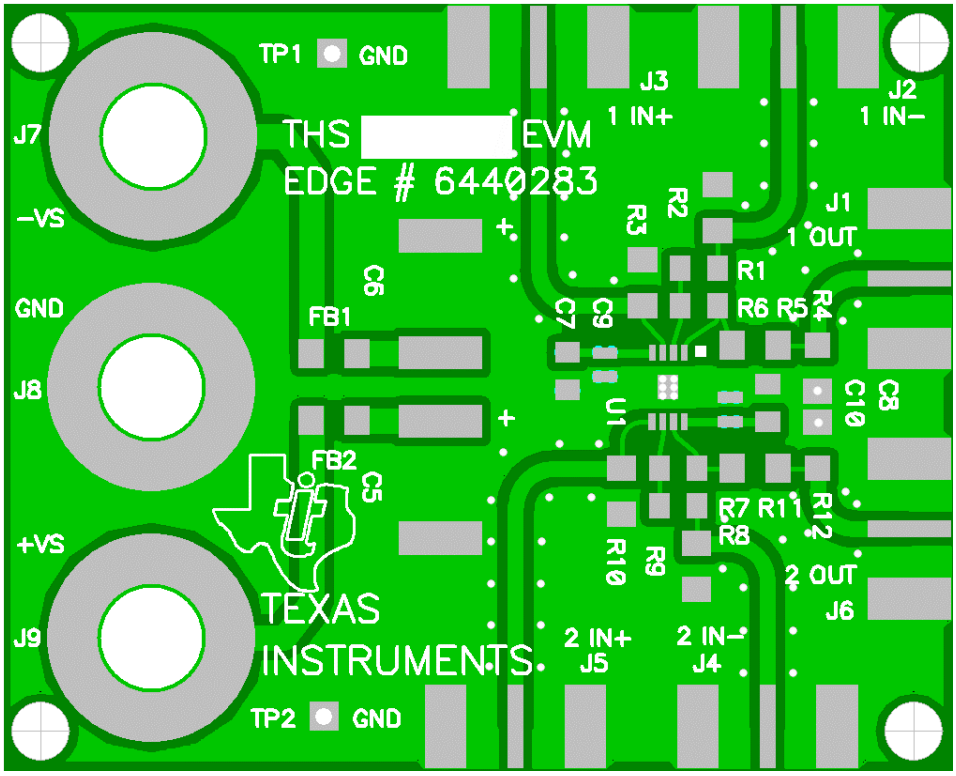


Figure 4-2. Internal Plane (Layer 2) Ground Plane

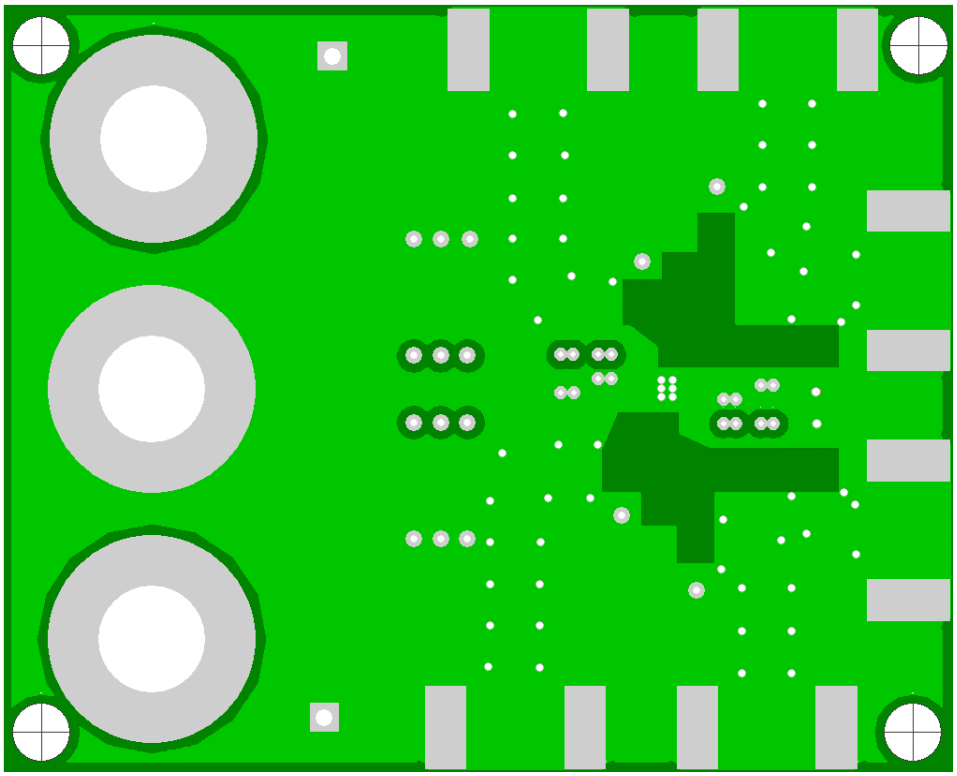


Figure 4-3. Internal Plane (Layer 3) Power Plane7

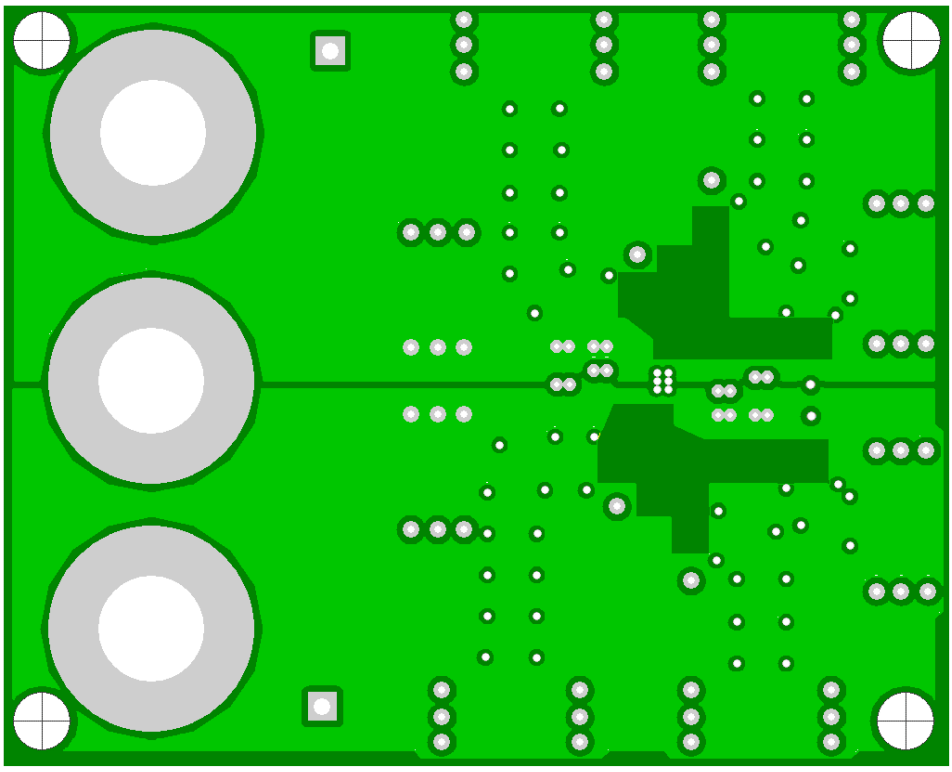


Figure 4-4. Bottom (Layer 4) Ground and Signal