TMS320C6000 DSP Interrupt Selector Reference Guide

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Preface

Read This First

About This Manual

This document describes the interrupt selector, interrupt selector registers, and the available interrupts in the digital signal processors (DSPs) of the TMS320C6000™ DSP family.

Notational Conventions

This document uses the following conventions.

- Hexadecimal numbers are shown with the suffix h. For example, the following number is 40 hexadecimal (decimal 64): 40h.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure designate a bit that is used for future device expansion.

Related Documentation From Texas Instruments

The following documents describe the C6000™ devices and related support tools. Copies of these documents are available on the Internet at www.ti.com. *Tip:* Enter the literature number in the search box provided at www.ti.com.

TMS320C6000 CPU and Instruction Set Reference Guide (literature number SPRU189) describes the TMS320C6000™ CPU architecture, instruction set, pipeline, and interrupts for these digital signal processors.

TMS320C6000 Peripherals Reference Guide (literature number SPRU190) describes the peripherals available on the TMS320C6000™ DSPs.

TMS320C6000 Technical Brief (literature number SPRU197) gives an introduction to the TMS320C62x™ and TMS320C67x™ DSPs, development tools, and third-party support.

TMS320C64x Technical Overview (SPRU395) gives an introduction to the TMS320C64x™ DSP and discusses the application areas that are enhanced by the TMS320C64x VelociTI™.

TMS320C6000 Programmer's Guide (literature number SPRU198) describes ways to optimize C and assembly code for the TMS320C6000™ DSPs and includes application program examples.

TMS320C6000 Code Composer Studio Tutorial (literature number SPRU301) introduces the Code Composer Studio™ integrated development environment and software tools.

Code Composer Studio Application Programming Interface Reference Guide (literature number SPRU321) describes the Code Composer Studio™ application programming interface (API), which allows you to program custom plug-ins for Code Composer.

TMS320C6x Peripheral Support Library Programmer's Reference (literature number SPRU273) describes the contents of the TMS320C6000™ peripheral support library of functions and macros. It lists functions and macros both by header file and alphabetically, provides a complete description of each, and gives code examples to show how they are used.

TMS320C6000 Chip Support Library API Reference Guide (literature number SPRU401) describes a set of application programming interfaces (APIs) used to configure and control the on-chip peripherals.

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Interrupt Selector and Exernal Interrupts

This document describes the interrupt selector, interrupt selector registers, and the available interrupts in the digital signal processors (DSPs) of the TMS320C6000™ DSP family.

1 Overview

The C6000™ DSP peripheral set has up to 32 interrupt sources. The CPU however has 12 interrupts available for use. The interrupt selector allows you to choose and prioritize which 12 of the 32 your system needs to use. The interrupt selector also allows you to effectively change the polarity of external interrupt inputs.

Table 1 summarizes the differences between the interrupt selectors of the C6000 devices.

Table 1. Differences in C6000 DSP Interrupt Selectors

Features	Supported on Device
Available Interrupts	C6000 devices have different available interrupts according to their peripheral sets.
IACK and INUM pins	C620x/C670x DSP only
EXT_INT4–EXT_INT7 pins	All C6000 devices. On C64x DSP, these pins are MUXed with the GPIO peripheral pins.

2 Available Interrupt Sources

Table 2 lists the available interrupts on the C620x/C670x DSP. See the device-specific datasheet for a list of the available interrupts on the C621x/C671x DSP and C64x™ DSP. For more information on interrupts, including the interrupt vector table, see the *TMS320C6000 CPU and Instruction Set Reference Guide* (SPRU189).

Table 2. TMS320C620x/C670x DSP Available Interrupts

Interrupt Selection Number	Interrupt Acronym	Interrupt Description
00000b	DSPINT	Host port to DSP interrupt
00001b	TINT0	Timer 0 interrupt
00010b	TINT1	Timer 1 interrupt
00011b	SD_INT	EMIF SDRAM timer interrupt
00100b	EXT_INT4	External interrupt pin 4
00101b	EXT_INT5	External interrupt pin 5
00110b	EXT_INT6	External interrupt pin 6
00111b	EXT_INT7	External interrupt pin 7
01000b	DMA_INT0	DMA channel 0 interrupt
01001b	DMA_INT1	DMA channel 1 interrupt
01010b	DMA_INT2	DMA channel 2 interrupt
01011b	DMA_INT3	DMA channel 3 interrupt
01100b	XINT0	McBSP 0 transmit interrupt
01101b	RINT0	McBSP 0 receive interrupt
01110b	XINT1	McBSP 1 transmit interrupt
01111b	RINT1	McBSP 1 receive interrupt
10000b	–	Reserved
10001b	XINT2†	McBSP 2 transmit interrupt
	PCI_WAKEUP‡	PCI wake up interrupt
10010b	RINT2†	McBSP 2 receive interrupt
	ADMA_HLT‡	Auxiliary DMA halted interrupt
10011–11111b	–	Reserved

† Only available on the C6202(B) DSP and C6203(B) DSP
‡ Only available on the C6205 DSP

3 External Interrupt Signal Timing

EXT_INT4−EXT_INT7 and NMI are dedicated external interrupt sources (EXT_INT4−EXT_INT7 pins are MUXed with the GPIO peripheral pins on the C64x DSP). In addition, the receive frame synchronization (FSR) and transmit frame synchronization (FSX) signals of the multichannel buffered serial port (McBSP) can be programmed to directly drive the RINT and XINT signals. Because these signals are asynchronous, they are synchronized before being sent to either the DMA/EDMA or CPU. Refer to the *TMS320C6000 CPU and Instruction Set Reference Guide* (SPRU189) and your device-specific datasheet for details on external interrupt signals timing.

For the C620x/C670x DSP, the NMI can interrupt a maskable interrupt fetch packet (ISFP) just before the interrupt reaches E1. In this case, an IACK and INUM for the NMI is not seen because the IACK and INUM corresponding to the maskable interrupt is on the pins.

Note:

The IACK and INUM pins do not exist on the C621x/C671x DSP and C64x DSP. These pins only exist on the C620x/C670x DSP.

4 Configuring the Interrupt Selector

The interrupt selector registers are meant to be configured once after reset during initialization and before enabling interrupts.

Note:

After the registers have been set, the interrupt flag register should be cleared to remove any spurious transitions caused by the configuration.

You may reconfigure the interrupt selector during other times, but spurious interrupt conditions may be detected by the CPU on the interrupts affected by the modified fields. For example, if EXT_INT4 is low, EXT_INT5 is high, and INT9 is remapped from EXT_INT4 to EXT_INT5, the low-to-high transition on INT9 is recognized as an interrupt and sets IF9.

5 Registers

Table 3 shows the interrupt selector registers. The interrupt multiplexer registers determine the mapping between the interrupt sources described in section 2 and the CPU interrupts 4 through 15 (INT4–INT15). The external interrupt polarity register sets the polarity of external interrupts. See the device-specific datasheet for the memory address of these registers.

Table 3. Interrupt Selector Registers

Acronym	Register Name	Section
MUXH	Interrupt multiplexer high register	5.1
MUXL	Interrupt multiplexer low register	5.2
EXTPOL	External interrupt polarity register	5.3

5.1 Interrupt Multiplexer High Register (MUXH)

The interrupt multiplexer high register (MUXH) maps the interrupt sources to particular interrupts. The MUXH is shown in Figure 1 and described in Table 4. The INTSEL10–INTSEL15 fields correspond to the CPU interrupts INT10–INT15. By setting the INTSEL bits to the value of the desired interrupt selection number, you can map any interrupt source to any CPU interrupt. The default values of the INTSEL bits are shown in Figure 1. The default mapping of interrupt sources to CPU interrupts for the C620x/C670x devices are shown in Table 6 (page 13). For the default mapping of interrupt sources to CPU interrupts for the C621x/C671x and C64x devices, see the device-specific datasheet.

5.2 Interrupt Multiplexer Low Register (MUXL)

The interrupt multiplexer low register (MUXL) maps the interrupt sources to particular interrupts. The MUXL is shown in Figure 2 and described in Table 5. The INTSEL4–INTSEL9 fields correspond to the CPU interrupts INT4–INT9. By setting the INTSEL bits to the value of the desired interrupt selection number, you can map any interrupt source to any CPU interrupt. The default values of the INTSEL bits are shown in Figure 2. The default mapping of interrupt sources to CPU interrupts for the C620x/C670x devices are shown in Table 6 (page 13). For the default mapping of interrupt sources to CPU interrupts for the C621x/C671x and C64x devices, see the device-specific datasheet.

Figure 1. Interrupt Multiplexer High Register (MUXH)

31	30 – 26	25 – 21	20 – 16
Reserved	INTSEL15	INTSEL14	INTSEL13
R-0	R/W-0 0010	R/W-0 0001	R/W-0 0000

15	14 – 10	9 – 5	4 – 0
Reserved	INTSEL12	INTSEL11	INTSEL10
R-0	R/W-0 1011	R/W-0 1010	R/W-0 0011

Legend: R = Read only; R/W = Read/Write; -*n* = value after reset

Table 4. Interrupt Multiplexer High Register (MUXH) Field Descriptions

Bit	***field***†	***symval***†	Value	Description
31	Reserved	–	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
30–26	INTSEL15	OF(*value*)	0–1Fh	Interrupt selector 15 bits. This value maps interrupt 15 to any CPU interrupt.
25–21	INTSEL14	OF(*value*)	0–1Fh	Interrupt selector 14 bits. This value maps interrupt 14 to any CPU interrupt.
20–16	INTSEL13	OF(*value*)	0–1Fh	Interrupt selector 13 bits. This value maps interrupt 13 to any CPU interrupt.
15	Reserved	–	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
14–10	INTSEL12	OF(*value*)	0–1Fh	Interrupt selector 12 bits. This value maps interrupt 12 to any CPU interrupt.
9–5	INTSEL11	OF(*value*)	0–1Fh	Interrupt selector 11 bits. This value maps interrupt 11 to any CPU interrupt.
4–0	INTSEL10	OF(*value*)	0–1Fh	Interrupt selector 10 bits. This value maps interrupt 10 to any CPU interrupt.

† For CSL implementation, use the notation IRQ_MUXH_INTSEL*n_symval*

Figure 2. Interrupt Multiplexer Low Register (MUXL)

31	30 26	25 21	20 16
Reserved	INTSEL9	INTSEL8	INTSEL7
R-0	R/W-0 1001	R/W-0 1000	R/W-0 0111

15	14 10	9 5	4 0
Reserved	INTSEL6	INTSEL5	INTSEL4
R-0	R/W-0 0110	R/W-0 0101	R/W-0 0100

Legend: R = Read only; R/W = Read/Write; -*n* = value after reset

Table 5. Interrupt Multiplexer Low Register (MUXL) Field Descriptions

Bit	***field***†	***symval***†	Value	Description
31	Reserved	–	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
30–26	INTSEL9	OF(*value*)	0–1Fh	Interrupt selector 9 bits. This value maps interrupt 9 to any CPU interrupt.
25–21	INTSEL8	OF(*value*)	0–1Fh	Interrupt selector 8 bits. This value maps interrupt 8 to any CPU interrupt.
20–16	INTSEL7	OF(*value*)	0–1Fh	Interrupt selector 7 bits. This value maps interrupt 7 to any CPU interrupt.
15	Reserved	–	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
14–10	INTSEL6	OF(*value*)	0–1Fh	Interrupt selector 6 bits. This value maps interrupt 6 to any CPU interrupt.
9–5	INTSEL5	OF(*value*)	0–1Fh	Interrupt selector 5 bits. This value maps interrupt 5 to any CPU interrupt.
4–0	INTSEL4	OF(*value*)	0–1Fh	Interrupt selector 4 bits. This value maps interrupt 4 to any CPU interrupt.

† For CSL implementation, use the notation IRQ_MUXL_INTSEL*n_symval*

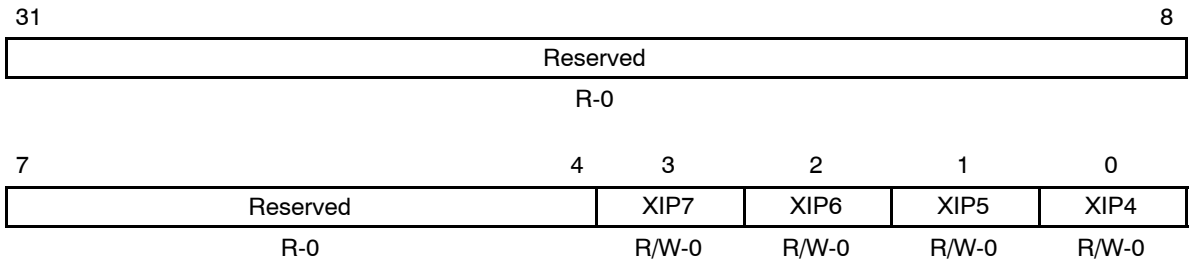
Table 6. TMS320C620x/C670x DSP Default Interrupt Mapping

CPU Interrupt	Related INTSEL field	INTSEL Reset Value	Interrupt Acronym	Interrupt Description
INT4	INTSEL4	0 0100b	EXT_INT4	External interrupt pin 4
INT5	INTSEL5	0 0101b	EXT_INT5	External interrupt pin 5
INT6	INTSEL6	0 0110b	EXT_INT6	External interrupt pin 6
INT7	INTSEL7	0 0111b	EXT_INT7	External interrupt pin 7
INT8	INTSEL8	0 1000b	DMA_INT0	DMA Channel 0 Interrupt
INT9	INTSEL9	0 1001b	DMA_INT1	DMA Channel 1 interrupt
INT10	INTSEL10	0 0011b	SD_INT	EMIF SDRAM timer interrupt
INT11	INTSEL11	0 1010b	DMA_INT2	DMA Channel 2 interrupt
INT12	INTSEL12	0 1011b	DMA_INT3	DMA Channel 3 interrupt
INT13	INTSEL13	0 0000b	DSPINT	Host port to DSP interrupt
INT14	INTSEL14	0 0001b	TINT0	Timer 0 interrupt
INT15	INTSEL15	0 0010b	TINT1	Timer 1 interrupt

5.3 External Interrupt Polarity Register (EXTPOL)

The external interrupt polarity register (EXTPOL) allows you to change the polarity of the four external interrupts (EXT_INT4−EXT_INT7). The EXTPOL is shown in Figure 3 and described in Table 7. When the XIP bit is its default value of 0, a low-to-high transition on an interrupt source is recognized as an interrupt. By setting the corresponding XIP bit to 1, you can invert the external interrupt source and effectively have the CPU detect high-to-low transitions of the external interrupt. Changing an XIP bit value creates transitions on the related CPU interrupt (INT4−INT7) that the external interrupt (EXT_INT) is selected to drive. For example, if XIP4 is changed from 0 to 1 and EXT_INT4 is low or if XIP4 is changed from 1 to 0 and EXT_INT4 is high, the CPU interrupt that is mapped to EXT_INT4 becomes set. EXTPOL only affects interrupts to the CPU and has no effect on DMA events.

Figure 3. External Interrupt Polarity Register (EXTPOL)



Legend: R = Read only; R/W = Read/Write; -*n* = value after reset

Table 7. External Interrupt Polarity Register (EXTPOL) Field Descriptions

Bit	Field	*symval*†	Value	Description
31−4	Reserved	−	0	Reserved. The reserved bit location is always read as 0. A value written to this field has no effect.
3−0	XIP	OF(*value*)	0−Fh	External interrupt polarity bits. A 4-bit unsigned value used to change the polarity of the four external interrupts (EXT_INT4 to EXT_INT7).
			0	A low-to-high transition on an interrupt source is recognized as an interrupt.
			1	A high-to-low transition on an interrupt source is recognized as an interrupt.

† For CSL implementation, use the notation IRQ_EXTPOL_XIP_*symval*

Revision History

Table 8 lists the changes made since the previous version of this document.

Table 8. Document Revision History

Page	Additions/Modifications/Deletions
7	Changed second sentence in Section 2: See the device-specific datasheet for a list of the available interrupts on the C621x/C671x DSP and C64x™ DSP.
9	Deleted Table 3, *TMS320C621x/C671x DSP Available Interrupts*.
10	Deleted Table 4, *TMS320C64x DSP Available Interrupts*. Subsequent tables renumbered.
10	Changed last two sentences in Section 5.1: By setting the INTSEL bits to the value of the desired interrupt selection number, you can map any interrupt source to any CPU interrupt. The default values of the INTSEL bits are shown in Figure 1. The default mapping of interrupt sources to CPU interrupts for the C620x/C670x devices are shown in Table 6 (page 13). For the default mapping of interrupt sources to CPU interrupts for the C621x/C671x and C64x devices, see the device-specific datasheet.
10	Changed last two sentence in Section 5.2: By setting the INTSEL bits to the value of the desired interrupt selection number, you can map any interrupt source to any CPU interrupt. The default values of the INTSEL bits are shown in Figure 2. The default mapping of interrupt sources to CPU interrupts for the C620x/C670x devices are shown in Table 6 (page 13). For the default mapping of interrupt sources to CPU interrupts for the C621x/C671x and C64x devices, see the device-specific datasheet.
13	Changed Table 6 to TMS320C620x/C670x DSP only.

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