TI Designs

Communication Module Reference Design for Functional Isolated RS-485, CAN, and I2C Data Transmission

Description

The TIDA-01281 design is a low-cost, high-efficiency, isolated RS-485, I2C, and CAN communication module solution intended for use in industrial systems such as uninterruptible power supplies (UPS) and energy storage banks that require isolated communication and isolated power for RS-485, I2C, and CAN transceivers.

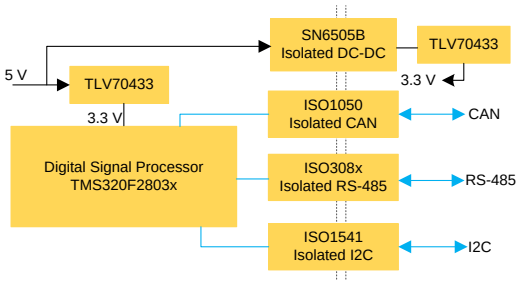
The design has an onboard C2000™ Piccolo™ microcontroller to handle communications protocol for each interface. The board has a built-in, low component count, high-efficiency, primary-side controlled isolated power supply to generate secondary power for communication transceivers.

The TIDA-01281 design is tested for data transmissions under various conditions and in EFT and ESD environments, highlighting the performance of TI devices for robust data transmission in harsh environments.

Resources

TIDA-01281	Design Folder
TMS320F28033	Product Folder
TLV70433	Product Folder
SN6505B	Product Folder
ISO1050	Product Folder
ISO3082	Product Folder
ISO1541	Product Folder

TI E2E™ Community — ASK Our E2E Experts

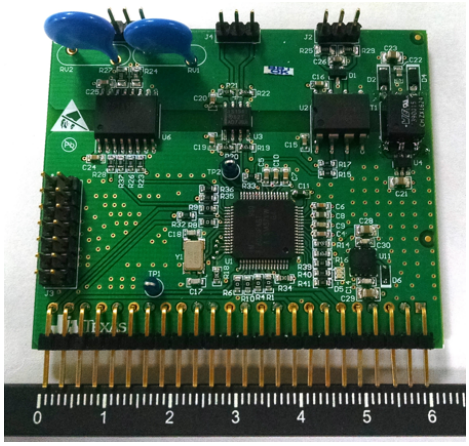


Features

- Simple, Efficient, and Flexible Isolated Communication Module for RS-485, I2C, and CAN Interfaces
- Robust Isolation Performance for Reliable Operation in Harsh Environments Meeting Functional Isolation and Immunity of 4000-V_{PK} and 2500-V_{RMS}, 560-V_{PK} Working Voltage
- Common Mode Transient Immunity (CMTI) of 50 kV/µs for High Immunity in Noisy Environments
- Built-in Compact, Low Emission, >87% Efficiency Isolated Supply to Power Isolated-Side Circuit
- Meets IEC-61000-4-2: ESD ±8-kV Contact, IEC-61000-4-4: EFT ±2-kV RS-485 and ±1 kV for CAN
- Low Component Count and Cost-Optimized Solution Supporting Operation From 3- to 5-V Supply Range
- Standalone Control Card With Analog and Digital Interface of C2000™ Device for Test and Validation of Power Stages Used in UPS Systems, Telecom Rectifiers, Server PSUs, and Battery Management Systems

Applications

- Uninterruptible Power Supplies (UPS)
- Server PSUs and Telecom Rectifiers
- Industrial Power Supplies
- Energy Storage Banks
- Battery Management Systems



1 System Overview

1.1 System Description

Uninterruptible power supply (UPS) systems provide uninterrupted, reliable, and high quality power for vital loads such as medical facilities, life supporting systems, data storage and computer systems, telecommunications, and industrial processing. UPS systems protect sensitive loads against power outages, overvoltage, and undervoltage conditions as well as suppress line transients and harmonic disturbances.

Communications in current generation UPS systems are invaluable and crucial due to multiple reasons: communication is not only used for handling mains disturbance events, but also for providing data for improved load management efficiency, preventative maintenance, and failure diagnostics.

A typical block diagram of an online UPS (double conversion UPS) is shown in Figure 1:

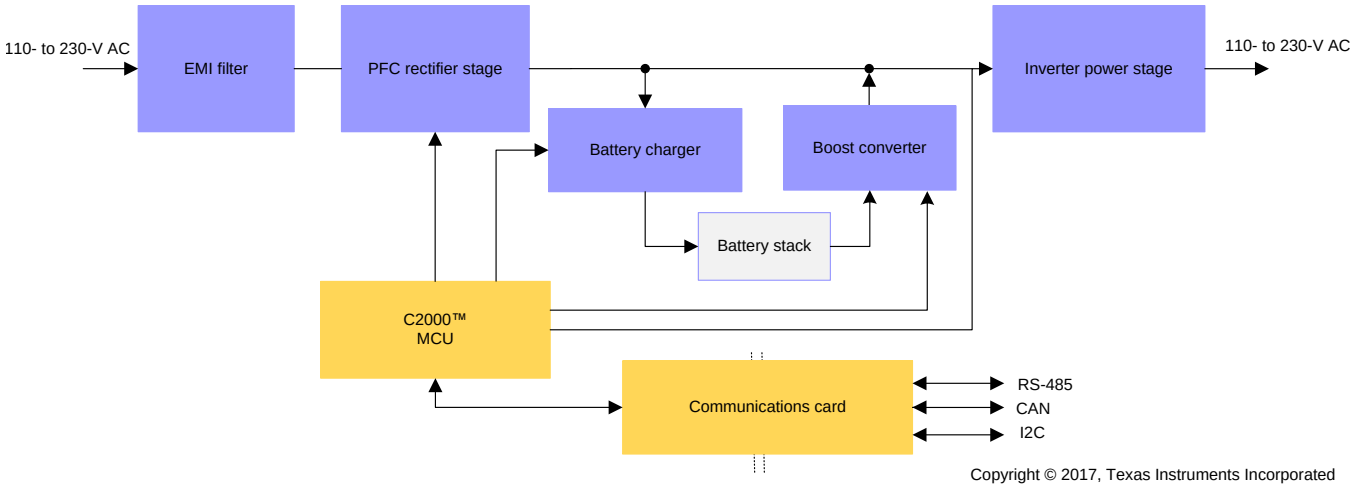


Figure 1. System Block Diagram of Online UPS System

UPS systems need to communicate and broadcast basic parameters such as inverter output voltage, output current, frequency, kVA and kW, battery voltage, charge and discharge current and remaining battery life, statistics regarding mains failures, and UPS operation to close by enterprise network and to HMI display modules. As enterprise units and broadcast modules are located far from UPS systems, an RS-485 or RS-422 link is used to achieve longer communication distances.

In addition, UPS systems need continuous real-time monitoring of the unit and health statistics communication between multiple UPS systems for operations such as balancing the power delivered by each unit when operating in parallel and activating a redundant unit during critical failure of the systems. CAN communication is commonly used for these operations.

Further, a two-wire serial interface, I2C, is used for inter-communication between multiple cards and multiple modules within a UPS system.

The TIDA-01281 design provides a tested and validated platform to implement the following communication interfaces: RS-485, I2C, and CAN.

To achieve a robust data communications link in harsh industrial environments, each of the communication ports must provide an isolated interface between the cable network and the connected systems to protect against voltage spikes and ground loops within the noisy environment and improve system reliability.

This TI Design provides power isolation for the communication link by using an isolated DC-DC power supply using the SN6505B, whereas signal isolation of the communication link is built into each of the transceivers (RS-485, I2C, and CAN) through capacitive isolation technology, which incorporates an integrated SiO2 dielectric capacitor.

The TIDA-01281 is tested for data transmissions under various conditions and is validated for working in EFT and ESD environments that meet IEC-61000 standards. This TI Design can also be used in systems such as telecom rectifiers, industrial rectifiers, energy storage systems, and energy management units, all which need these communication interfaces.

In addition to these communication abilities, the module can be used as an independent control card to control multiple power stages commonly used in UPS systems, telecom rectifiers, server PSUs, and battery management systems as analog and digital interfaces of the C2000 device, which are provided on the connector pins.

1.2 Key System Specifications

Table 1. Key System Specifications

NAME	DESCRIPTION
COMMUNICATION	
SPI (RS-485)	3-wire , up to 200 kbps (half duplex)
CAN interface (I2C)	Bidirectional data , up to 1 Mbps
I2C interface (I2C)	Bidirectional data , clock up to 1 MHz
Transient protection	
ESD for RS-485 and CAN	IEC 61000-4-2, Level-4 (±8 kV), contact discharge, indirect discharge by HCP and VCP
EFT (RS-485)	IEC 61000-4-4, Level-4 (±2 kV); IEC62040-2, Class B
EFT (CAN)	IEC 61000-4-4, Level-3 (±1 kV); IEC62040-2, Class B
AUXILIARY SUPPLY (PUSH-PULL CONVERTER)	
Input voltage	4.2 to 6.0 V (with LDO), 3.3 V (without LDO)
Output voltage	5.0 V (without LDO)
Power output	1 W
Efficiency	> 85%

1.3 Block Diagram

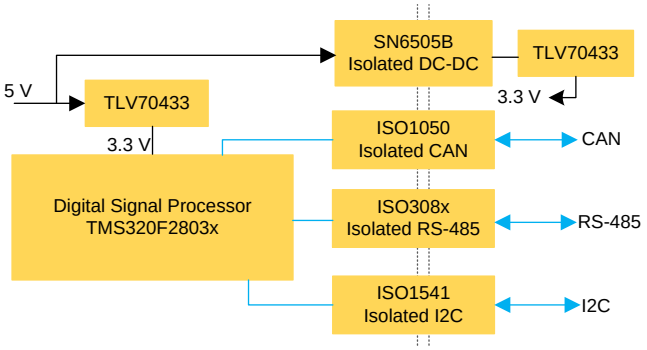


Figure 2. Block Diagram for TIDA-01281

Figure 2 shows the high-level block diagram of the TIDA-01281 design. The highlighted parts used in this TI Design are explained in the following subsections.

1.4 Highlighted Products

1.4.1 TMS320F28035

The F2803x Piccolo™ family of microcontrollers provides power to the C28x core and control law accelerator (CLA) coupled with highly integrated control peripherals in low pin-count devices. This family is code-compatible with previous C28x-based code and provides a high level of analog integration. An internal voltage regulator allows for single-rail operation. Enhancements have been made to the high resolution pulse width modulator (HRPWM) to allow for dual-edge control (frequency modulation). Analog comparators with internal 10-bit references have been added and can be routed directly to control the PWM outputs. The ADC converts from a 0- to 3.3-V fixed full-scale range and supports ratio-metric V_{REFHI}/V_{REFLO}. The ADC interface has been optimized for low overhead and latency.

This device supports all three serial communication peripherals (serial communication interface (SCI) port (UART), enhanced controller area network (eCAN), and I2C) used for RS-485 communication in this TI Design. These communication peripherals feature the following:

- SCI module:
  - Two external pins:
    1. SCITXD: SCI transmit-output pin
    2. SCIRXD: SCI receive-input pin
  - Baud rate programmable to 64K different rates:

$$\text{Baud rate} = \frac{\text{LSPCLK}}{(\text{BRR} + 1) \times 8} \quad \text{when BRR} \neq 0$$

$$\text{Baud rate} = \frac{\text{LSPCLK}}{16} \quad \text{when BRR} = 0$$

  - Data-word format:
    - One start bit
    - Data word length programmable from one to eight bits
    - Optional even/odd/no parity bit
    - One or two stop bits
  - Four error detection flags: parity, overrun, framing, and break detection
  - Two wake-up multiprocessor modes: idle-line and address bit
  - Half- or full-duplex operation
  - Double-buffered receive and transmit functions
  - Transmitter and receiver operations can be accomplished through interrupt-driven or polled algorithms with status flags:
    - Transmitter: TXRDY flag (transmitter-buffer register is ready to receive another character) and TX EMPTY flag (transmitter-shift register is empty)
    - Receiver: RXRDY flag (receiver-buffer register is ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR flag (monitoring four interrupt conditions)
  - Separate enable bits for transmitter and receiver interrupts (except BRKDT)
  - Non-return-to-zero (NRZ) format
- eCAN module:
  - Fully compliant with ISO11898-1 (CAN 2.0B)
  - Supports data rates up to 1 Mbps
  - Thirty-two mailboxes, each with the following properties:
    - Configurable as receive or transmit
    - Configurable with standard or extended identifier
    - Has a programmable receive mask

- Supports data and remote frame
- Composed of 0 to 8 bytes of data
- Uses a 32-bit time stamp on receive and transmit message
- Protects against reception of new message
- Holds the dynamically programmable priority of transmit message
- Employs a programmable interrupt scheme with two interrupt levels
- Employs a programmable alarm on transmission or reception time-out

– Low-power mode
– Programmable wake-up on bus activity
– Automatic reply to a remote request message
– Automatic retransmission of a frame in case of loss of arbitration or error
– 32-bit local network time counter synchronized by a specific message (communication in conjunction with mailbox 16)
– Self-test mode: Operates in a loopback mode receiving its own message. A "dummy" acknowledge is provided, thereby eliminating the need for another node to provide the acknowledge bit.

- I2C module:
  – Compliance with the Philips Semiconductors I2C-bus specification (version 2.1):
    - Support for 1- to 8-bit format transfers
    - 7- and 10-bit addressing modes
    - General call
    - START byte mode
    - Support for multiple master transmitters and slave receivers
    - Support for multiple slave transmitters and master receivers
    - Combined master transmit/receive and receive/transmit mode
    - Data transfer rate of from 10 to 400 kbps (I2C fast-mode rate)
  – One four-word receive FIFO and one four-word transmit FIFO
  – One interrupt that can be used by the CPU. This interrupt can be generated as a result of one of the following conditions:
    - Transmit-data ready
    - Receive-data ready
    - Register-access ready
    - No-acknowledgment received
    - Arbitration lost
    - Stop condition detected
    - Addressed as slave
  – An additional interrupt that can be used by the CPU when in FIFO mode
  – Module enable and disable capability
  – Free data format mode

1.4.2 ISO3082 Isolated 5-V Half-Duplex RS-485 Transceiver

The ISO3082 is an isolated half-duplex differential line transceiver for TIA/EIA RS-485 and RS-422 applications. This device is ideal for long transmission lines because the ground loop is broken to allow for a much larger common-mode voltage range. The symmetrical isolation barrier of the device is tested to provide 2500 V_{RMS} of isolation for 60 seconds per UL 1577 between the bus-line transceiver and the logic-level interface.

Any cabled I/O can be subjected to electrical noise transients from various sources. These noise transients can damage the transceiver or nearby sensitive circuitry if they are large or long enough. These isolated devices can significantly increase protection and reduce this risk to expensive control circuits.

Key features of the ISO3082 include:

- Meets or exceeds TIA/EIA RS-485 requirements
- Signaling rates up to 20 Mbps
- 1/8 unit load; Up to 256 nodes on a bus
- Thermal s0hutdown protection
- Low bus capacitance: 16 pF (typical)
- 50-kV/μs typical transient immunity
- Fail-safe receiver for bus open, short, idle
- 3.3-V inputs are 5-V tolerant
- Bus-pin ESD protection:
  - 12-kV HBM between bus pins and GND2
  - 6-kV HBM between bus pins and GND1
- Safety and regulatory approvals
  - 4000-V_{PK} basic insulation, 560-V_{PK} V_{IORM} per DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 and DIN EN 61010-1
  - 2500-V_{RMS} isolation per UL 1577
  - 4000-V_{PK} isolation per CSA component acceptance notice 5A and IEC 60950-1

1.4.3 ISO1050 Isolated CAN Transceiver

The ISO1050 is a galvanically isolated CAN transceiver that meets the specifications of the ISO11898-2 standard. The device has the logic input and output buffers separated by a silicon oxide (SiO2) insulation barrier that provides galvanic isolation of up to 5000 V_{RMS} for ISO1050DW and 2500 V_{RMS} for ISO1050DUB. Used in conjunction with isolated power supplies, the device prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

As a CAN transceiver, the device provides differential transmit capability to the bus and differential receive capability to a CAN controller at signaling rates up to 1 Mbps. The device is designed for operation in especially harsh environments, and it features cross-wire, overvoltage and loss of ground protection from –27 to 40 V and over-temperature shutdown, as well as -12-V to 12-V common-mode range.

Key features of the ISO1050 include:

- Meets ISO11898-2 requirements
- 5000-V_{RMS} isolation (ISO1050DW)
- 2500-V_{RMS} isolation (ISO1050DUB)
- Fail-safe outputs
- Low loop delay: 150 ns (typical), 210 ns (maximum)
- 50-kV/μs typical transient immunity
- Bus-fault protection of –27 to 40 V
- Driver (TXD) dominant time-out function
- I/O voltage range supports 3.3-V and 5-V microprocessors
- VDE approval per DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12 and DIN EN 61010-1
- UL 1577 approved
- CSA approved for IEC 60950-1, IEC 61010-1, IEC 60601-1 3rd Ed (medical), and Component Acceptance Notice 5A
- TUV 5-kV_{RMS} reinforced insulation approval for EN/UL/CSA 60950-1 (ISO1050DW only)
- CQC reinforced insulation per GB4843.1-2011 (ISO1050DW only)
- Typical 25-year life at rated working voltage

1.4.4 ISO1541 Low-Power Bidirectional I2C Isolator

The ISO1541 is a low-power, bidirectional isolator that is compatible with an I2C interface. This device has its input and output buffers separated by TI's capacitive isolation technology using a silicon dioxide (SiO2) barrier. When used with isolated power supplies, this device blocks high voltages, isolate grounds, and prevents noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

This isolation technology provides for function, performance, size, and power consumption advantages when compared to optocouplers. The ISO1541 enables a complete isolated I2C interface to be implemented within a small form factor. This device has a bidirectional data and a unidirectional clock channel. Isolated bidirectional communication is accomplished within these devices by offsetting the Side 1 Low-level Output to a value greater than the Side 1 High-Level Input voltage, thus preventing an internal logic latch that otherwise would occur with standard digital isolators.

Key features of the ISO1541 include:

- Isolated bidirectional, I2C compatible communication
- Supports up to 1-MHz operation
- 3- to 5.5-V supply range
- Open-drain outputs with 3.5-mA Side 1 and 35-mA Side 2 sink current capability
- –40°C to 125°C operating temperature
- ±50-kV/μs transient immunity (typical)
- HBM ESD protection of 4 kV on all pins; 8 kV on bus pins
- Safety and regulatory approvals:
  - 4242-V_{PK} isolation per DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
  - 2500-V_{RMS} isolation for 1 minute per UL 1577
  - CSA component acceptance notice 5A, IEC 60950-1 and IEC 61010-1 end equipment standards
  - CQC basic insulation per GB4943.1-2011

2 Communication in Power Supplies

A power supply system is inadequate without proper communication. A power system is made smart by adding two-way communication. This communication enables utilities to achieve three key objectives: intelligent monitoring, security, and load balancing.

The communication must be reliable, secure, and low cost. In most situations, it is useful for a single large UPS to be able to communicate with several protected devices. Communication in power system is also required to monitor various performance and safety critical parameters such as peak input and output current, feedback voltage, frequency, and other parameters to check for fault conditions and take necessary actions.

Industrial serial interfacing are areas where noise can seriously affect the integrity of data transfers. A tested method of improving noise performance for any interface circuit is galvanic isolation. Isolation in data communication systems is achieved without direct galvanic connection (wires) between drivers and receivers. Magnetic linkage from transformers provides the power for the system, and TI's capacitively-coupled digital isolators provide the data connection. Galvanic isolation removes ground-loop currents, and the resulting noise voltage that corrupts data is eliminated. Also, common-mode noise effects and many forms of radiated noise can be reduced to negligible limits using this technique. Unwanted currents and voltages on a cable bus connecting multiple systems could potentially cause severe problems. High voltages and currents can destroy components connected to the bus. To protect against this potentially destructive energy, all communication devices for this design are isolated.

2.1 Serial Communication: RS-485

The RS-485 communication standard enables highly robust data transmission over a long distance and electrically noisy environment by using a balanced differential bus line over a twisted pair cable with 120-Ω characteristic impedance. The RS-485 bus standard is one of the most widely used physical layer bus design in industrial applications. The key features of RS-485 that make it ideal for industrial communication applications include:

- Balanced interface
- Long distance links up to 4000 feet at 100 kbps and 40 feet at 10 Mbps
- Bidirectional communications possible over a single pair of twisted cables
- Differential transmission increases noise immunity and decreases noise emissions
- Multiple drivers and receivers can be connected on the same bus and can support up to 32 unit loads
- Wide common-mode range allows for differences in ground potential between the driver and receiver
- TIA/EIA-485 allow for data rates of up to 10 Mbps. Devices meeting the TIA/EIA-485 specifications do not have to operate over the entire range and are not limited to 10 Mbps.
- Multipoint operation from a single 5-V supply and –7- to 12-V bus common-mode range

In harsh and noisy environments such as multi-unit residential buildings or industrial settings, an RS-485 bus architecture can be used to implement a low-cost yet robust communications network. The differential nature of RS-485 signaling makes it less susceptible to external interference. Moreover, the RS-485 specification supports multidrop configurations, thus allowing the connection of multiple meters to a single bus. The best practice for RS-485 networks specifies 120 Ω of termination on each end of the RS-485 bus to reduce signal reflections.

The RS-485 standard specifies the minimum bus signal levels during data transmission. A driver must provide at least a 1.5-V differential over a 54-Ω load, and a receiver must detect a differential input of at least 200 mV. These provides a sufficient margin for a reliable data transmission even under severe signal degradation across the cable and connectors. High- and low-logic states on an RS-485 bus are represented by a positive or negative differential voltage. Figure 3 shows the standard specified bus signal levels for RS-485.

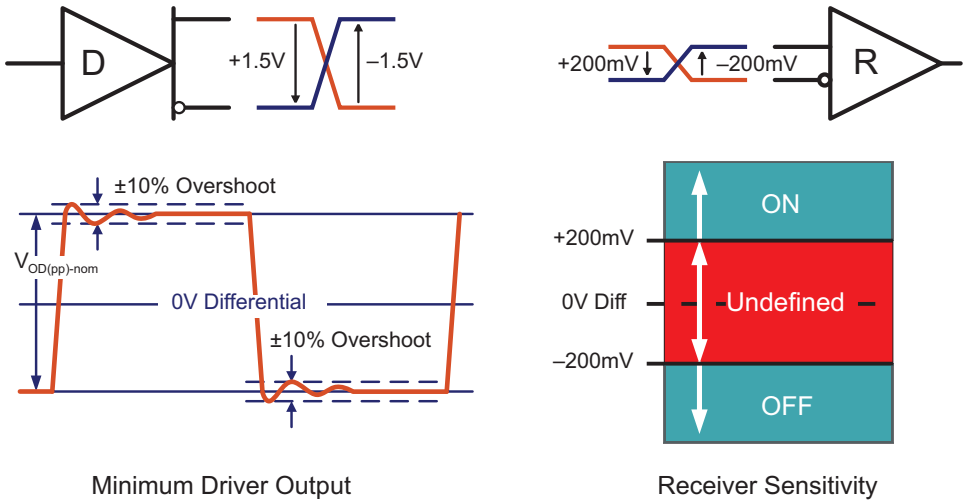


Figure 3. RS-485 Specified Bus Signal Levels

2.1.1 TI's Solution for RS-485: ISO3082

The ISO3082 is an isolated half-duplex differential line transceiver for TIA/EIA RS-485 and RS-422 applications. This device is rated to provide galvanic isolation of up to 2500 V_{RMS} for 60 seconds as per the standard. It has active-high driver enable and active-low receiver enable to control the data flow. The ISO3082 is suitable for low data transmission up to 200 kbps. The ISO3088 is also provided by TI, which is pin compatible with the ISO3082 and supports data rate up to 20Mbps.

When the receiver enable pin, RE, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_{(A)} – V_{(B)}$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and less than the negative and lower than the negative input threshold, $V_{IT–}$, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and $V_{IT–}$, the output is indeterminate. When RE is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus). The functional diagram of the ISO3082 is shown in Figure 4 .

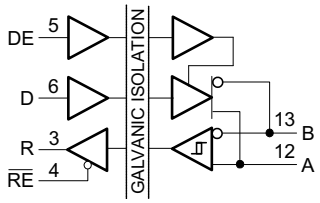


Figure 4. ISO3082 Functional Block Diagram

2.1.2 Transient Protection

This TI Design features a very robust three-stage protection scheme. A TVS diode is implemented on each bus line along with series pulse proof resistors, metal oxide varistors (MOVs), and a transient blocking unit (TBU) protecting the RS-485 transceiver from lethal ESD, EFT, and surge during handling, interruption of inductive loads, relay contact bounce, and lightning strikes. Without protection, if the energy that is delivered during one of these transient events is large enough in amplitude, it can permanently damage the device.

The TVS diode acts as a clamping circuit that redirects the transient energy to ground and away from the transceiver while the pulse-proof resistors act as a current limiter to protect the transceiver from dangerous overvoltage conditions. The MOV protects the Bourns TBU® from exposure to excessive transient voltage, clamping or crowbarring the transient to a level less than the impulse. When the transient current exceeds the TBU trigger current limit, the sub-microsecond response of the TBU limits the current flow to the transceiver. The MOV reduces the transients to a few hundred volts of clamping voltage while the TBUs limit transient current to less than 1 mA. Figure 5 shows the RS-485 transceiver with all of its components:

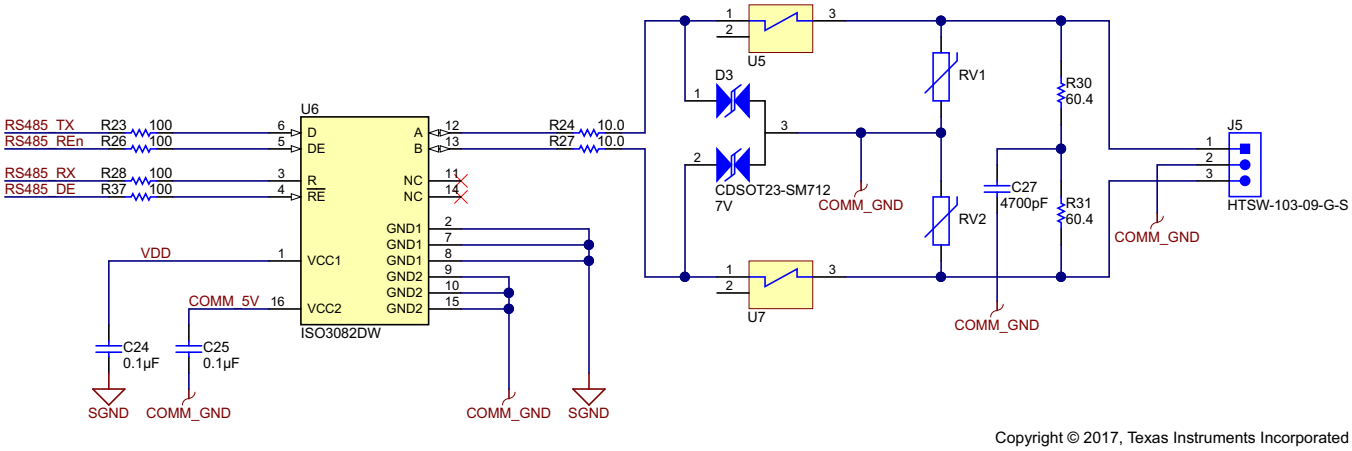


Figure 5. RS-485 Transceiver With Transient Protection Circuit

2.2 I2C

I2C is a simple, low-bandwidth, short-distance protocol. Most available I2C devices operate at speeds up to 400 kbps, with some venturing up into the low megahertz range. I2C can easily link multiple devices together because it has a built-in addressing scheme. I2C is open-drain topology, requiring two lines, serial data (SDA), and serial clock (SCL), to be connected to VDD by pull-up resistors. To have logic zero online, pull the line to ground (an operating MOSFET). To have logic one, let the line float (a not-operating MOSFET) to make it high due to the pullup resistor. Pullup resistors are selected based on recommended drain currents. This design uses 4.7-kΩ pullup resistors.

I2C advantages are:

- Requires only two bus lines (SDA and SCL)
- No strict baud rate requirements, the master generates a bus clock
- Simple master/slave relationships between all components
- Each device connected to the bus is software-addressable by a unique address
- A true multi-master bus providing arbitration and collision detection

2.2.1 Operating Modes

The I2C module has four basic operating modes to support data transfers as a master and as a slave. See Table 2 for the names and descriptions of the modes.

If the I2C module is a master, it begins as a master-transmitter and typically transmits an address for a particular slave. When giving data to the slave, the I2C module must remain a master-transmitter. To receive data from a slave, the I2C module must be changed to the master-receiver mode.

If the I2C module is a slave, it begins as a slave-receiver and typically sends acknowledgment when it recognizes its slave address from a master. If the master will be sending data to the I2C module, the module must remain a slave-receiver. If the master has requested data from the I2C module, the module must be changed to the slave-transmitter mode.

Table 2. Operating Modes of I2C Module

OPERATING MODE	DESCRIPTION
Slave-receiver modes	The I2C module is a slave and receives data from a master. All slaves begin in this mode. In this mode, serial data bits received on SDA are shifted in with the clock pulses that are generated by the master. As a slave, the I2C module does not generate the clock signal, but it can hold SCL low while the intervention of the device is required (RSFULL = 1 in I2CSTR) after a byte has been received.
Slave-transmitter mode	The I2C module is a slave and transmits data to a master. This mode can be entered only from the slave-receiver mode; the I2C module must first receive a command from the master. When you are using any of the 7- or 10-bit addressing formats, the I2C module enters its slave-transmitter mode if the slave address byte is the same as its own address (in I2COAR) and the master has transmitted R/W = 1. As a slave-transmitter, the I2C module then shifts the serial data out on SDA with the clock pulses that are generated by the master. While a slave, the I2C module does not generate the clock signal, but it can hold SCL low while the intervention of the device is required (XSMT = 0 in I2CSTR) after a byte has been transmitted.
Master-receiver mode	The I2C module is a master and receives data from a slave. This mode can be entered only from the master-transmitter mode; the I2C module must first transmit a command to the slave. When you are using any of the 7- or 10-bit addressing formats, the I2C module enters its master-receiver mode after transmitting the slave address byte and R/W = 1. Serial data bits on SDA are shifted into the I2C module with the clock pulses generated by the I2C module on SCL. The clock pulses are inhibited and SCL is held low when the intervention of the device is required (RSFULL = 1 in I2CSTR) after a byte has been received.
Master-transmitter modes	The I2C module is a master and transmits control information and data to a slave. All masters begin in this mode. In this mode, data assembled in any of the 7- or 10-bit addressing formats is shifted out on SDA. The bit shifting is synchronized with the clock pulses generated by the I2C module on SCL. The clock pulses are inhibited and SCL is held low when the intervention of the device is required (XSMT = 0 in I2CSTR) after a byte has been transmitted.

2.2.2 I2C Module START and STOP Conditions

START and STOP conditions can be generated by the I2C module when the module is configured to be a master on the I2C bus. As shown in Figure 6:

- The START condition is defined as a high-to-low transition on the SDA line while SCL is high. A master drives this condition to indicate the start of a data transfer.
- The STOP condition is defined as a low-to-high transition on the SDA line while SCL is high. A master drives this condition to indicate the end of a data transfer.

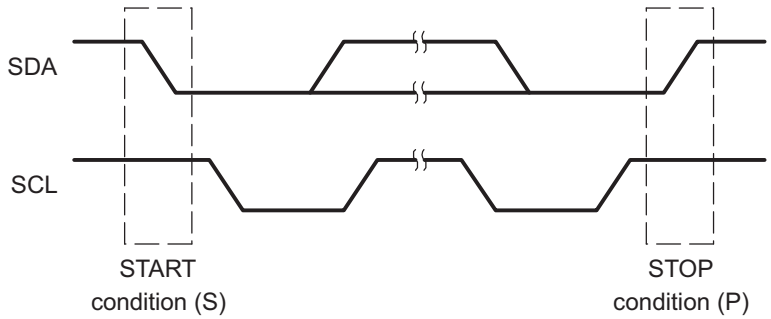


Figure 6. I2C Module START and STOP Conditions

2.2.3 I2C Interface by TI: ISO1541

The ISO1541 is a low-power, bidirectional isolator that is compatible with I2C interfaces. This device has logic input and output buffers separated by TI's capacitive isolation technology using a SiO2 barrier. When used in conjunction with isolated power supplies, this device blocks high voltages, isolates grounds, and prevents noise currents from entering the local ground and interfering with or damaging sensitive circuitry. Figure 7 show the functional diagram for the ISO1541.

This isolation technology provides for function, performance, size, and power consumption advantages when compared to optocouplers. The ISO1541 enables a complete isolated I2C interface to be implemented within a small form factor.

The ISO1541 has a bidirectional data and a unidirectional clock channel. The ISO1541 is useful in applications that have a single master. Isolated bidirectional communication is accomplished within ISO1541 by offsetting the side one low-level output voltage to a value greater than the side one high-level input voltage thus preventing an internal logic latch that otherwise would occur with standard digital isolators.

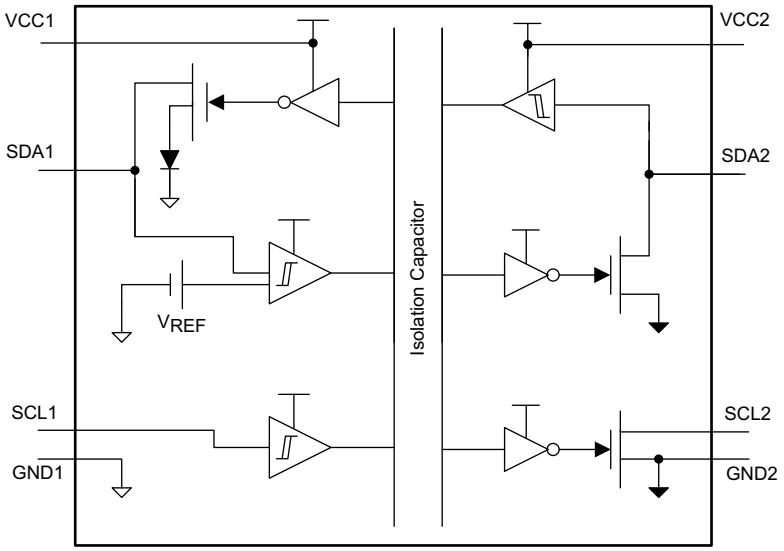


Figure 7. ISO1541 Functional Block Diagram

2.3 CAN

2.3.1 CAN Module

The controller area network (CAN) uses a serial multimaster communication protocol that efficiently supports distributed real-time control, with a very high level of security, and a communication rate of up to 1 Mbps. The CAN bus is ideal for applications operating in noisy and harsh environments such as in the automotive and other industrial fields that require communication.

Prioritized messages of up to eight bytes in data length can be sent on a multimaster serial bus using an arbitration protocol and an error-detection mechanism for a high level of data integrity.

2.3.2 CAN Protocol Overview

The CAN protocol supports four different frame types for communication:

- Data frames that carry data from a transmitter node to the receiver nodes
- Remote frames that are transmitted by a node to request the transmission of a data frame with the same identifier
- Error frames that are transmitted by any node on a bus-error detection
- Overload frames that provide an extra delay between the preceding and the succeeding data frames or remote frames

In addition, CAN specification version 2.0B defines two different formats that differ in the length of the identifier field: standard frames with an 11-bit identifier and extended frames with a 29-bit identifier. CAN standard data frames contain from 44 to 108 bits and CAN extended data frames contain 64 to 128 bits. Furthermore, up to 23 stuff bits can be inserted in a standard data frame, and up to 28 stuff bits in an extended data frame, depending on the data-stream coding. The overall maximum data frame length is then 131 bits for a standard frame and 156 bits for an extended frame.

The bit fields that make up standard or extended data frames, along with their position as shown in Figure 8 include the following:

- Start of frame
- Arbitration field containing the identifier and the type of message being sent
- Control filed indicating the number of bytes being transmitted
- Up to 8 bytes of data
- Cyclic redundancy check (CRC)
- End of frame bits

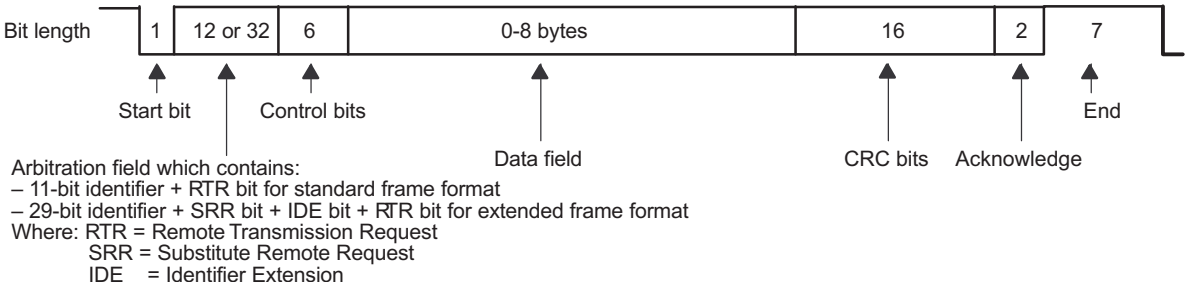


Figure 8. CAN Data Frame

Unless otherwise noted, the numbers are amount of bits in the field.

2.3.3 CAN Module by TI: ISO1050

The ISO1050 is a digitally isolated CAN transceiver with a typical transient immunity of 50 kV/µs. The device can operate from a 3.3-V supply on side 1 and a 5-V supply on side 2. This is particularly advantageous for applications operating in harsh industrial environments because the 3.3 V on side 1 enables the connection to low-volt microcontrollers for power preservation, whereas the 5 V on side 2 maintains a high signal-to-noise ratio of the bus signals. Figure 9 shows the functional diagram of the ISO1050.

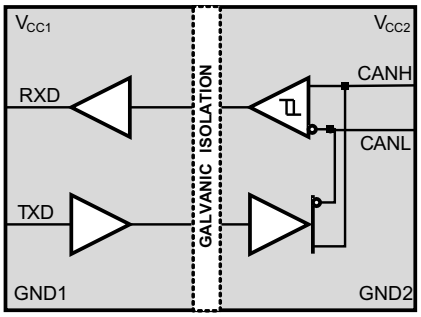


Figure 9. ISO1050 Functional Diagram

The ISO1050 also has incorporated various protection features to make sure fail-safe communication. Various important protection features are:

- TXD Dominant time-out (DTO): TXD DTO circuit prevents the local node from blocking network communication in the event of a hardware or software failure where TXD is held dominant longer than the time-out period t_{TXD_DTO}.
- Thermal shutdown: If the junction temperature of the device exceeds the thermal shutdown threshold (from –55°C to 125°C), the device turns off the CAN driver circuits blocking the TXD to bus transmission path.
- Undervoltage lockout and fail-safe: Protects the bus during an undervoltage event on V_{CC1} or V_{CC2} supply pins by disabling the transceiver to prevent false transmissions due to an unstable supply.
- CAN bus short-circuit current limiting: Limits the short-circuit current when a CAN bus line is shorted

A CAN network design is a series of trade-offs, but these devices operate over wide –12- to 12-V common-mode range. In ISO11898-2, the driver differential output is specified with a 60-Ω load (the two 120-Ω termination resistors in parallel) and the differential output must be greater than 1.5 V. The ISO1050 is specified to meet the 1.5-V requirement with a 60-Ω load, and additionally specified with a differential output of 1.4 V with a 45-Ω load. The differential input resistance of the ISO1050 is a minimum of 30 kΩ. If 167 ISO1050 transceivers are in parallel on a bus, this is equivalent to a 180-Ω differential load. That transceiver load of 180 Ω in parallel with the 60 Ω gives a total 45 Ω. Therefore, the ISO1050 theoretically supports over 167 transceivers on a single bus segment with margin to the 1.2-V minimum differential input at each node. However, for CAN network design margin must be given for signal loss across the system and cabling, parasitic loadings, network imbalances, ground offsets and signal integrity thus a practical maximum number of nodes is typically much lower. Bus length may also be extended beyond the original ISO11898 standard of 40 m by careful system design and data rate tradeoffs. For example, CAN open network design guidelines allow the network to be up to 1 km with changes in the termination resistance, cabling, less than 64 nodes and significantly lowered data rate.

2.3.3.1 CAN Bus States

The CAN bus has two states during operation: dominant and recessive. A dominant bus state, equivalent to logic low, is when the bus is driven differentially by a driver. A recessive bus state is when the bus is biased to a common mode of $V_{CC}/2$ through the high-resistance internal input resistors of the receiver, equivalent to a logic high. The host microprocessor of the CAN node will use the TXD pin to drive the bus and will receive data from the bus on the RXD pin. Figure 10 gives the physical representation of the bus states.

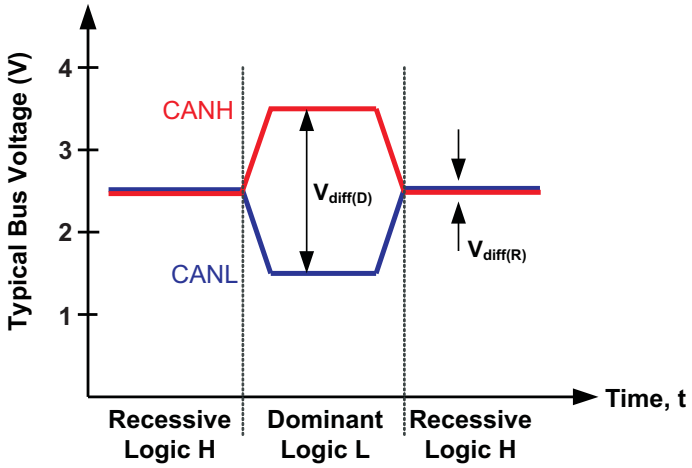


Figure 10. CAN Bus States (Physical Bit Representation)

2.3.3.2 CAN Termination

The ISO11898 standard specifies the interconnect to be a single twisted pair cable (shielded or unshielded) with 120-Ω characteristic impedance (ZO). Resistors equal to the characteristic impedance of the line should be used to terminate both ends of the cable to prevent signal reflections. Unterminated drop-lines (stubs) connecting nodes to the bus should be kept as short as possible to minimize signal reflections. The termination may be in a node, but if nodes may be removed from the bus, the termination must be carefully placed so that it is not removed from the bus.

Termination may be a single 120-Ω resistor at the end of the bus, either on the cable or in a terminating node. If filtering and stabilization of the common mode voltage of the bus is desired, then split termination may be used. Split termination improves the electromagnetic emissions behavior of the network by eliminating fluctuations in the bus common-mode voltages at the start and end of message transmissions. See Figure 11 for CAN bus termination concepts.

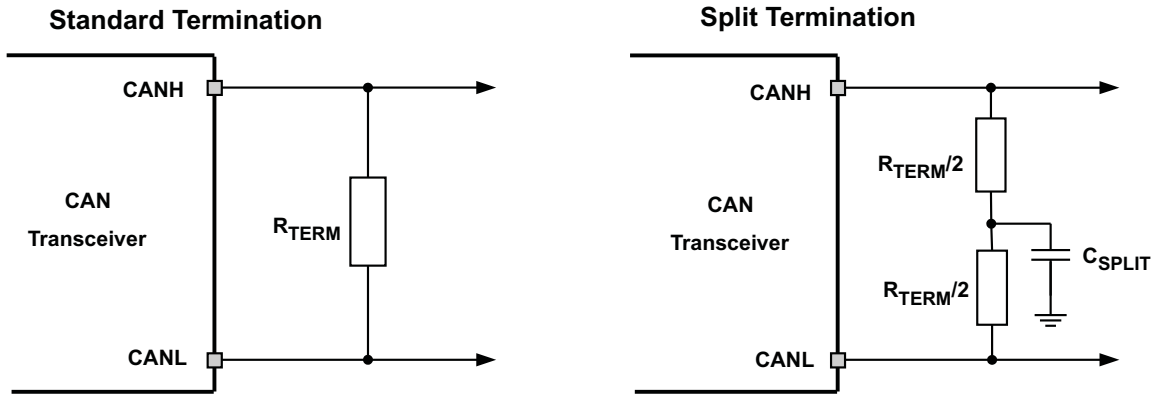


Figure 11. CAN Bus Termination Concepts

2.3.4 Transient Protection

This design implements EFT protection for CAN bus. A TVS diode is implemented on each bus line protecting CAN transceiver from ESD and EFT. The TVS diode acts as a clamping circuit redirecting the transient energy to ground and away from transceiver. Figure 12 shows the protection and termination used for CAN module.

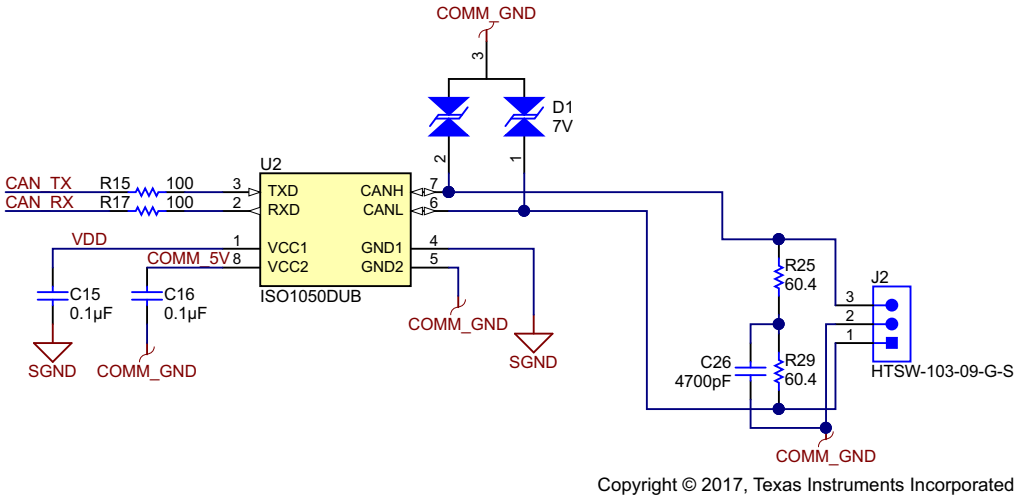


Figure 12. CAN Module Schematic

2.4 Power Stage

All the transceivers used in this TI Design are isolated modules. Thus, in order to provide the isolated power supply, this design uses an isolated auxiliary push-pull power supply. See Figure 13 for the schematic of isolated auxiliary power supply.

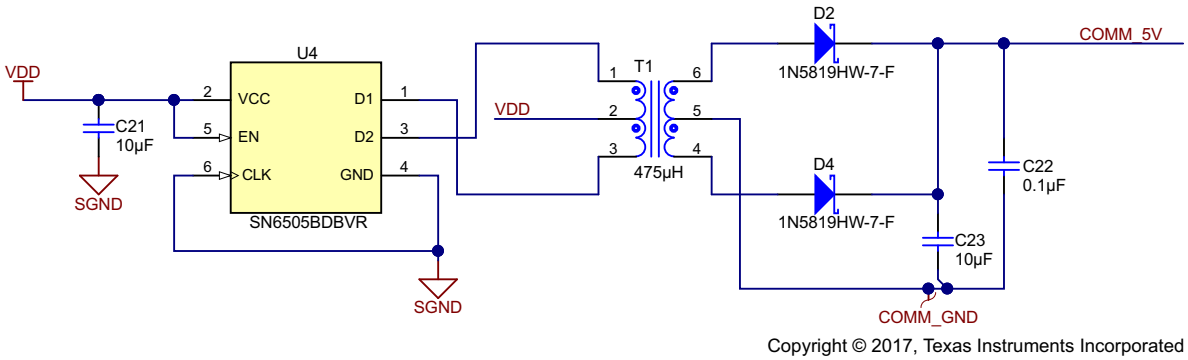


Figure 13. Isolated Power Supply Based on Push-Pull Topology

The auxiliary power supply input and output parameters are mentioned in Table 3:

Table 3. Auxiliary Power Supply Parameters

PARAMETER	SPECIFICATION
V_{IN}	3.3 V
V_{OUT}	5 V
Output power	1 W
Switching frequency	420 kHz

2.4.1 Push-Pull Transformer Design

The important parameters that need to be calculated for the push-pull transformer are:

- Turns ratio (N_S/N_P)
- Volt sec product
- Primary current carrying capability

To calculate the turns ratio, the nominal input voltage is taken to be V_{NOM} = 3.3 V.

Assuming 85% efficiency for the push-pull stage, the primary current I_{PRI} can calculated using Equation 1:

$$I_{pri} = \frac{P_{OUT}}{\left(\eta \times V_{NOM}\right)} = \frac{1}{\left(0.85 \times 3.3\right)} = 357 \text{ mA} \quad (1)$$

The voltage appearing across the primary of the transformer when one of the push-pull FET is switched on is calculated using Equation 2:

$$V_{pri} = V_{NOM} - \left(I_{pri} \times R_{DSon}\right) - \left(I_{pri} \times DCR\right) \quad (2)$$

$$V_{pri} = 3.3 - 0.357 \times \left(0.16 + 0.15\right) = 3.1893 \text{ V}$$

The required reflected voltage across the secondary winding of the transformer is given by Equation 3:

$$V_{sec} = V_{OUT} + V_{f\_drop} \quad (3)$$

$$V_{sec} = 5 + 0.3 = 5.3 \text{ V}$$

From equation Equation 2 and Equation 3, the turns ratio N_S/N_P can be calculated from Equation 4:

$$\frac{N_S}{N_P} = \frac{V_{sec}}{V_{pri}} = \frac{5.3}{3.1893} = 1.7 \quad (4)$$

The minimum required volt-second product, V_{TMIN}, of the transformer can be calculated using Equation 5:

$$V_{Tmin} \geq V_{primax} \times T_{max} \times D_{max} \geq V_{rpimax} \times \frac{D_{max}}{F_{max}} \quad (5)$$

V_{primax} is assumed to be 1.05 times the V_{NOM}. $V_{primax} = 1.05 \times 3.3 = 3.465$ V

Because the SN6505B operates with a fixed duty cycle of 50%, the D_{MAX} is taken as 0.5.

The minimum switching frequency of the SN505B when using the internal oscillator can be obtained from the datasheet (F_{min} = 363 kHz).

By substituting the values in Equation 5: $V_{Tmin} \geq 3.465 \times \frac{0.5}{363000} = 4.77$ Vμs

A transformer from Wurth with 1:1.7 turns ratio is chosen for this TI Design.

2.4.2 Rectifier Diode Selection

To increase the efficiency of the push-pull forward converter, the forward voltage drop of the secondary side rectifier diodes should be as small as possible. Also, as the SN6505B is a high frequency switching converter, the diode must possess a short recovery time. Schottky diodes are selected as they meet these requirements of low forward voltage drop and fast recovery time. The diode must also withstand a reverse voltage of twice the output voltage.

3 Getting Started Hardware

See Figure 14 and Figure 15 for a board picture with its major components marked in red.

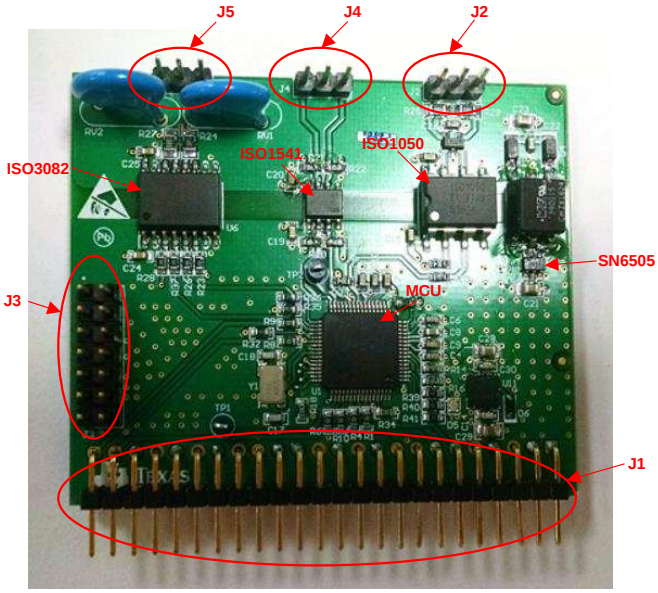


Figure 14. TIDA-01281 Front-Side Board Picture With Major Components

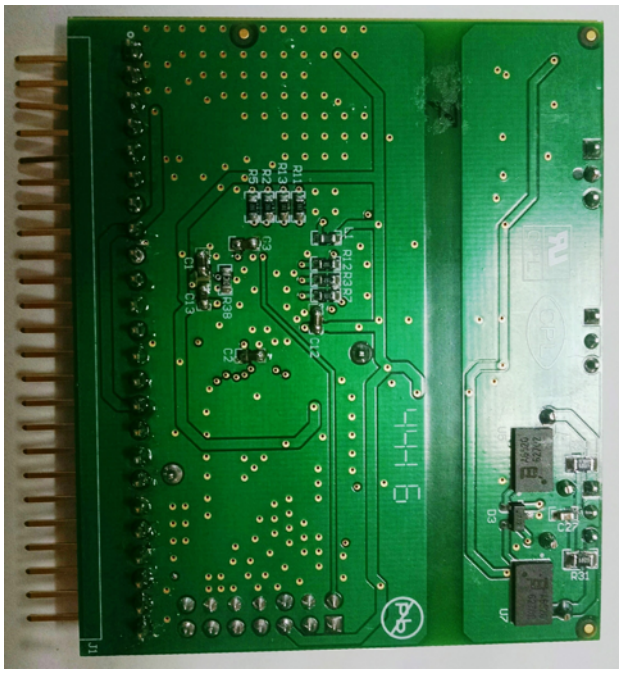


Figure 15. TIDA-01281 Back-Side Picture

3.1 Connectors on Board

There are five connectors on the TIDA-01281 board. Three of the connectors (J2, J4, and J5) are for isolated CAN, I2C, and RS-485 communication, respectively. The connector J1 exposes various GPIO, ADC, PWM, and power supply input and ground pins of the TIDA-01281 board. The connector J3 is the 14 pin JTAG connector required to program the TMS320F28033 controller.

The pin details of each of the connectors are given in the following tables.

Table 4. Connector J1 Details

CONNECTOR J1 PIN NUMBER	FUNCTION	TMS320F28033 PIN
1	ADC/GPIO	13
2	ADC/GPIO	12
3	GND	—
4	ADC/GPIO	11
5	GND	—
6	PWM/GPIO	56
7	PWM/GPIO	54
8	3.3V/5V input	—
9	PWM/GPIO	52
10	ADC/GPIO	10
11	GND	—
12	ADC/GPIO	20
13	GND	—
14	GPIO	49
15	3.3V/5V input	—
16	ADC/GPIO	22
17	GND	—
18	ADC/GPIO	23
19	GND	—
20	GPIO	44
21	GND	—
22	PWM/GPIO	39
23	PWM/GPIO	51
24	PWM/GPIO	35

The connector J3 is the JTAG interface for programming and debugging the onboard TMS320F28033 controller. The connector J3 can be directly used for connecting a standard 14-pin JTAG debugger.

Table 5. Connector J3 Details

CONNECTOR J3 PIN NUMBER	FUNCTION
1	TMS
2	TRST
3	TDI
4	GND
5	VDD
6	NC
7	TDO
8	GND
9	TCK
10	GND
11	TCK
12	GND
13	NC
14	NC

The connector J2 is the isolated CAN interface of the TIDA-01281 board. Its pinout is given in Table 6.

Table 6. Connector J2 Details

CONNECTOR J2 PIN NUMBER	FUNCTION
1	CANL
2	EARTH/GND
3	CANH

The connector J4 is the isolated I2C interface of the TIDA-01281 board. Its pinout is given in Table 7.

Table 7. Connector J4 Details

CONNECTOR J4 PIN NUMBER	FUNCTION
1	SCL
2	EARTH/GND
3	SDA

The connector J5 is the isolated RS-485 interface of the TIDA-01281. Its pinout is given in Table 8.

Table 8. Connector J5 Details

CONNECTOR J5 PIN NUMBER	FUNCTION
1	D–
2	EARTH/GND
3	D+

3.2 Programing the TIDA-01281

In order to test the communication features of the TIDA-01281, the controlSUITE™ and Code Composer Studio™ (CCS) need to be installed on a PC.

controlSUITE provides a cohesive set of software drivers, peripheral examples, and other support information for the C2000 family of devices. CCS is an IDE that supports TI's microcontroller and embedded processors portfolio. More details on the controlSUITE and CCS including where to download them from are provided in Section 6.

For performing the functions tests, the examples provided in controlSUITE for I2C, SCI (RS-485), and the CAN provide a good starting point for studying and only need to be modified slightly.

The TMS320F28033 can be programmed using a XDS-200 JTAG programmer from Spectrum Digital. Figure 16 shows the connection setup for programming the TIDA-01281 boards.

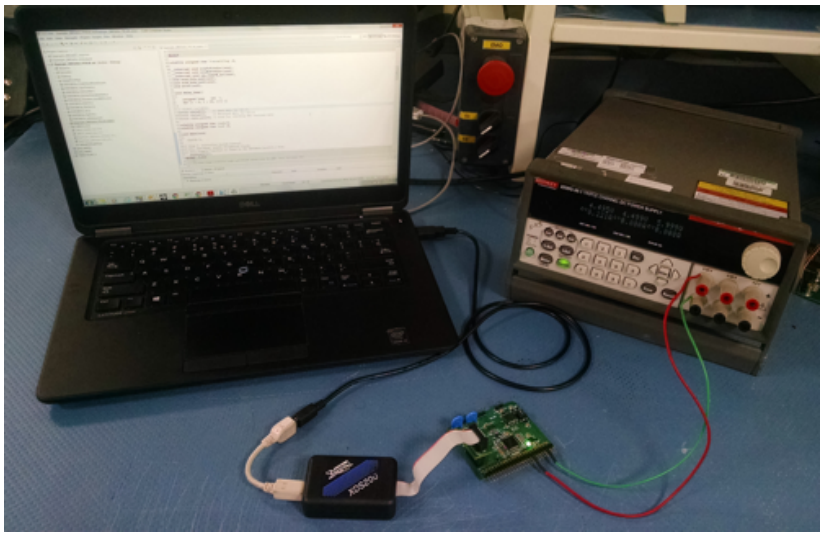


Figure 16. Connection Setup

Apart from the XDS-200, any XDS-100V or a higher capability JTAG emulator like the XDS-510 or XDS-560 also can be used.

3.3 Test Setup

To test the RS-485 and CAN communication features of the TIDA-01281, two TIDA-01281 boards are connected together. One of the boards works as the transmitter and the other board works as the receiver. This arrangement is shown in Figure 17.

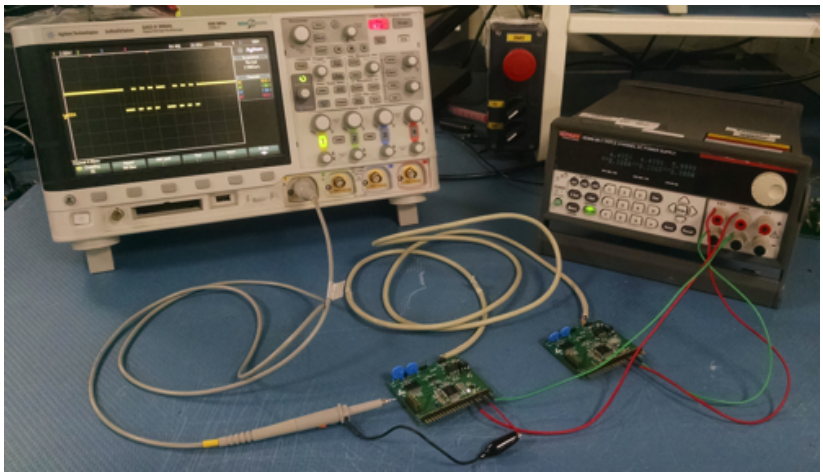


Figure 17. Test Setup

To test I2C communication, an external EEPROM is used. Few bytes of data is written into the EEPROM and read back to verify the communication.

3.3.1 Equipment Needed

Gather the following equipment to test this board:

1. Two DC power supplies capable of supplying up to 250 mA at 5 V
2. A four-channel digital oscilloscope
3. Two TIDA-01281 boards
4. A three-wire shielded cable for communication

3.4 Procedure

3.4.1 Testing RS-485, CAN

Follow this procedure to test the design for RS-485 and CAN:

1. Connect two TIDA-01281 boards using connector J5 to test RS-485 or J2 to test CAN.
2. Connect a regulated DC supply to each board using connector J1 and set it to 5 V.
3. Make one board a RS-485 and CAN transmitter and another board a RS-485 and CAN receiver by programming appropriate firmware into each board.
4. Connect the JTAG emulator to the receiver board to observe the successful communication.

3.4.2 Testing for I2C

Follow this procedure to test the design for I2C:

1. Connect the TIDA-01281 board to an external EEPROM using connector J4.
2. Configure a regulated DC supply to the TIDA-01281 board.
3. Program the I2C firmware into the TIDA-01281. Set the EEPROM's I2C address correctly in the firmware.
4. Run the firmware and read the data back from the EEPROM to confirm that it matches with the data written into it.

4 Testing and Results

This TI Design was tested for basic communication using RS-485, I2C and CAN; ESD and EFT tests for CAN and RS-485 protocol; and power consumption and efficiency with one board as a transmitter and other board as a receiver. To test the functioning of the design, program one of the boards to function as a transmitter, which sends a continuous stream of data packets and other board as receiver to continuously receive and check for the integrity of the data received. The board has LED indicators to confirm if the data being received matches with the expected data. Detailed test results are provided in the following subsections.

4.1 Basic Communication Test Results

4.1.1 RS-485

Figure 18 and Figure 19 show the multiple and single data packet communication between the transmitter and receiver, respectively.

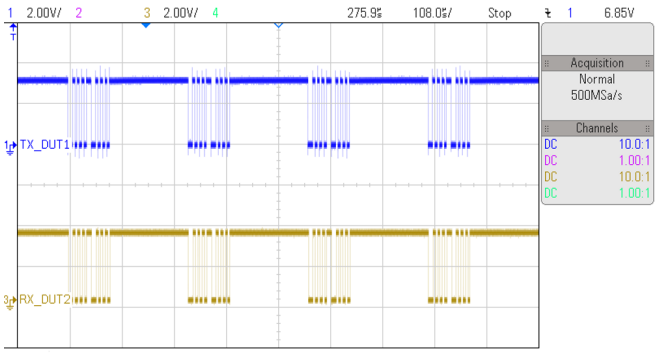


Figure 18. RS-485 Multiple Data Packet Communication

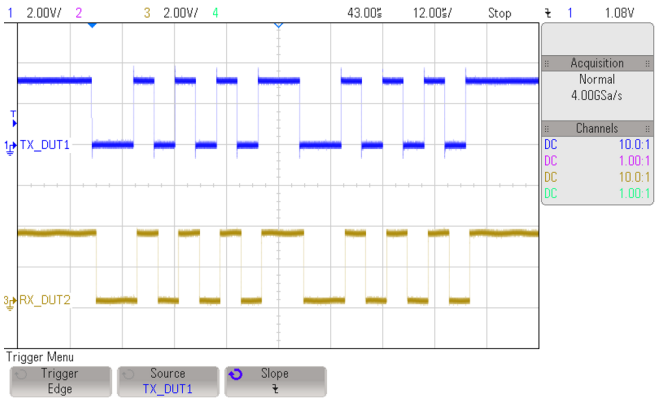


Figure 19. RS-485 Single Data Packet Communication

Figure 20 and Figure 21 show the overall rising edge and falling edge transmission delay, respectively. There is a delay of around 900 ns for the rising edge and around 1 µs for the falling edge.

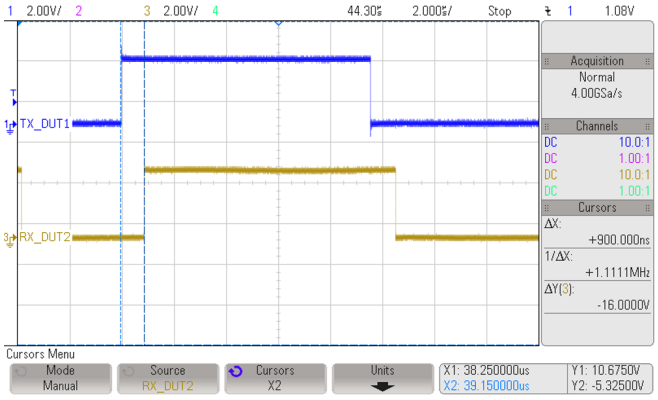


Figure 20. RS-485 Rising Edge Transmission Delay

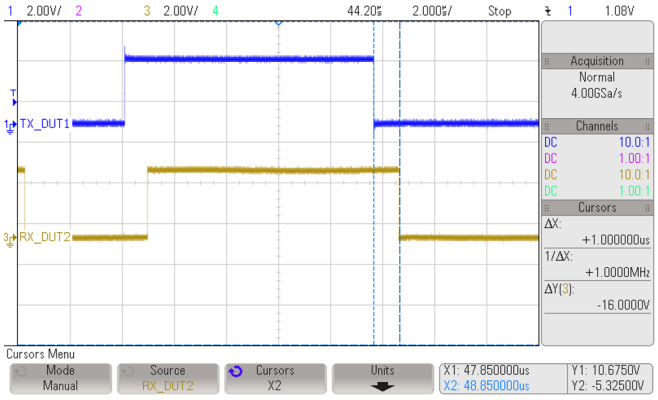


Figure 21. RS-485 Falling Edge Transmission Delay

This TI Design uses the half-duplex isolated transceiver ISO3082 for communication using RS-485. The following figures show the input and output of the transceiver after termination resistors. Figure 22 and Figure 23 compare the waveform at the input of the transceiver and the output at termination resistors while transmitting multiple data packets and a single data packet, respectively.

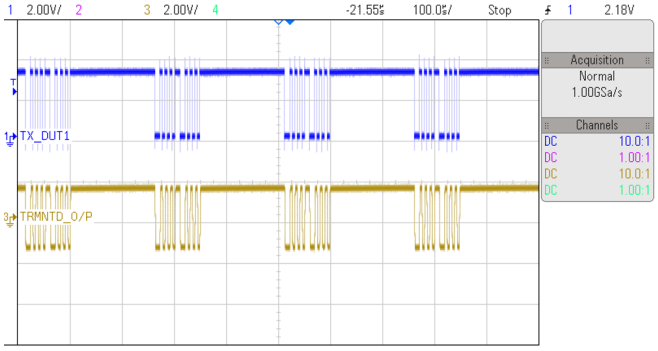


Figure 22. ISO3082 Input and Terminated Output Waveform (Multiple Data Packets)

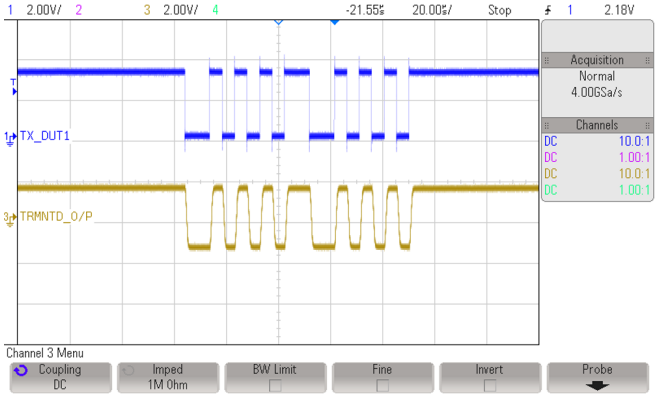


Figure 23. ISO3082 Input and Terminated Output Waveform (Single Data Packet)

Figure 24 and Figure 25 show the propagation delay between the input of transceiver and terminated output. The propagation delay is measured between the edge and 50% of output final value and is around 750 ns for the rising edge and 850 ns for the falling edge.

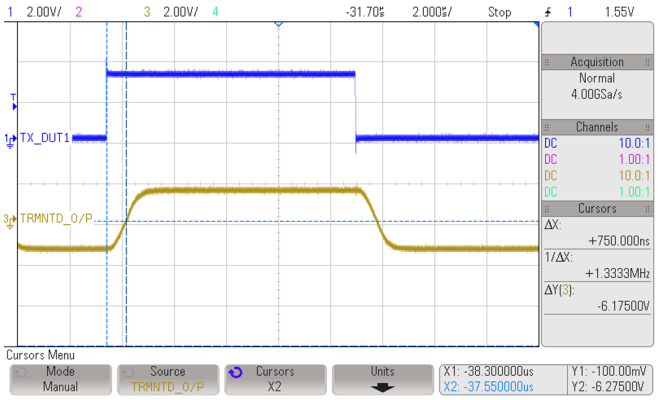


Figure 24. Rising Edge Propagation Delay of ISO3082

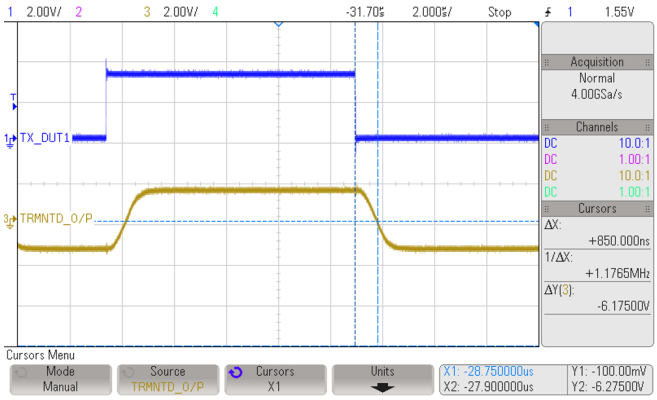


Figure 25. Falling Edge Propagation Delay of ISO3082

Figure 26 and Figure 27 show the rise time and fall time of terminated output, respectively. The rise time and fall time are about 850 ns.

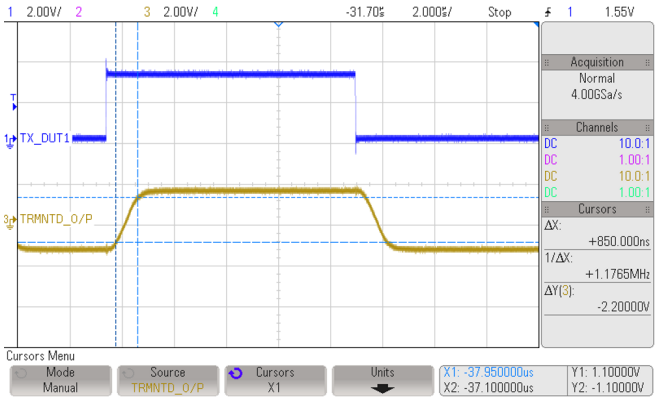


Figure 26. Rise Time of Terminated Output of ISO3082

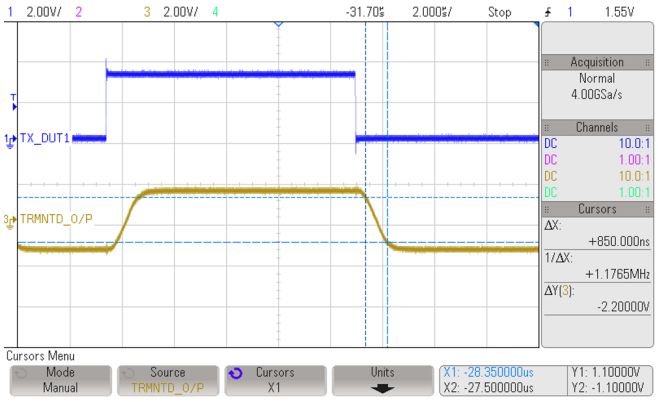


Figure 27. Fall Time of Terminated Output of ISO3082

4.1.2 CAN

Figure 28 and Figure 29 show the multiple and single data packet communication between the transmitter and receiver, respectively.

Figure 28. CAN Multiple Data Packet Communication

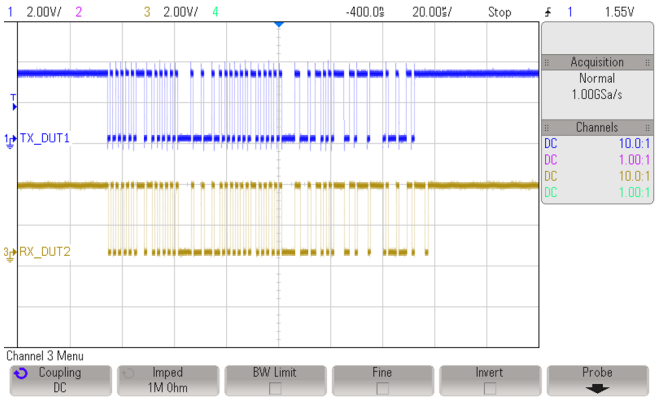


Figure 29. CAN Single Data Packet Communication

Figure 30 and Figure 31 show the total falling edge and rising edge transmission delay between CAN communication, respectively. There is a delay of 162 ns for the falling edge and 146 ns for the rising edge.

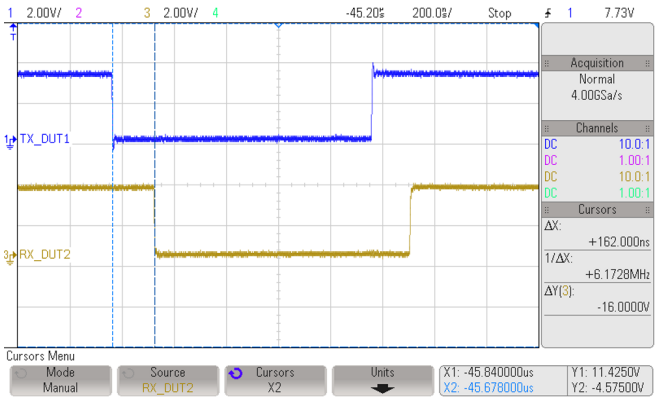


Figure 30. CAN Falling Edge Transmission Delay

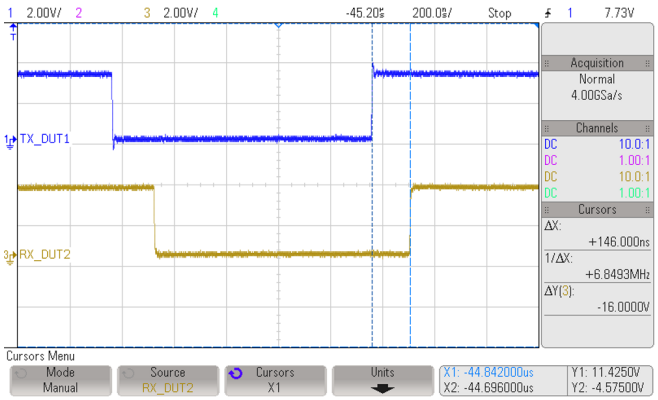


Figure 31. CAN Rising Edge Transmission Delay

This TI Design uses the isolated CAN transceiver ISO1050 for communication through CAN. The following figures show the input and output of the transceiver after termination resistors. Figure 32 and Figure 33 compare the waveform at the input of the transceiver and output at termination resistors while transmitting multiple data packets and single data packet, respectively.

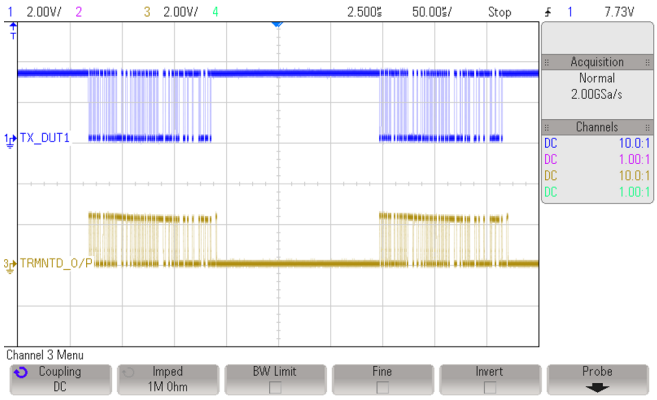


Figure 32. ISO1050 Input and Terminated Output Waveform (Multiple Data Packets)

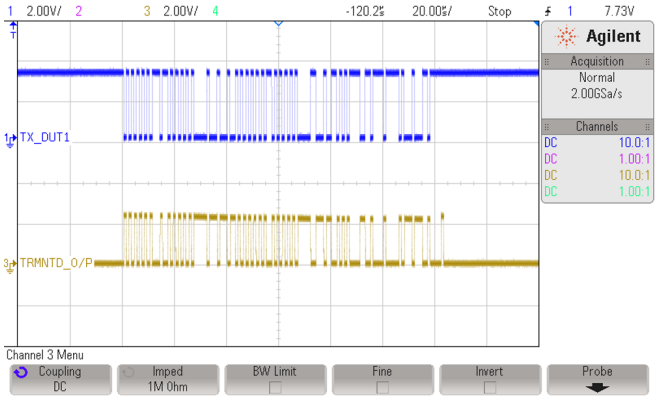


Figure 33. ISO1050 Input and Terminated Output Waveform (Single Data Packet)

Figure 34 and Figure 35 show the propagation delay between the input of transceiver and terminated output. The propagation delay is measured between the edge and 50% of output final value and is around 36 ns for the rising edge input and 80 ns for the falling edge.

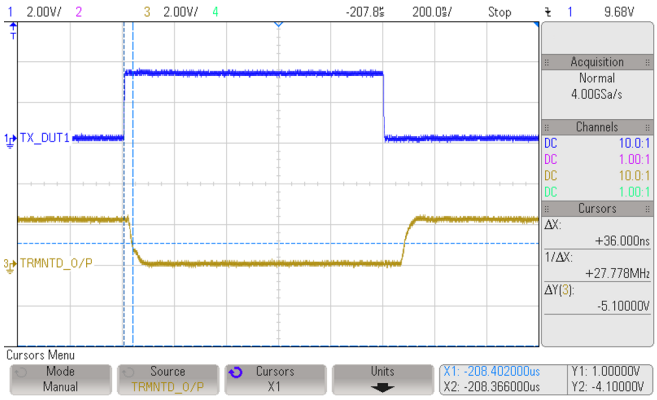


Figure 34. Rising Edge Propagation Delay of ISO1050

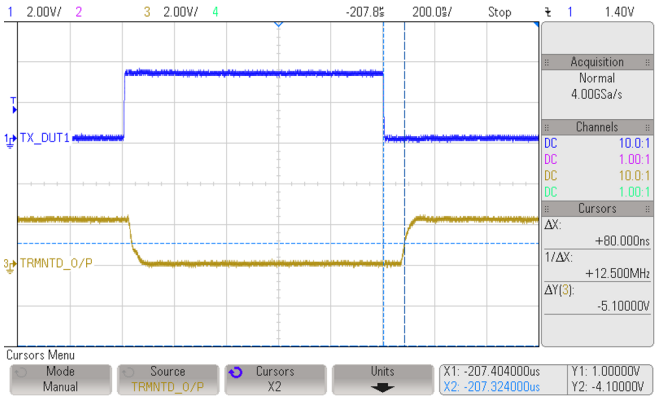


Figure 35. Falling Edge Propagation Delay of ISO1050

Figure 36 and Figure 37 show the fall time and rise time of terminated output, respectively. The rise time and fall time are about 38 ns.

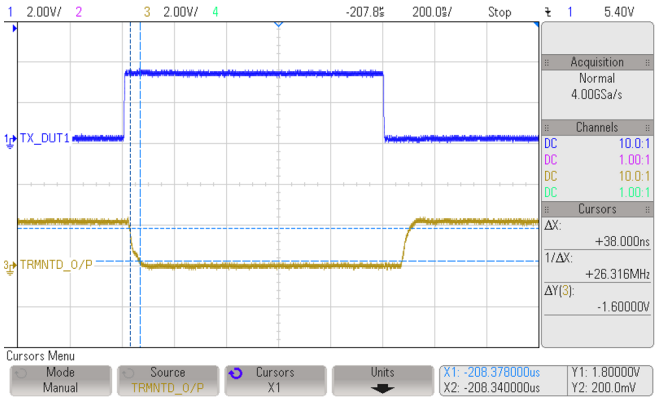


Figure 36. Fall Time of ISO1050

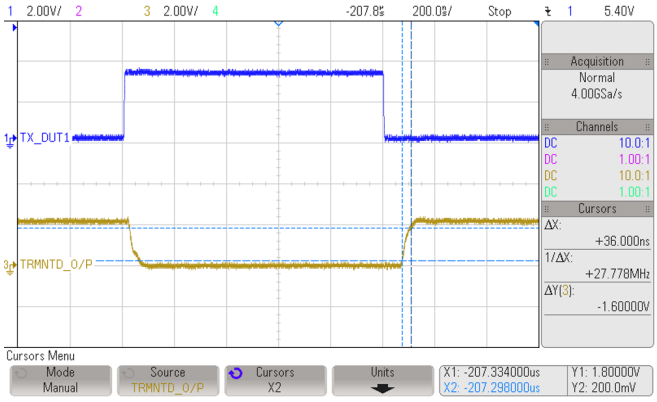


Figure 37. Rise Time of ISO1050

4.1.3 I2C

To test the functioning of I2C, this TI Design is used as master and EPROM as slave.Figure 38 and Figure 39 show the clock and data at the output of board.

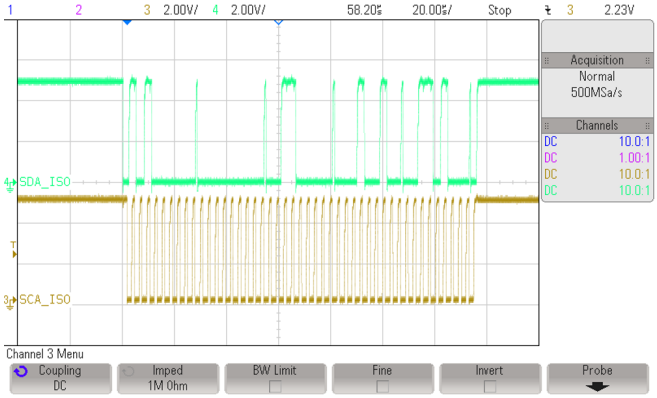


Figure 38. I2C Output Clock and Data

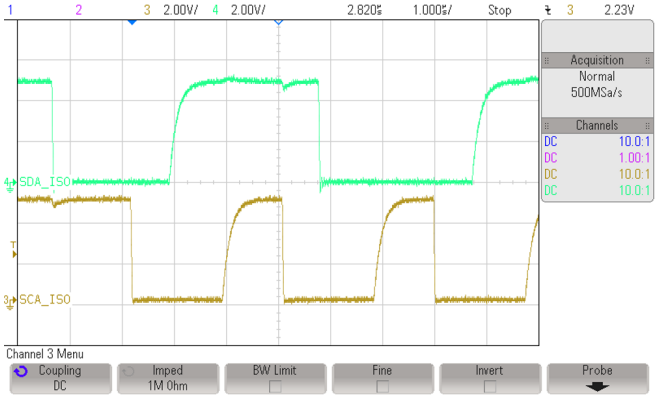


Figure 39. I2C Output Clock and Data (Zoomed)

Figure 40 shows the I2C clock and data at the input of transceiver, ISO1541. The rise time of the data is around 280 ns.

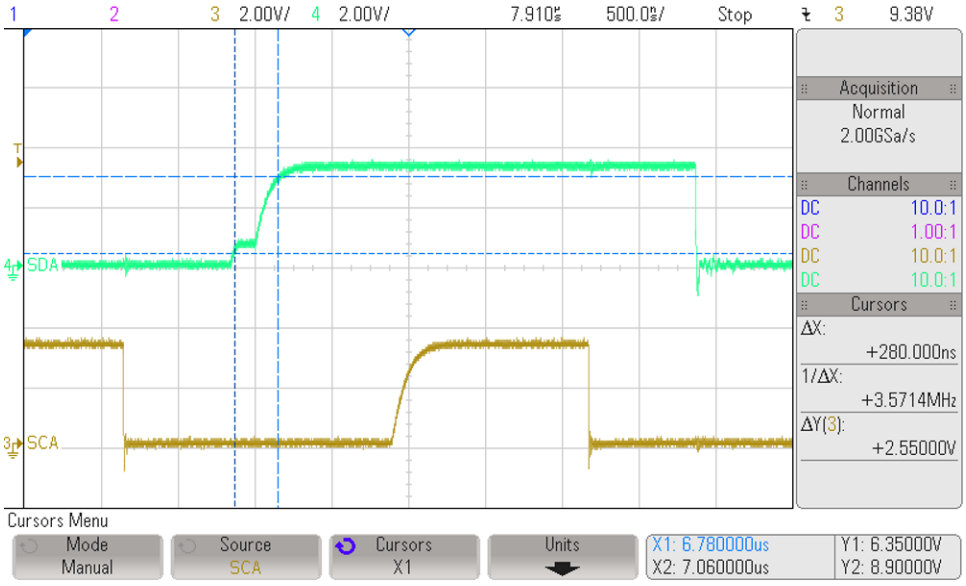


Figure 40. ISO1541 Input Data Rise Time

Because the ISO1541 is an isolated transceiver, it is important to compare the clock at the input and output of the transceiver. Figure 41 shows the clock at the input and output of transceiver where SCA is the input clock waveform and SCA_ISO is at the output of transceiver.

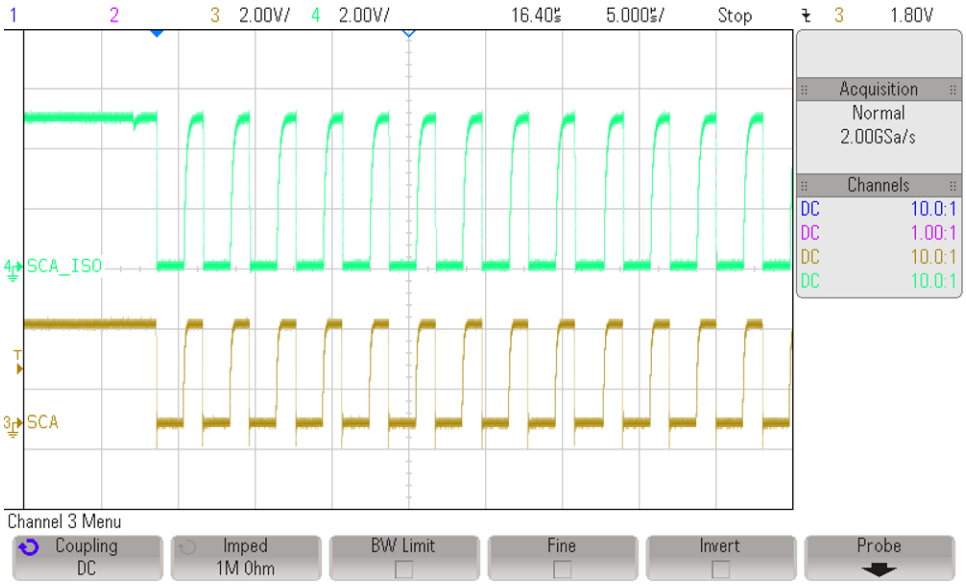


Figure 41. I2C Clock Waveform at the Input and Output of ISO1541

Figure 42 and Figure 43 show the rising edge and falling edge propagation delay between the input and output clock signal. The rising edge delay is around 90 ns and the falling edge delay is around 40 ns.

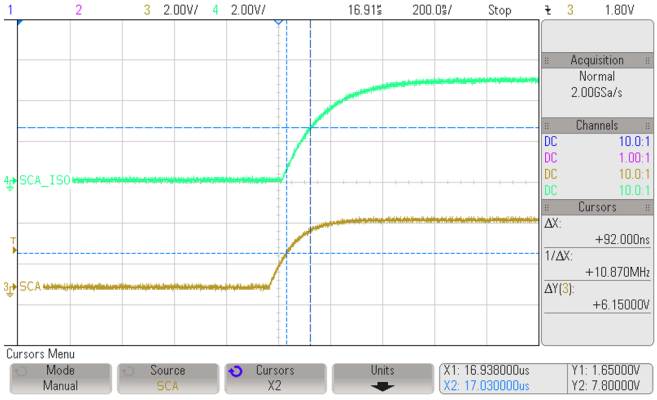


Figure 42. Rising Edge Propagation Delay of ISO1541

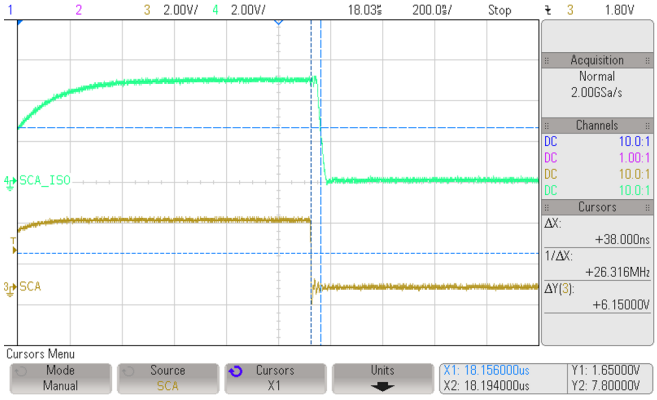


Figure 43. Falling Edge Propagation Delay of ISO1541

4.2 ESD and EFT Test

For this TI Design, EFT on signal and power line and ESD tests were conducted for RS-485 and CAN communication. Figure 44 shows the setup for EFT test on signal lines.

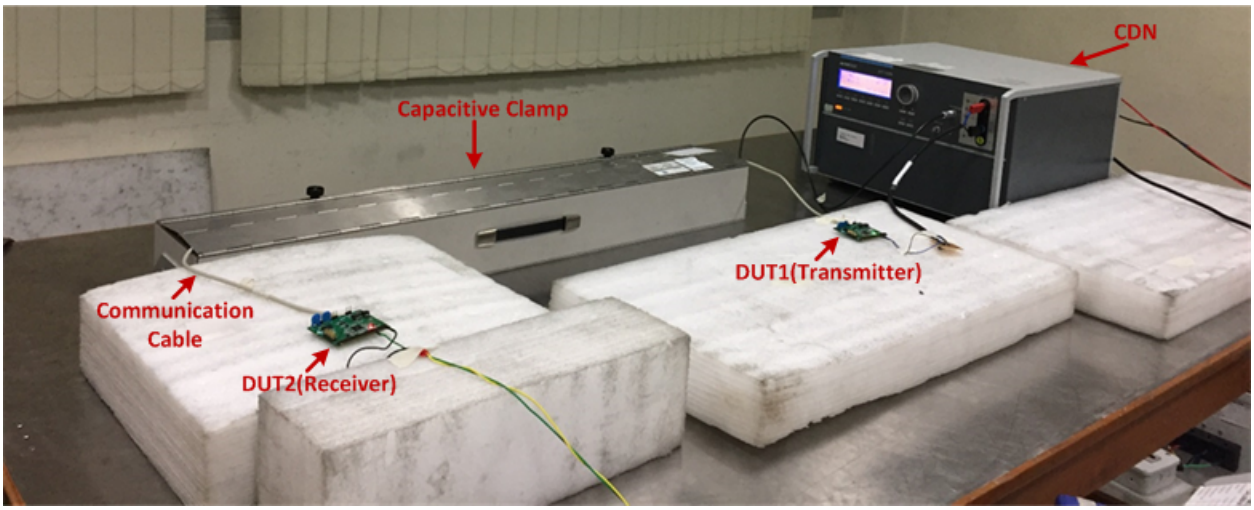


Figure 44. EFT Test Setup

EFT was applied on communication line through a capacitive clamp for signal line test and through a coupling decoupling network (CDN) for the DC power line test while the communication was taking place.

Figure 45, Figure 46, and Figure 47 show the setup for ESD test for contact discharge, indirect discharge through horizontal coupling plane b(HCP) and indirect discharge through Vertical Coupling Plane (VCP).

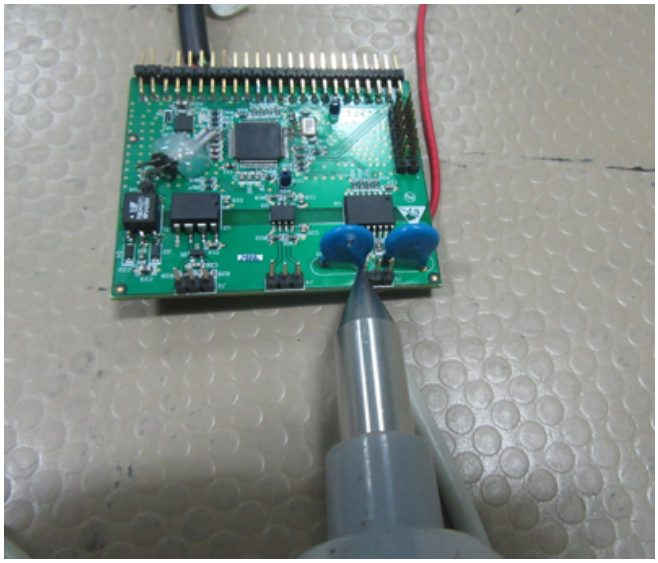


Figure 45. ESD Test Setup for Contact Discharge

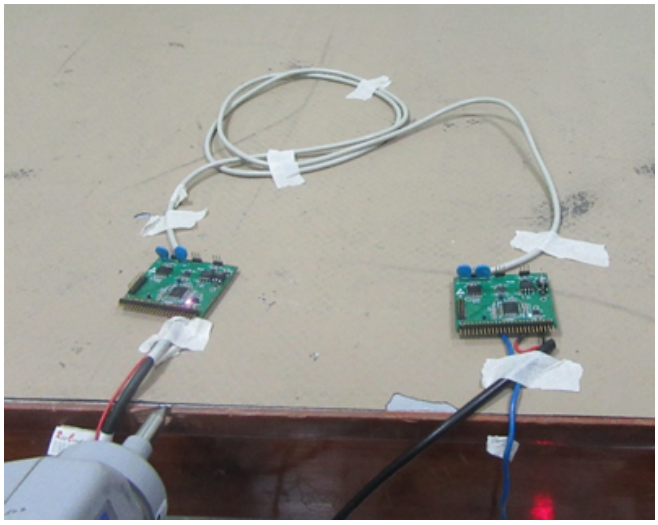


Figure 46. ESD Test Setup for Indirect Discharge by HCP

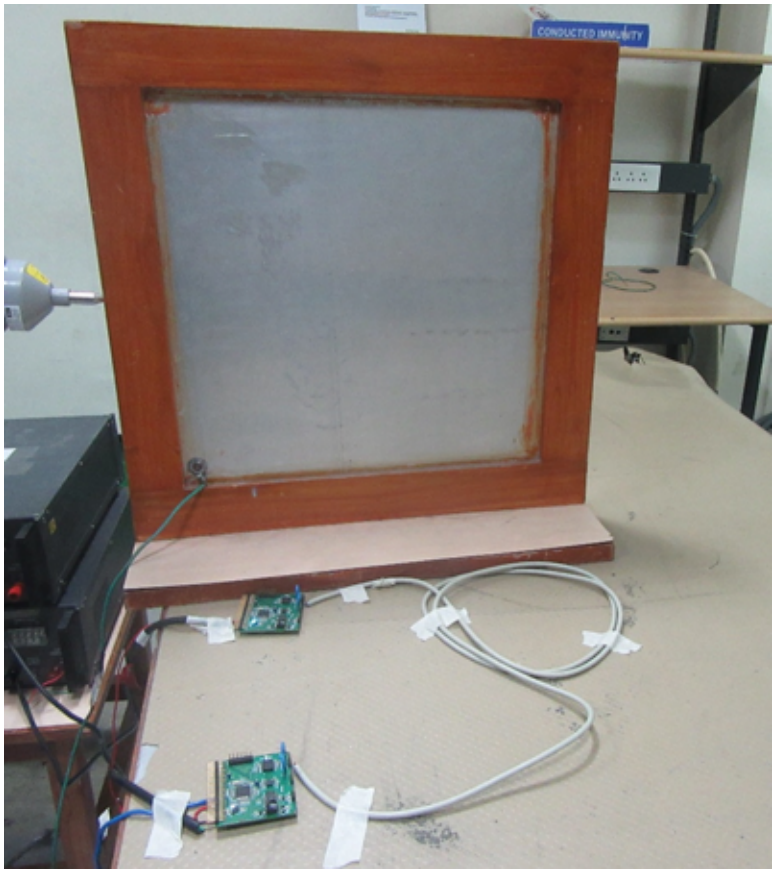


Figure 47. ESD Test Setup for Indirect Discharge by VCP

The results for ESD and EFT tests are listed in Table 9:

Table 9. ESD and EFT Test Results

BASIC STANDARD	PORT		CRITERION THRESHOLD
IEC 61000-4-2 ESD, Level 4	RS-485 communication line	Contact discharge	±8 kV
		Indirect discharge by HCP	
		Indirect discharge by VCP	
	CAN communication line	Contact discharge	± 8kV
		Indirect discharge by HCP	
		Indirect discharge by VCP	
IEC 61000-4-4 EFT, Level 4	RS-485 communication line through capacitive clamp		±2 kV, 5 kHz
IEC 61000-4-4 EFT, Level 3	CAN communication line through capacitive clamp		±1 kV, 5 kHz

EFT test was also conducted on DC power line, but no protection has been provided in this TI Design because it is intended to be used as a part of a larger system, which has the needed protection circuitry. With external bidirectional TVS diode and an electrolytic capacitor, the board is tested for ±2 kV given directly through CDN. Proper protection circuit must be used if the board requires higher EFT voltage levels.

4.3 Performance of Auxiliary Power Supply

The TIDA-01281 implements an isolated DC-DC auxiliary power supply to generate the isolated 5-V rail needed to provide bias power supply to isolated side of all the three transceivers.

Figure 48 shows the output voltage ripple at a 1-W resistive load and Figure 49 plots the efficiency of converter from a 0- to 1-W load.

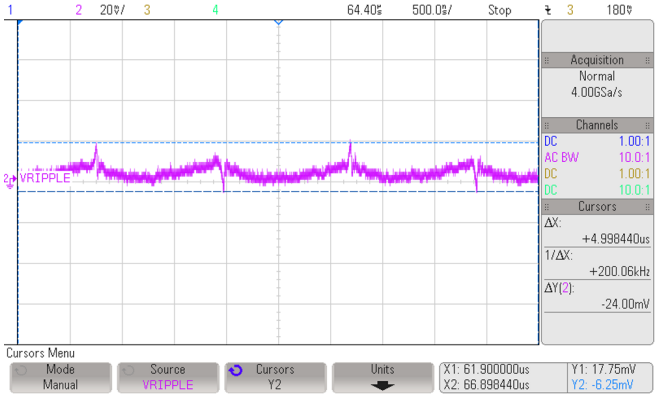


Figure 48. Output Ripple at 1-W Load

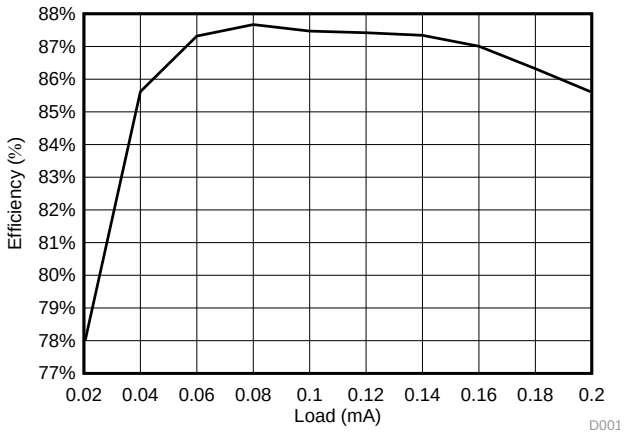


Figure 49. Efficiency of Auxiliary Power Supply

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01281.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01281.

5.3 Altium Project

To download the Altium project files, see the design files at TIDA-01281.

5.4 Gerber Files

To download the Gerber files, see the design files at TIDA-01281.

5.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01281.

6 Related Documentation

1. Texas Instruments, *TMS320x2802x, 2803x Piccolo Serial Communications Interface (SCI)*, Reference Guide (SPRUGH1)
2. Texas Instruments, *TMS320x2802x, 2803x Piccolo Inter-Integrated Circuit (I2C) Module*, Reference Guide (SPRUFZ9)
3. Texas Instruments, *TMS320x2803x Piccolo Enhanced Controller Area Network (eCAN)*, Reference Guide (SPRUGL7)

6.1 Trademarks

7 About the Authors

RAMKUMAR S is a systems engineer at Texas Instruments where he is responsible for developing reference design solutions for the industrial segment. Ramkumar brings his diverse experience in analog and digital power supplies design to this role. Ramkumar earned his master of technology (M.Tech) from the Indian Institute of Technology in Delhi.

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7.1 Acknowledgments

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