Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	2.80mil		
4	Dielectric1	FR-4	59.20mil	4.8	
5	Signal Layer 1	Copper	2.80mil		
6	Dielectric 3		5.00mil	4.2	
7	Signal Layer 2	Copper	2.80mil		
8	Dielectric 2		10.00mil	4.2	
9	Bottom Layer	Copper	2.80mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

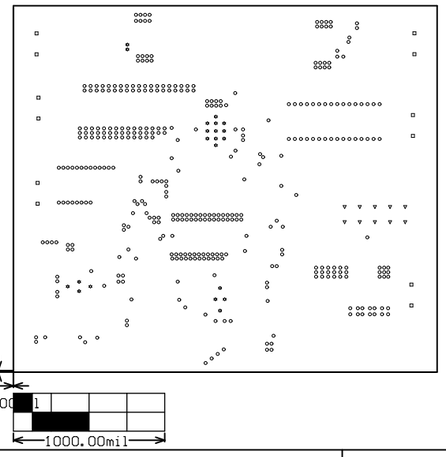
MIN. TRACK WIDTH: 8 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 24 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER _____
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER _____
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/- _____

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER _____

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER _____
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER _____
[X] MATTE [ ] SEMI-GLOSS
SURFACE FINISH: [ ] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [X] OTHER _____
ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER
ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [X] NONE [ ] REQUIRED [ ] PER ORDER



Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Tolerance
✡	21	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	
○	386	10.00mil (0.254mm)	PTH	Round	Top Layer - Bottom Layer	
▽	10	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	
□	12	50.00mil (1.270mm)	PTH	Round	Top Layer - Bottom Layer	
	429 Total					

TEXAS INSTRUMENTS

PROJECT TITLE:

DESIGNED FOR: Public Release

FILE NAME: PMP20080_PCB.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: PMP20080	REV: RevA	SVN REV: Not In VersionControl
LAYER NAME = [illegible]ions	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 7/26/2016 3:16:03 PM	TEXAS INSTRUMENTS	

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ENGINEER:	LAYOUT BY:
R Sheikh	Who did the Layout?
SCALE: 1.00	ALTIUM DESIGNER VERSION: 16.1.9.221