Application Note

CBT-C, CB3T, and CB3Q Signal-Switch Families

ABSTRACT

Signal-switch devices are used widely in applications requiring bus isolation, multiplexing, demultiplexing, and voltage translation. Compared to other logic and linear product alternatives, signal switches are the fastest and least power consuming. Texas Instruments (TI) signal-switch families have low on-state resistance, negligible power consumption, and better undershoot protection, compared to the older switch families. These qualities make CBT-C, CB3Q, and CB3T devices very good candidates for today's high-speed applications that require switches. This application report discusses some of the critical characteristics, features, and applications of TI's newest switches.

Refer to the *Selecting the Right Texas Instruments Signal Switch* application note to find details on new TMUX signal switches and multiplexers.

Table of Contents

List of Figures

Trademarks

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1 Introduction

On-off switches are one of the most common control elements in electrical circuitry. This has evolved over the years, from the manually operated circuit breaker of the early experiments to the multi-switch integrated circuit of today. In every application, the function of the switch remains the same: to isolate or connect two sections of an electrical circuit. Therefore, an ideal switch should have zero resistance (short circuit) when on and infinite resistance (open circuit) when off. However, in practical applications, a bus switch should have as low resistance as possible when on, for bus connection, and as high resistance as possible when off, for bus isolation.

2 Semiconductor Switches

An insulated-gate field-effect transistor (IGFET) switch is a widely used electronic switch. A metal-oxide semiconductor field-effect transistor (MOSFET) is one type of IGFET. Although the term MOSFET is more commonly used, now most of the electronic switches do not use the metal oxide as the gate. Instead, a more advanced process is being used to form the gate. TI uses advanced poly-silicon gate-enhancement-mode transistor technology to fabricate semiconductor switches, which gives more control of performance characteristics. Throughout this application report the term MOSFET and the associated terms related to MOSFET are used because they are more common in semiconductor literature. When sufficient bias voltage is applied to the gate of a MOSFET, it creates a low-resistance path between its source and drain. When the bias voltage is removed, the resistance of this path becomes very large. MOSFET scan be of two types, n-channel MOSFET (NMOS) and p-channel MOSFET (PMOS).

2.1 NMOS Switch

The symbol of an NMOS is shown in Figure 2-1. The source and the drain of an NMOS are interchangeable. The terminal with the lowest voltage is considered to be the source. The resistance between the drain and the source depends on the voltage difference between the gate and the source (V_{GS}). When there is sufficient voltage applied to the gate with respect to the source, the switch becomes conductive, and a voltage signal applied to the drain passes through this switch without distortion. The gate-to-source voltage at which the NMOS begins conduction is known as the threshold voltage (V_T). If the gate-to-source voltage becomes significantly less than the threshold voltage of the NMOS (V_T), the channel resistance increases rapidly.

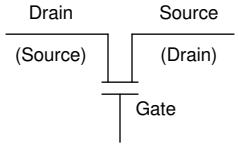


Figure 2-1. NMOS

2.2 PMOS Switch

A PMOS is similar to an NMOS (see Figure 2-2). However, to keep the source-to-drain resistance low, the difference in the source-to-gate voltage (VSG) should be greater than the threshold voltage. In a PMOS, the terminal with the lowest voltage is considered to be the drain.

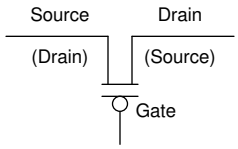


Figure 2-2. PMOS

3 Basic Signal-Switch Structures

Signal switches in their simplest form are MOSFET structures, with the gate driven by a CMOS inverter. Three types of structures are most common:

- NMOS series switch
- NMOS/PMOS parallel switch
- NMOS series switch, with the charge pump

3.1 NMOS Series Switch

The most basic signal-switch structure is an NMOS pass transistor, with the gate driven by a CMOS inverter. The simplified structure is shown in Figure 3-1.

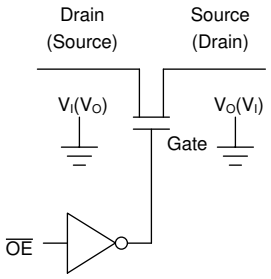


Figure 3-1. NMOS Series Switch

When the output enable (OE) signal is low, the voltage at the gate is high, or equal to V_{CC}. If the voltage at the drain (V_I) is less than V_{CC} by the threshold voltage of the n-channel transistor, the on-state resistance (r_{on}) is low and the voltage at the source is equal to V_I ($V_O = V_I$). If V_I approaches V_{CC}, r_{on} increases rapidly, the source voltage does not increase with the drain voltage, and the output voltage remains at $V_{CC}– V_T$. A limitation of the NMOS series switch is that it can pass signals only up to a threshold voltage below V_{CC}. Figure 3-2 shows the general shape of r_{on} vs V_I characteristic of a typical NMOS series switch.

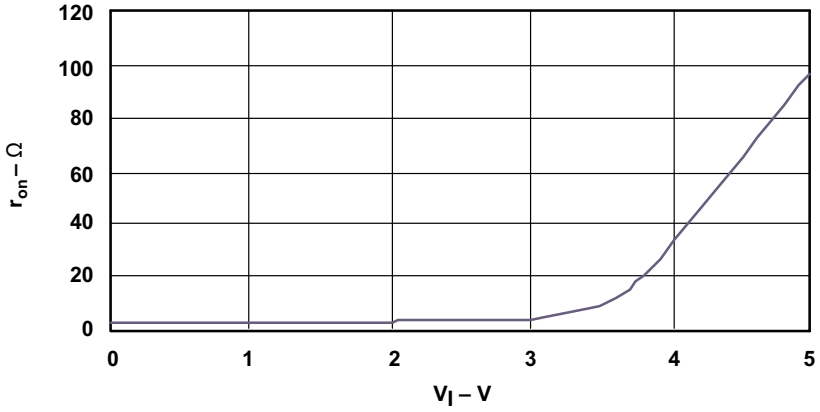


Figure 3-2. r_{on} vs V_I Characteristics of an NMOS Series Switch (V_{CC} - 5 V, I_O= –15 mA)

3.2 NMOS/PMOS Parallel Switch

An NMOS/PMOS parallel switch consists of an n-channel pass transistor in parallel with ap-channel pass transistor. Figure 3-3 shows the basic structure of an NMOS/PMOS parallel switch. In an n-channel MOSFET, the source-to-drain resistance is low when the drain voltage is less than $V_G – V_T$, where V_G is the gate voltage. In a p-channel MOSFET, the source-to-drain resistance is low when the source voltage is greater than $V_T + V_G$. with the parallel combination of n-channel and p-channel pass transistors, the source-to-drain, or channel resistance, can be lowered for the entire input voltage range from 0 V to V_G. When OE is low, V_G in NMOS/PMOS parallel switch is V_{CC}, and signals ranging from 0 V to V_{CC} can be passed through this switch. Figure 3-4 shows the general shape of the r_{on} versus V_I characteristics of a typical NMOS/PMOS parallel switch, as well as the NMOS and PMOS characteristics. The shape of r_{on} vs V_I curve may be different, depending on the

structures of NMOS and PMOS. The disadvantage of the NMOS/PMOS parallel switch is that the input and output capacitances increase due to the additional source and drain area of the combined transistors.

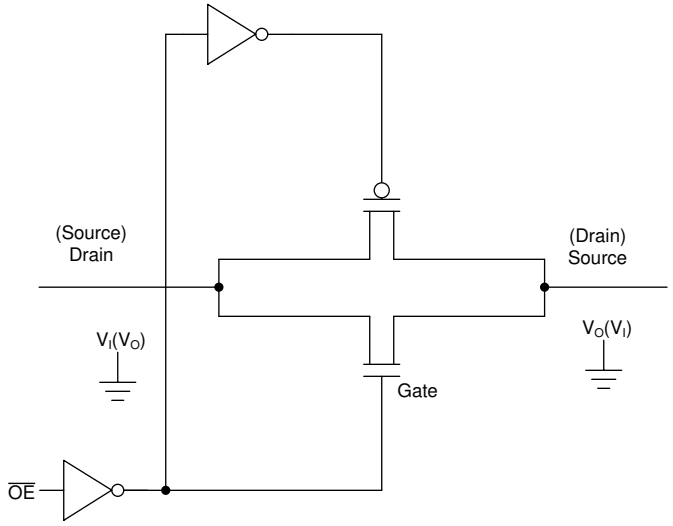


Figure 3-3. Basic Structure of an NMOS/PMOS Parallel Switch

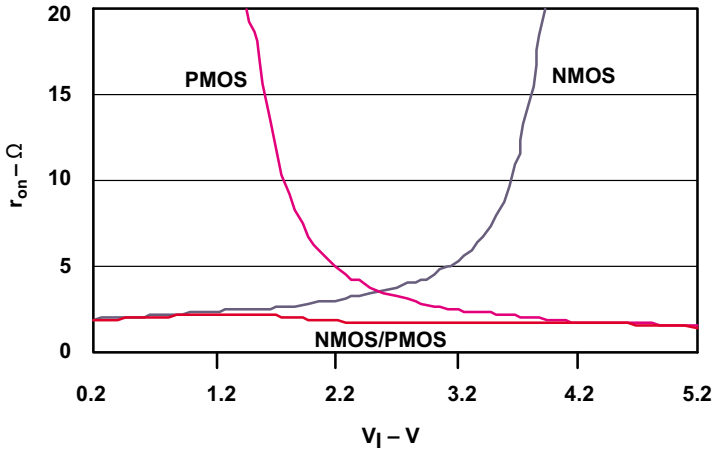


Figure 3-4. r_{on} vs V_I Characteristics of a Typical NMOS/PMOS Parallel Switch (V_{CC} = 5 V)

3.3 NMOS Series Switch with the Charge Pump

Although, in an NMOS/PMOS parallel switch, source-to-drain resistance is lower than in an NMOS series switch, the PMOS adds capacitance, which is undesirable for some applications. To solve this problem, another type of switch structure is used that involves a charge-pump circuit in the NMOS series switch. The charge-pump circuit generates a voltage at the gate of the NMOS that is 2 V to 3 V higher than V_{CC}. As a result, when the input reaches the V_{CC} level, the switch still is on and the output voltage is equal to the input voltage over the 0 V to V_{CC} input voltage range. The disadvantage of implementing a charge-pump circuit in the NMOS series switch is the additional power consumption because of the charge-pump circuit. Figure 3-5 shows a simple schematic of an NMOS series switch with the charge pump, and Figure 3-6 shows the r_{on} versus V_I characteristic.

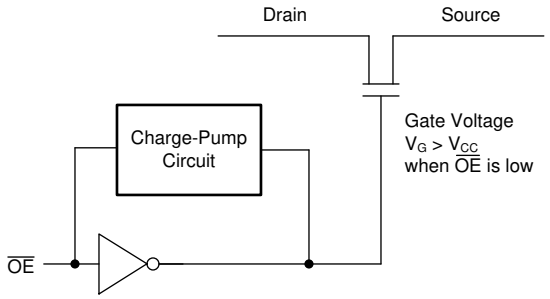


Figure 3-5. Basic Structure of an NMOS Series Switch with the Charge Pump

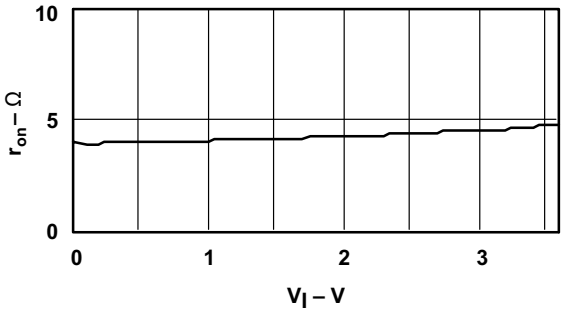


Figure 3-6. r_{on} vs V_I in an NMOS Series Switch with the Charge Pump (V_{CC} = 3.6 V)

4 Key Concerns in Digital-Switch Applications

4.1 Power and Control Voltage Requirements

One of the first considerations that must be made when selecting a switch is the supply rail voltage and the allowable input range of the signals passed through the switch. As shown in Figure 4-1, the CBT/CBT-C family of devices supports 5 V supply rails, while the CB3T, CBTLV, and CB3Q families support 2.5 V and 3.3 V rails. The dark blue regions indicate the voltage range of signals that are able to be passed through the switch. In some cases, these ranges match the supply voltage (CBT/CBT-C and CBTLV), while other switch families may pass signals that extend beyond the supply rail (CB3T and CB3Q). System requirements may dictate which devices can be used in a particular application. For example, designs implementing a 5 V supply rail and a 5 V signal are likely best served by a device in the CBT/CBT-C family, while a design using a 3.3 V supply rail and a 4 V signal are best served by a device in the CB3T or CB3Q family.

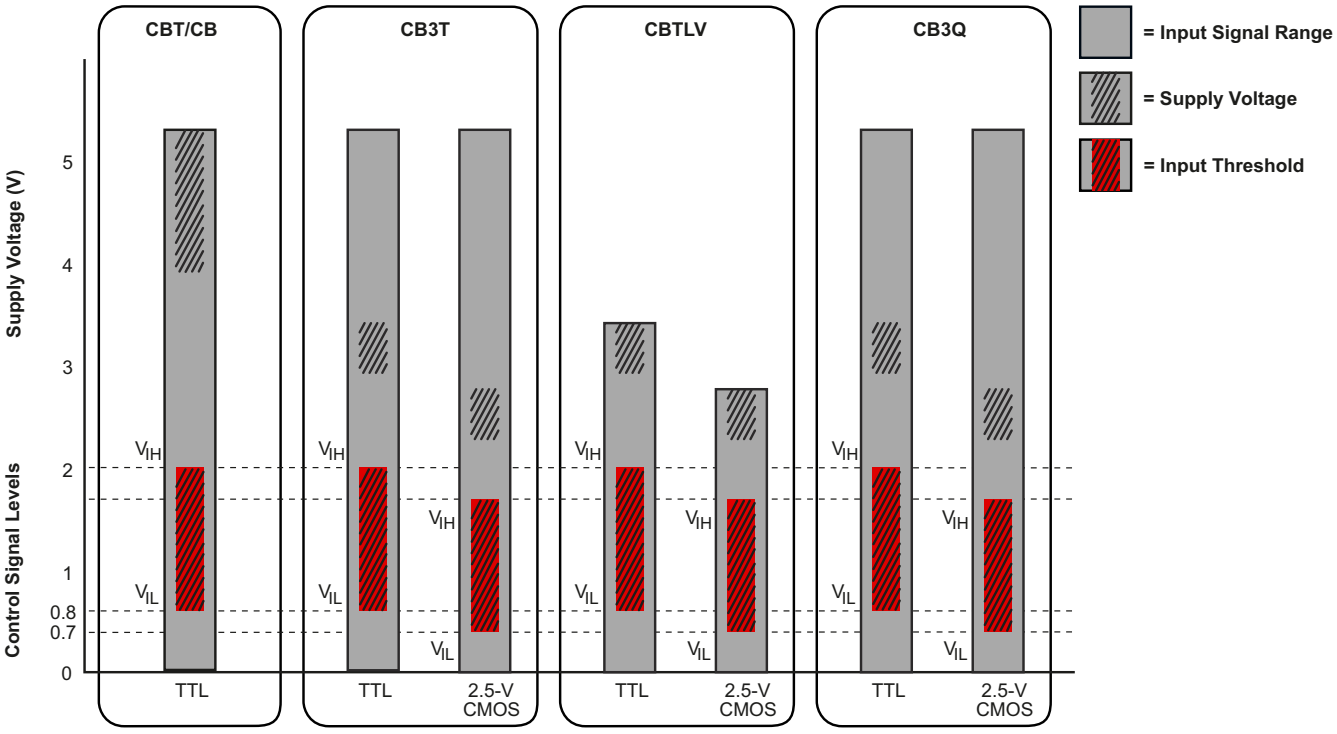


Figure 4-1. Control Signal Levels (V_{IH}, V_{IL}) and Supply Voltage

The input thresholds of these devices allow users to implement 3.3 V logic or 5 V logic, regardless of the supply voltage or signal voltage being used in design. The red bars in Figure 4-1 show the logic level voltage thresholds for the different digital switch families.

4.2 Rail-to-Rail Operation

Rail-to-rail operation describes the behavior where a signal switch passes signals that range between the most positive and most negative supply rails. Switches with rail-to-rail operation will pass signals with little to no voltage drop when the signal falls at or between the voltage rails. Figure 4-2 shows the behavior of different switches operating at different signal and rail levels.

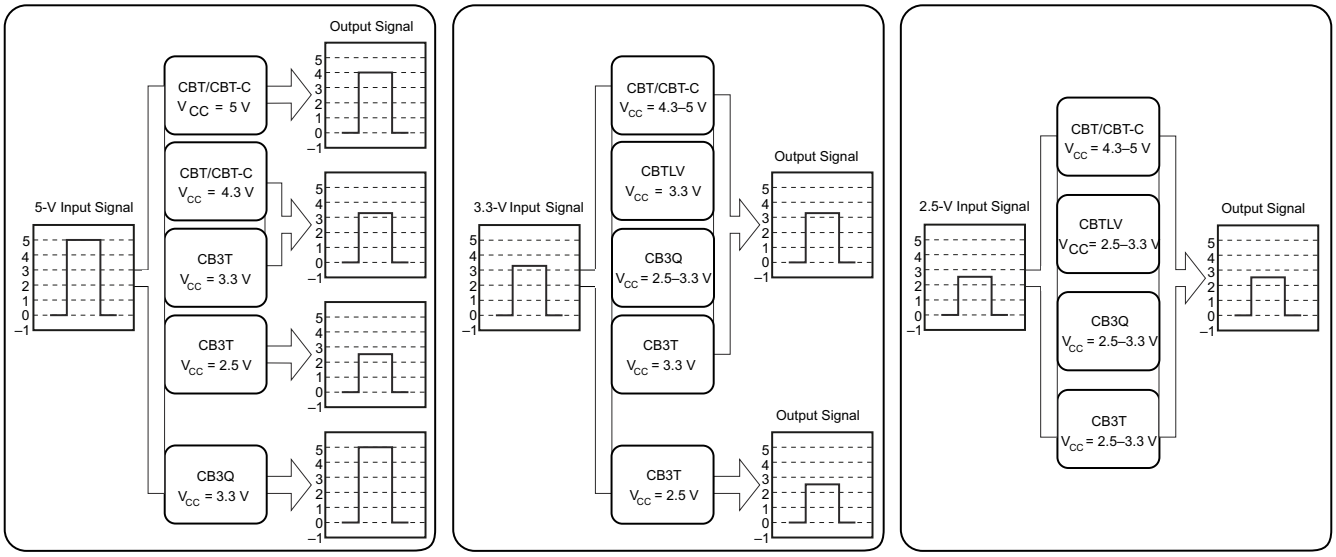


Figure 4-2. Signal Levels Through Digital Switches

Digital signals between communicating devices usually must meet some minimum voltage level to be registered as a *high* signal. All devices along a signal path, including a digital switch, should be considered when determining the efficacy of a design. Reduced high-level voltages from non-rail-to-rail switches should be considered, and designs should ensure that appropriate signal levels will be attained. Using rail-to-rail switches minimizes or removes risk from this phenomenon. Certain switches, like the CB3T and CB3Q families, allow I/O voltages beyond the supply, allowing designers increased opportunity for effective implementation and design.

4.3 Undershoot

Undershoot is a typical phenomenon in high-speed applications where impedance mismatches cause excessive ringing in the system. This poses a serious problem to bus switches that are turned off and attempt to isolate different buses. In this state, the gate voltage of the n-channel pass transistors are at ground potential, but a negative voltage on either I/O port with a magnitude greater than the NMOS V_T will cause the switch to conduct and no longer isolate the buses. Therefore, undershoots with a large magnitude and long duration result in data corruption, if no undershoot protection circuitry is included in the signal-switch design. The schematics in Figure 4-3 demonstrate the phenomenon of undershoots. For normal input voltages ranging from 0 V to V_{CC}, the switch is in the high-impedance state and the output bus is isolated from the input bus. The undershoot produces a glitch at the isolated bus, as shown in Figure 4-3.

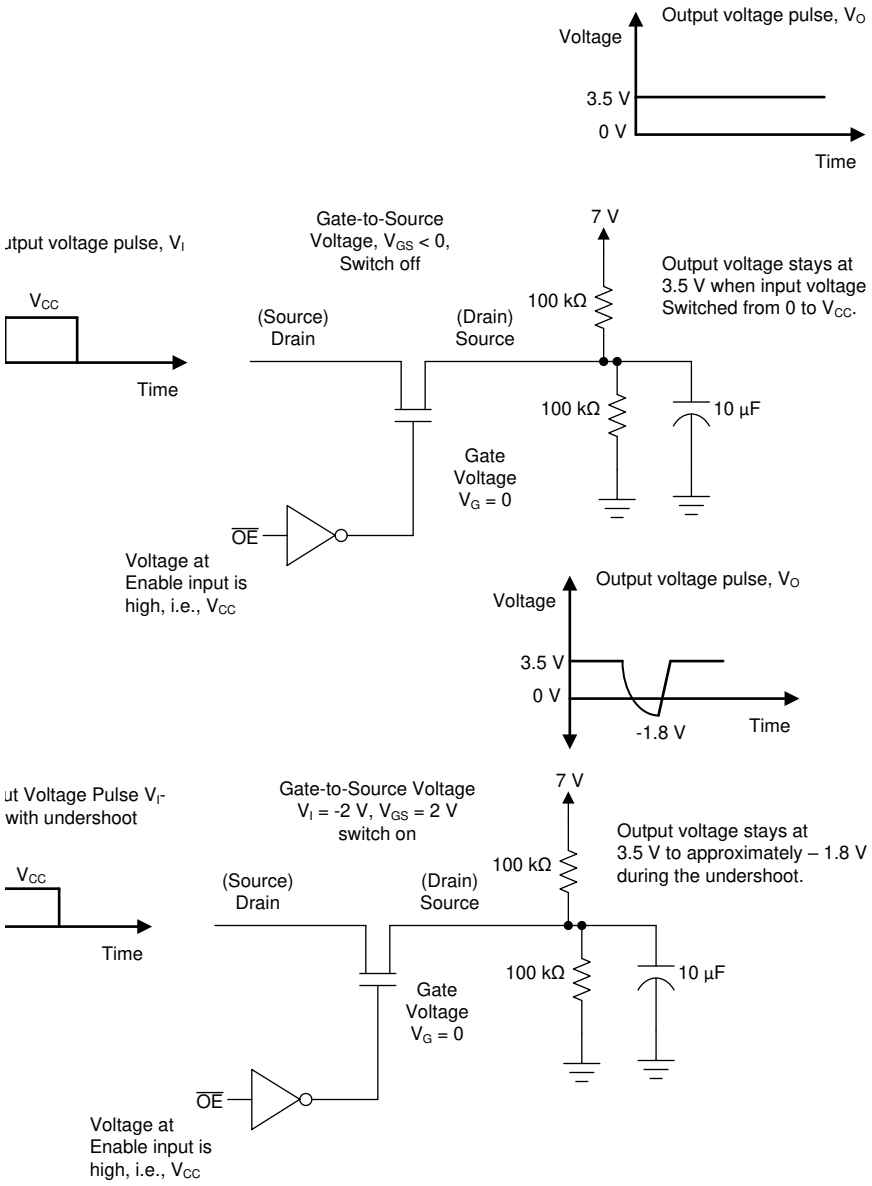


Figure 4-3. Undershoot in NMOS Series-Switch Devices When Disabled

There are two solutions to prevent the NMOS from turning on during the undershoot even while disabled:

- Capture or clamp the input undershoot energy. In this method, a clamp circuit is connected to ground or V_{CC}. This clamp circuit prevents the NMOS from turning on while an undershoot event occurs.
  - Schottky Clamp. In this method, a Schottky diode is connected from the I/O port of the switch to ground. When the voltage at the I/O port goes below ground, the diode is forward biased and clamps the source or drain voltage, keeping the input and output isolated. An example of this type of device is the CBTS bus switch provided by TI.
  - Active clamp to V_{CC}. In this method, an active clamp circuit is connected to V_{CC}, which tries to counteract the undershoot voltage by pulling the input voltage to V_{CC}. An example of this type of device is the CBTK bus switch provided by TI.
- Force the gate voltage of the NMOS to track the negative input voltage. TI's new CBT-C family uses this method to prevent undershoot. This method of protection is described later in this application report.

4.4 r_{on}

r_{on} is the resistance of the switch when turned on. r_{on} should be as low as possible to reduce signal loss and to reduce propagation delay. Propagation delay of the switch depends on the RC time constant, which is made up of the switch r_{on} and the load capacitance. For applications in transmission-line environments, r_{on} should be less than, or equal to, the line impedance to minimize unwanted signal reflections. For digital applications where the switch is connected to a resistive load, the switch resistance and the load resistance form a voltage divider. Therefore, in this case, r_{on} should be as low as possible to maintain a valid input logic high (for example, V_{IH}) of the downstream devices. r_{on} not only should be small, but also should be flat across the input voltage range to maintain a linear signal change from input to output. Signal distortion depends on the flatness of the r_{on} versus V_I curve, that is, equal to $20\log\Delta r_{on}$ /RL, where RL is the load resistance. So, to keep signal distortion minimum as the signal amplitude varies, r_{on} should be kept flat over the whole input signal range. In NMOS series switches, special gate voltage-boost circuitry is needed to keep r_{on} flat over the V_{CC} range. In NMOS/PMOS parallel switches, r_{on} is fairly constant and may have multiple peak values within 0 V to V_{CC} input voltage range. The shape of the r_{on} versus V_I curve depends on the threshold voltages of NMOS and PMOS (see Figure 3-4).

4.5 $C_{io(off)}$

$C_{io(off)}$ for a through switch is the off-state capacitance of one channel, measured from either the input or output of the switch. For a multiplexer or bus-exchange switch, $C_{io(off)}$ may include off-state capacitance for multiple channels. $C_{io(off)}$ should be as small as possible to prevent capacitive loading of the bus. Reducing C_{io} requires less drain and source area of the pass transistors that otherwise would increase on-state resistance. So, there is a trade-off between $C_{io(off)}$ and r_{on}.

4.6 $C_{io(on)}$

This is the on-state capacitance of the switch, measured from either the input or output of the switch. Usually $C_{io(on)}$ is greater than twice the $C_{io(off)}$ because it includes the capacitance on both input and output of the switch, as well as the channel capacitance. Like $C_{io(off)}$, $C_{io(on)}$ should be as small as possible to reduce capacitive loading of the bus. Reducing $C_{io(on)}$ requires less drain and source area of the pass transistors that otherwise would increase the on-state resistance. So, like the $C_{io(off)}$, there is a trade-off between $C_{io(on)}$ and r_{on}.

4.7 C_i (Control Input Capacitance)

When switching control input, a large control input capacitance will inject more charge to the gate of the pass transistor. This will cause crosstalk and degrade performance of the switch.

4.8 Leakage Current

Leakage current during the high-impedance state should be very small. Leakage current, if high, may load an isolated bus and corrupt the data.

4.9 Enable and Disable Delays and Propagation Delay

Enable and disable delays (t_{en} and t_{dis}) are measures of how quickly the switch can be turned on and off. Not only should these delays be as small as possible for high-speed operation, but also the difference of enable and disable delays should be as small as possible to reduce the current flow between the off switch and on switch. This is significant in multiplexing and demultiplexing operations where the difference, if large, can cause bus contention. For break-before-make functions, disable time should be less than enable time and for make-before-break functions, enable time should be less than disable time.

Propagation delay (t_{pd}) introduced by digital switches is negligible for all applications except those with the most critical timing budgets. When the digital switch is on, the delay through the pass transistor is minimal. Generally, the effective propagation delay of a digital signal varies as a product of output capacitance and varies widely across different applications. Texas Instruments specifies this value as the mathematical calculation of the typical r_{on} times the load capacitance.

4.10 Partial Power Down

Today's high-speed applications require that a device can be powered-down while still connected to a live bus. This requires the switch to be in the high-impedance state while the power is down. A special I_{off} circuit is incorporated to ensure that the switch is in the high-impedance state while the power is off. I_{off} circuitry prevents damaging current backflow through the device when it is powered down.

4.11 Voltage Translation

One popular application of the bus switch is voltage translation in a mixed-voltage environment. A simple NMOS can pass a signal from 0 V to V_{CC}– V_T, where V_T is the threshold voltage of the NMOS. This characteristic can be used for down translation. Figure 4-4 shows an example of 5-V to 3.3-V translation using an NMOS series switch, diode, and resistors.

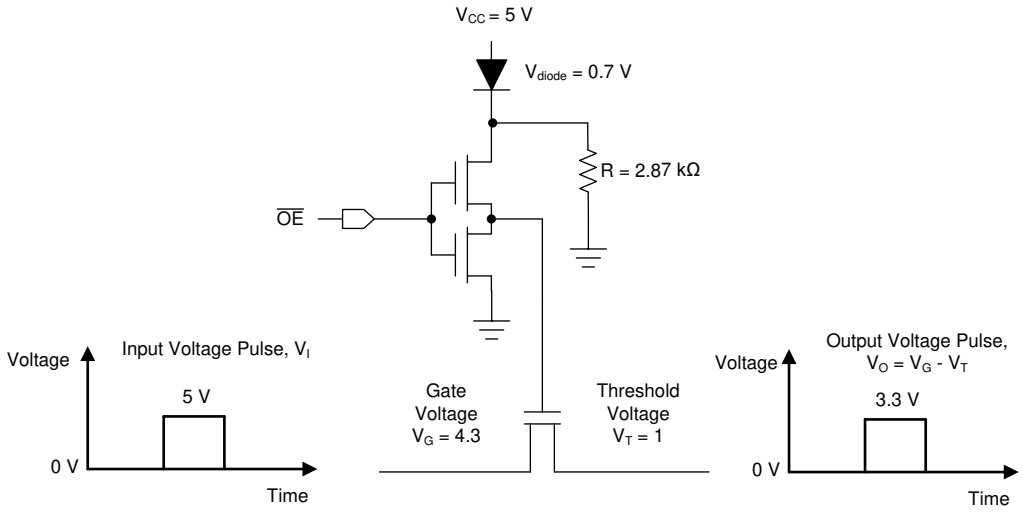


Figure 4-4. Voltage Translation Using an NMOS Series Switch

For voltage-translation applications, the switch is required to translate efficiently over a wide frequency range and is required to maintain the proper signal level. For example, when translating from a 5-V TTL to a 3.3-V LV_TTL signal, the switch is required to maintain the required V_{OH} (output high voltage) and VOL (output low voltage) of 3.3-V LV_T TL signal. One important consideration is that the bus switch can be used only for down translation, for example, high to low-level. For low to high-level translation, additional components (for example, pullup resistors) are required.

5 Signal Switch Families

TI offers a wide variety of signal switches suitable for many different types of applications. Some of the signal-switch families are discussed in the following sections:

- CBT-C: 5-V NMOS Switches with –2-V undershoot protection
- CBTLV: Low-voltage switches with parallel NMOS and PMOS transistors
- CB3Q: NMOS switches with a charge-pump circuit for low and flat r_{on}
- CB3T: Level-shifting NMOS bus switch

5.1 CBT-C Family

The switches in the CBT-C (Cross-Bar Technology - Clamp) family are NMOS series switches. The operating V_{CC} of this family is 5 V, and switching for various standards (for example, LVCMOS, LVTTL, and so forth) can be accomplished. This family also has an undershoot protection circuit integrated in the bus switch. The undershoot protection circuit prevents the n-channel pass transistor from turning on when the switch is off. When undershoot occurs, this circuit senses the negative voltage at the input and biases the gate of the n-channel pass transistor to that negative voltage. Since the gate and source voltage are now at the same potential (<0 V), the switch remains off. Undershoot protection on one side of the off switch can prevent up to –2 V undershoots on the other side of the switch. Static power consumption of this family is negligible. Dynamic power consumption depends on the frequency of the enable input of the device. Switching high and low at the enable input causes internal CMOS inverters to switch between low and high; therefore, a higher frequency of the control input signal results in higher dynamic power consumption. Undershoot protection in CBT-C is shown in Figure 5-1.

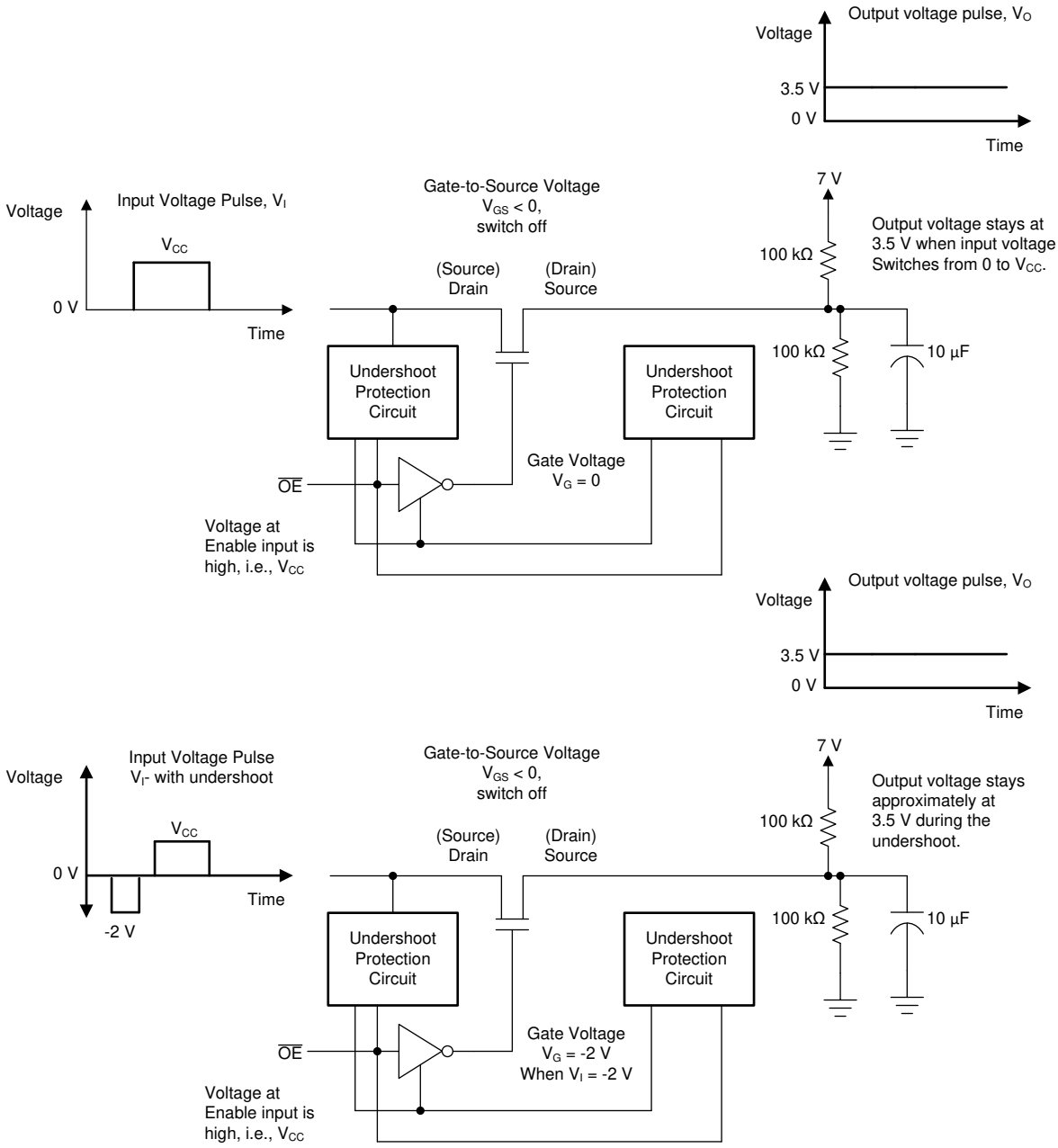


Figure 5-1. Undershoot Protection in CBT-C When Enable Input (OE) Voltage is High

5.1.1 Characteristics of CBT-C Family

The following paragraphs discuss some of the critical performance characteristics of the CBT16211C. The setup for measurements is given in Appendix A.

5.1.1.1 V_O vs V_I

Figure 5-2 shows the output-voltage vs input-voltage characteristics of the CBT16211C at an output load of 3 kΩ to ground. The output follows the input approximately until 3.5 V and remains flat as the switch begins to turn off. Output voltage also depends on the output current. If output current increases, the output voltage will become flat at a lower input voltage.

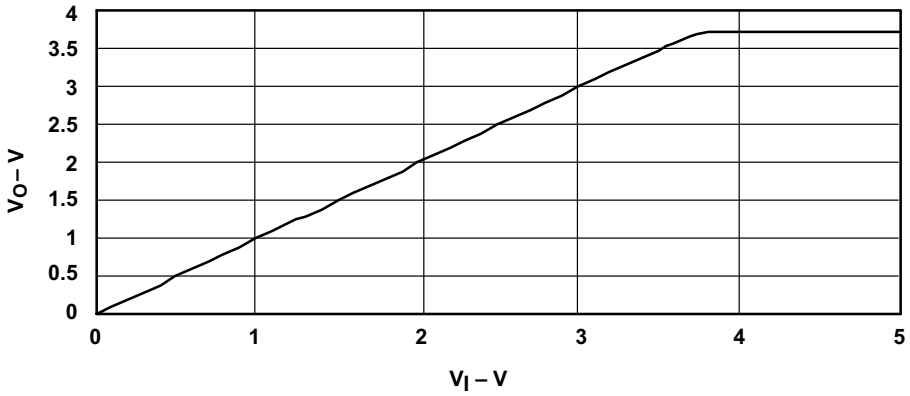


Figure 5-2. V_O vs V_I at V_{CC} = 5 V

5.1.1.2 r_{on} vs V_I

Figure 5-3 shows the switch resistance (r_{on}) when on, as a function of the input voltage. The output current is –15 mA. The on-state resistance is low when the input voltage is below 3.5 V and increases rapidly above 3.5 V. r_{on} depends on the output current and increases rapidly at a lower input voltage when the output current increases.

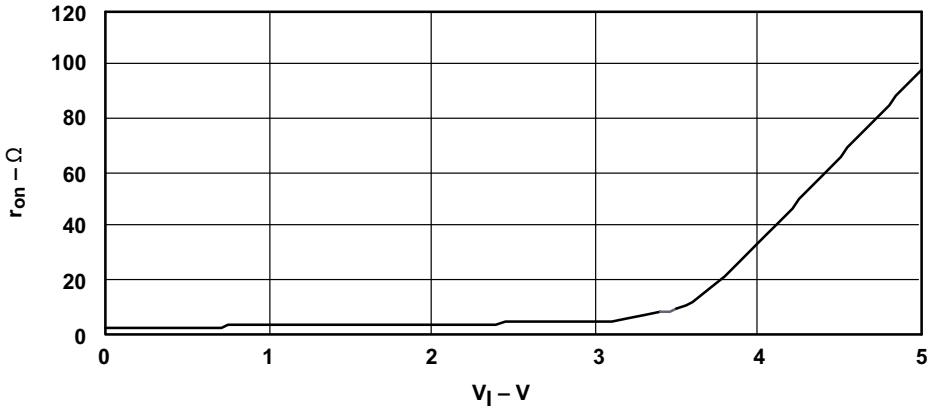


Figure 5-3. r_{on} vs V_I at V_{CC} = 5 V (IO = –15 mA)

5.1.1.3 Undershoot Protection

Figure 5-4 shows the undershoot protection performance of the CBT16211C when the switch is disabled. The output pin is connected to ground through a 100-kΩ resistor, a 10-pF capacitor, and to 10 V through a 100-kΩ pullup resistor. The test load is similar to a high-impedance application load. There is very little variation in output voltage caused by input-voltage undershoot.

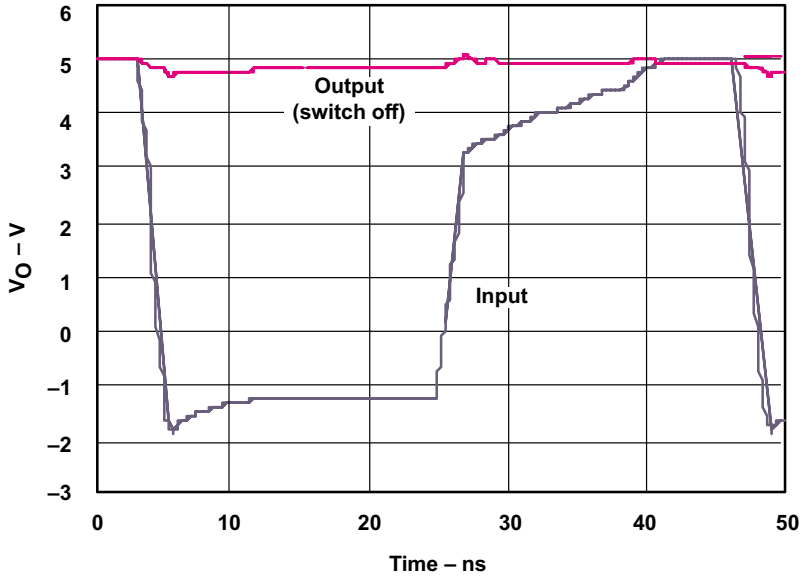


Figure 5-4. Undershoot in CBT16211C When Switch is Off (V_{CC} = 5 V)

5.1.2 Application of CBT-C Family

5.1.2.1 Bus Isolation

CBT-C devices can be used for 5-V PCI bus isolation for hot-plug applications (see Figure 5-5). PCI is an unterminated interface; therefore, undershoot may occur. CBT-C provides good isolation when an undershoot event occurs.

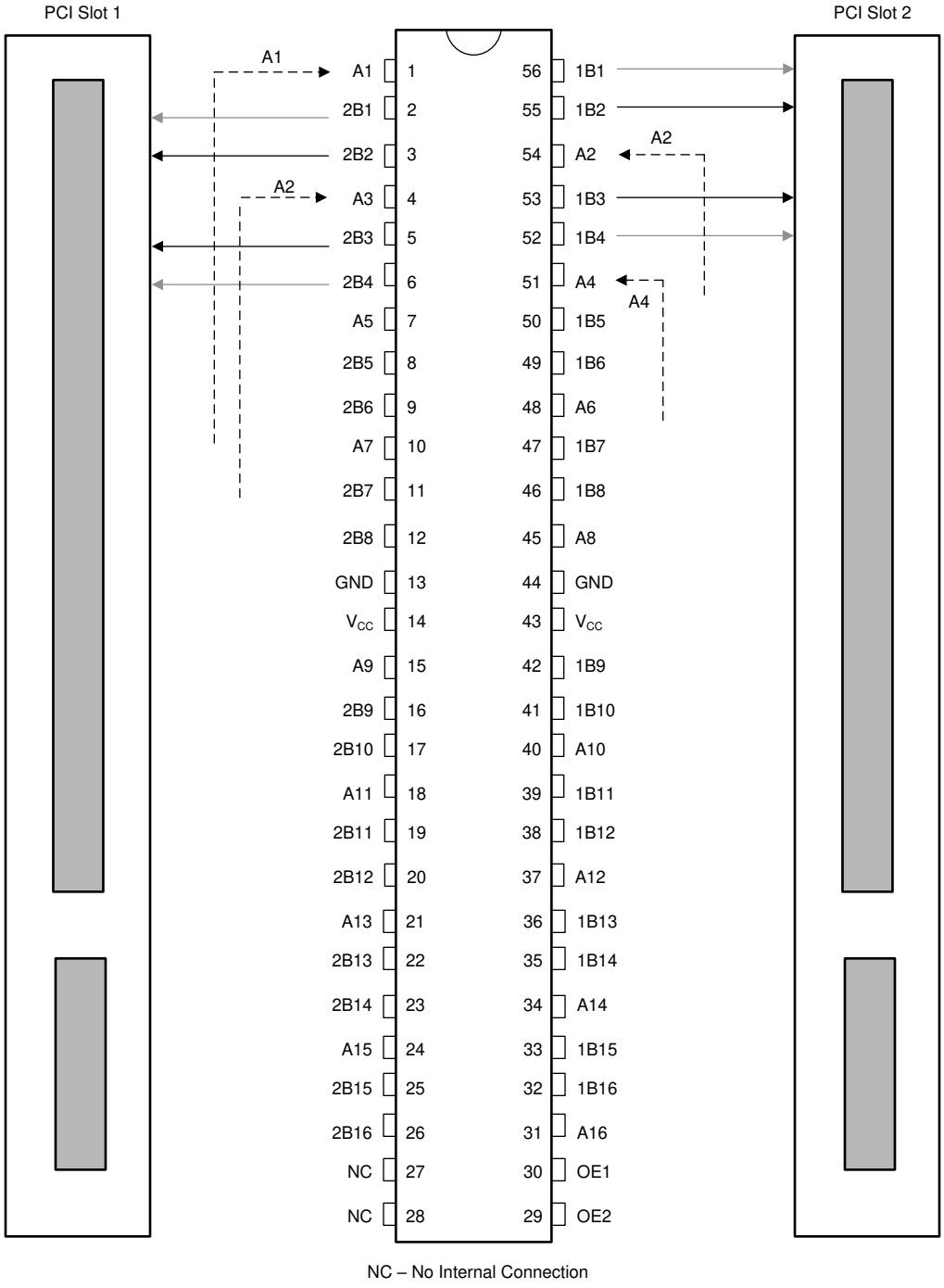


Figure 5-5. Example of Bus Isolation Using a CBT-C Device

5.2 CBTLV Family

The switches in the CBTLV (Low-Voltage Cross Bar Technology) family were the first general-purpose FET bus switches designed for 3.3 V systems. The devices in this family provide rail-to-rail switching and a low r_{on} (5 Ω) and low $C_{I/O}$ (4.5 pF). CBTLV switches consist of a simple NMOS transistor in parallel with a PMOS transistor. When the switch is open, it provides tri-state isolation for its bus line. When the switch is closed, it imposes near-zero propagation delay on the line. Figure 5-6 shows a simplified schematic of a CBTLV device.

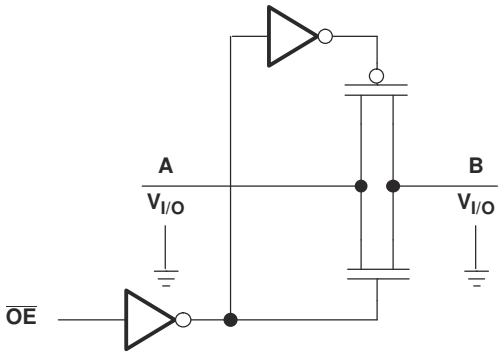


Figure 5-6. Simplified Schematic of a CBTLV Device

5.2.1 Characteristics of the CBTLV Family

Figure 5-7 shows the V_O vs. V_I characteristics of the SN74CBTLV3125 and the r_{on} flatness for V_{CC} = 2.5 V. The output voltage exactly follows the input across the input signal range from 0 V to V_{CC}.

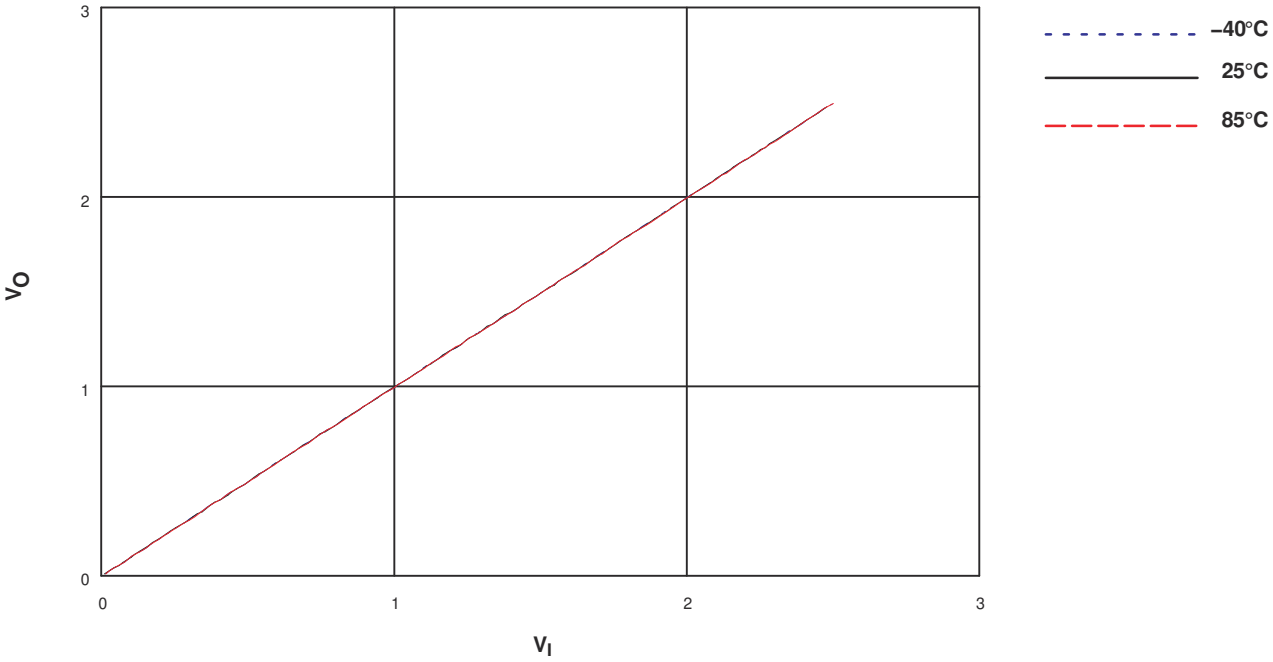


Figure 5-7. V_O vs. V_I, V_{CC} = 2.5 V (SN74CBTLV3125)

The architecture of the CBTLV switch results in an on-resistance as low as 5 Ω. Figure 5-8 shows measurements of the on-resistance across the signal range and at different temperatures.

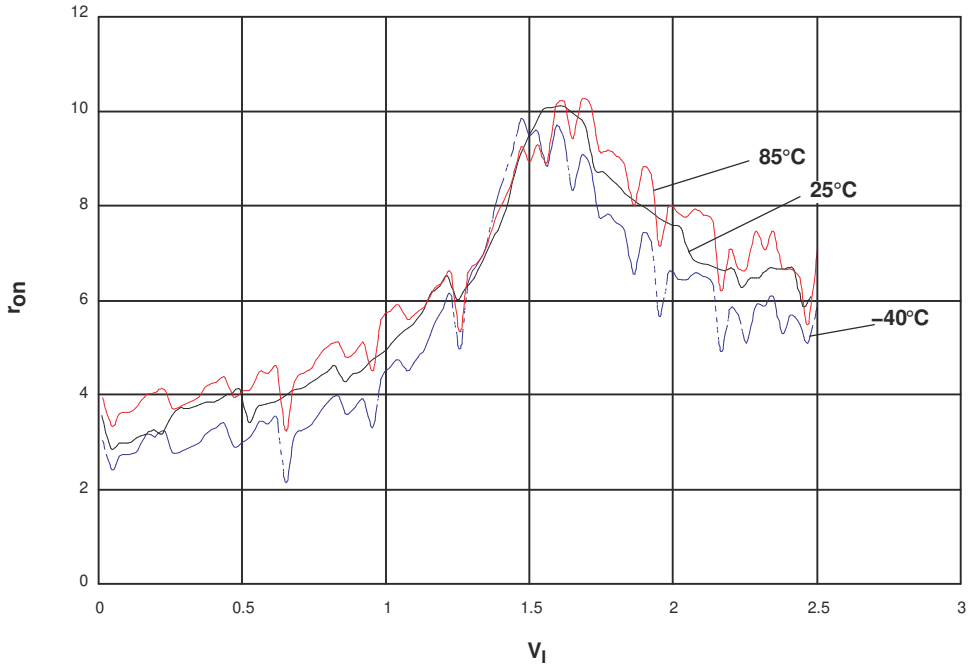


Figure 5-8. r_{on} vs. V_I, V_{CC} = 2.5 V (SN74CBTLV3125)

5.3 CB3Q Family

The switches of the CB3Q (High-Bandwidth Cross-Bar Technology) family are NMOS only, with a low and flat r_{on}. The flat characteristics of r_{on} are accomplished by a charge-pump circuit that generates a voltage of approximately 7 V at the gate of the n-channel pass transistor. As a result, 0-V to 5-V rail-to-rail switching can be accomplished because the gate-to-source voltage is well above the threshold of the n-channel transistor, and the switch is completely on over the whole 0-V to 5-V range. An internal oscillator circuit is a part of the charge-pump circuit; therefore, static power consumption of this family is higher than the CBT-C family. Dynamic power consumption depends on the frequency of the enable input. In addition to the low and flat r_{on} characteristics, this family has low input and output capacitance, making them suitable for high-performance applications. The maximum switching frequency for I/O signals depends on various factors, such as type of load, input-signal magnitude, input-signal edge rates, type of package, and so forth with a larger package, the inductance and capacitance can form a resonant circuit that may cause phase and magnitude distortion. with a large capacitive load, the RC time constant becomes higher and limits the frequency. Figure 5-9 shows a simplified schematic of a CB3Q device.

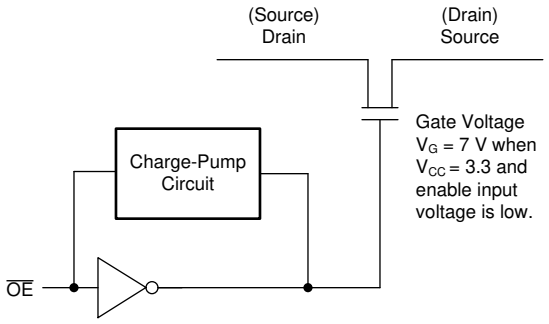


Figure 5-9. Simplified Schematic of a CB3Q device

5.3.1 Characteristics of the CB3Q Family

The following sections discuss some of the critical performance characteristics of the CB3Q3306A. The measurements setup can be found in Appendix A.

5.3.1.1 V_O vs V_I

Figure 5-10 and Figure 5-11 show the V_O vs V_I characteristics of the CB3Q3306A at different values of V_{CC} and at different temperatures. For V_{CC} = 3.6 V, the output exactly follows the input from 0 V to 5 V. Because of this characteristic, CB3Q devices can be used for switching analog and digital signals, ranging from 0 V to 5 V. For V_{CC} = 2.3 V, the gate voltage produced by the charge-pump circuit is reduced to about 4 V. So, the output approximately follows the input from 0 V to 3.3 V and becomes constant above 3.3 V.

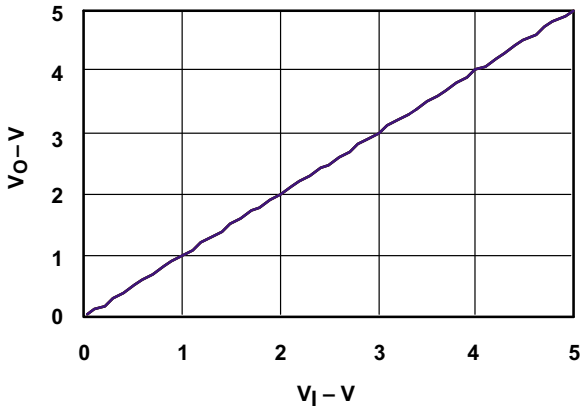


Figure 5-10. V_O vs V_I for the CB3Q3306A at V_{CC} = 3.6 V, TZ = 85°C

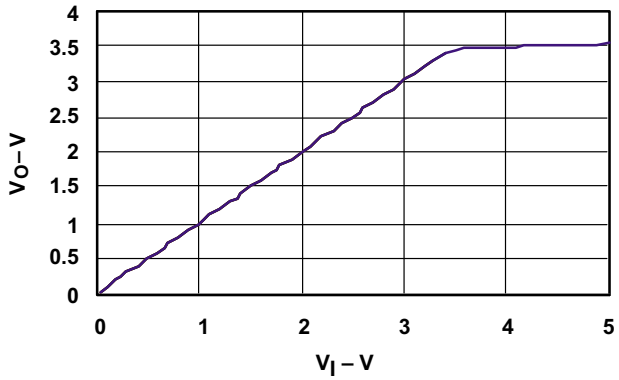


Figure 5-11. V_O vs V_I for the CB3Q3306A at V_{CC} = 2.3 V, TA = 85°C

5.3.1.2 r_{on} vs V_I

The CB3Q3306A has low and flat r_{on} characteristics. Figure 5-12 and Figure 5-13 show r_{on} versus input voltage characteristics at different values of V_{CC} and at different temperatures. The output current for r_{on} versus V_I characteristics is –15 mA, and this characteristic is dependent on output current. For V_{CC} = 3.6 V, r_{on} is fairly constant from the 0-V to 5-V input-voltage range. For V_{CC} = 2.3 V, r_{on} is flat over the range of 0 V to 2.5 V and increases rapidly above 2.5 V.

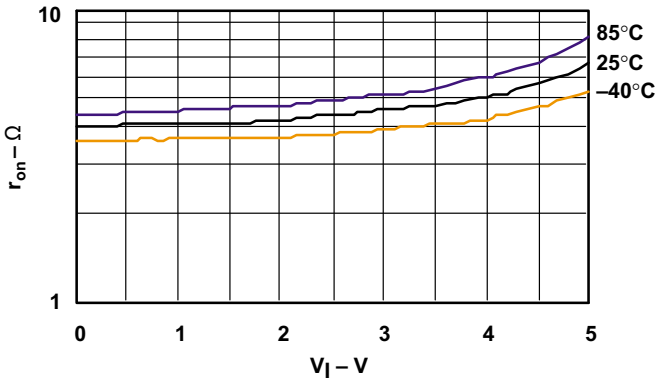


Figure 5-12. r_{on} vs V_I for the CB3Q3306A at V_{CC} = 3.6 V (IO = –15 mA)

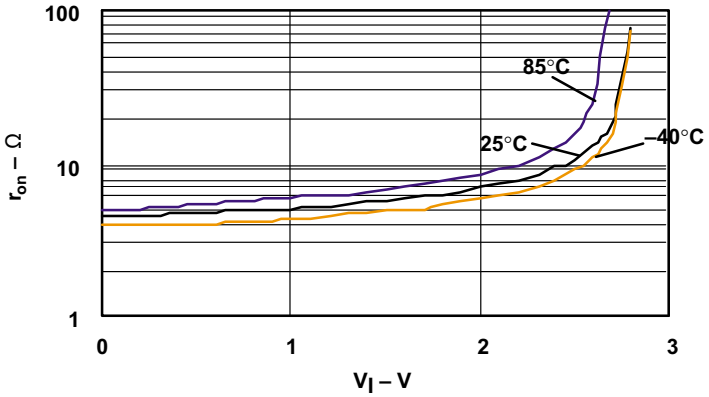


Figure 5-13. r_{on} vs V_I for the CB3Q3306A at V_{CC} = 2.3 V (IO = –15 mA)

5.3.1.3 Operation at High Frequency

Low input and output capacitance, low r_{on}, and low feed-through capacitance makes the CB3Q devices suitable for high-speed applications. Maximum frequency of operation depends on input voltage range, type of load, edge rate, type of package, off-isolation, crosstalk requirement, and so forth At high frequencies, off-isolation and crosstalk also increase, which limits the maximum frequency of operation. Figure 5-14 shows the input and output voltage waveforms at a frequency of 420 MHz, with a 500-Ω and 3-pF load. From Figure 5-14, it is clear that the switch, when on, allows high-frequency signals to pass without distortion. Also, the switch provides very good isolation between the input and output when it is turned off or disabled.

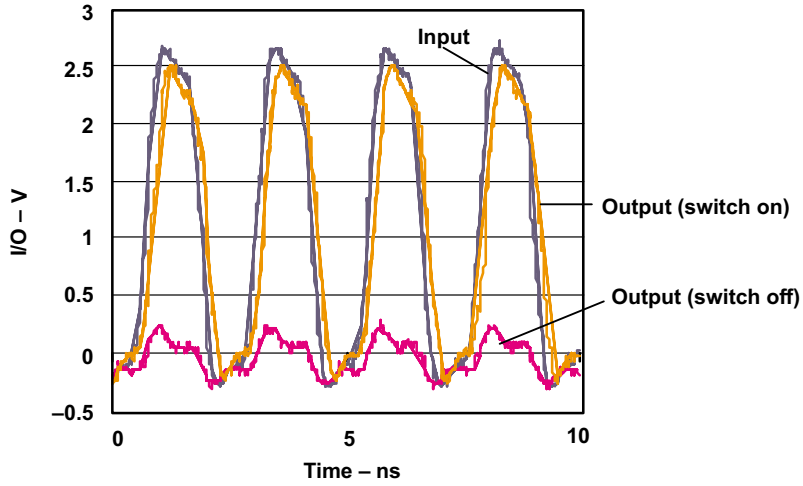


Figure 5-14. Input and Output Voltage Waveforms for the CB3Q3306A at 420 MHz (V_{CC} = 3.3 V)

5.3.1.4 Output Skew

Output skew is a measure of the variation of r_{on} over the channels in a multi bit switch. This is specifically significant when switching differential signals. For minimal signal distortion and noise in differential signaling, the variation of r_{on} should be as small as possible. Output skew at a specific voltage can be determined by measuring the time difference of the output voltage at various channels. Figure 5-15 and Figure 5-16 show the output voltage of the CB3Q3306A at different channels. Output skew can be determined from this graph. For example, for –40°C at 2.5 V, the skew is approximately 30 ps, which is fairly constant from 2.2 V to 2.6 V. For 100°C, the output skew is approximately 40 ps, which is fairly constant from 2.2 V to 2.6

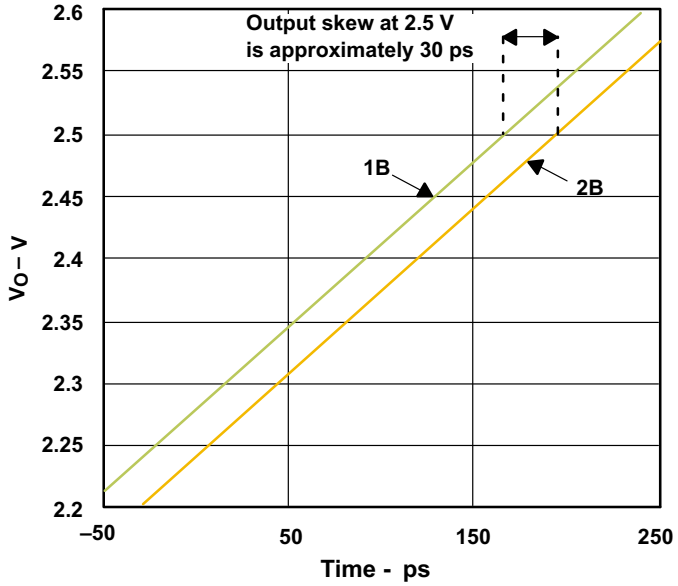


Figure 5-15. Output Skew at –40°C (V_{CC} = 3.3 V)

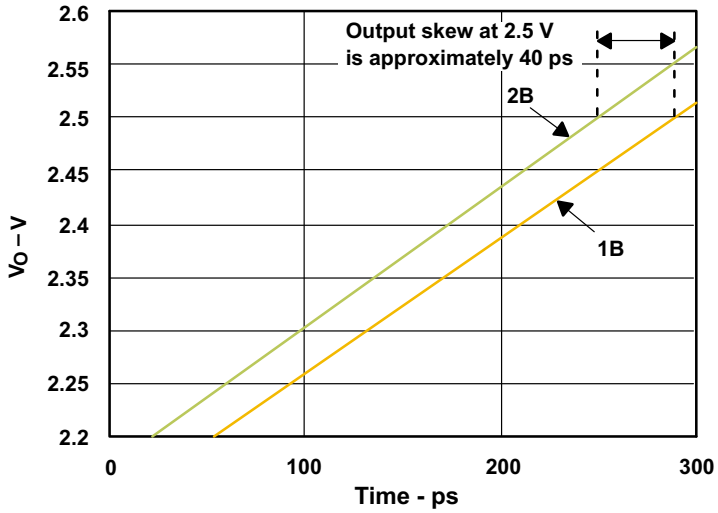


Figure 5-16. Output Skew at 100°C (V_{CC} = 3.3 V)

5.3.1.5 Frequency Response

Figure 5-17 and Figure 5-17 show the attenuation and off-isolation for the CB3Q3306A at different loads as a function of frequency. The bandwidth depends on the type of load, and bandwidth decreases as the load increases.

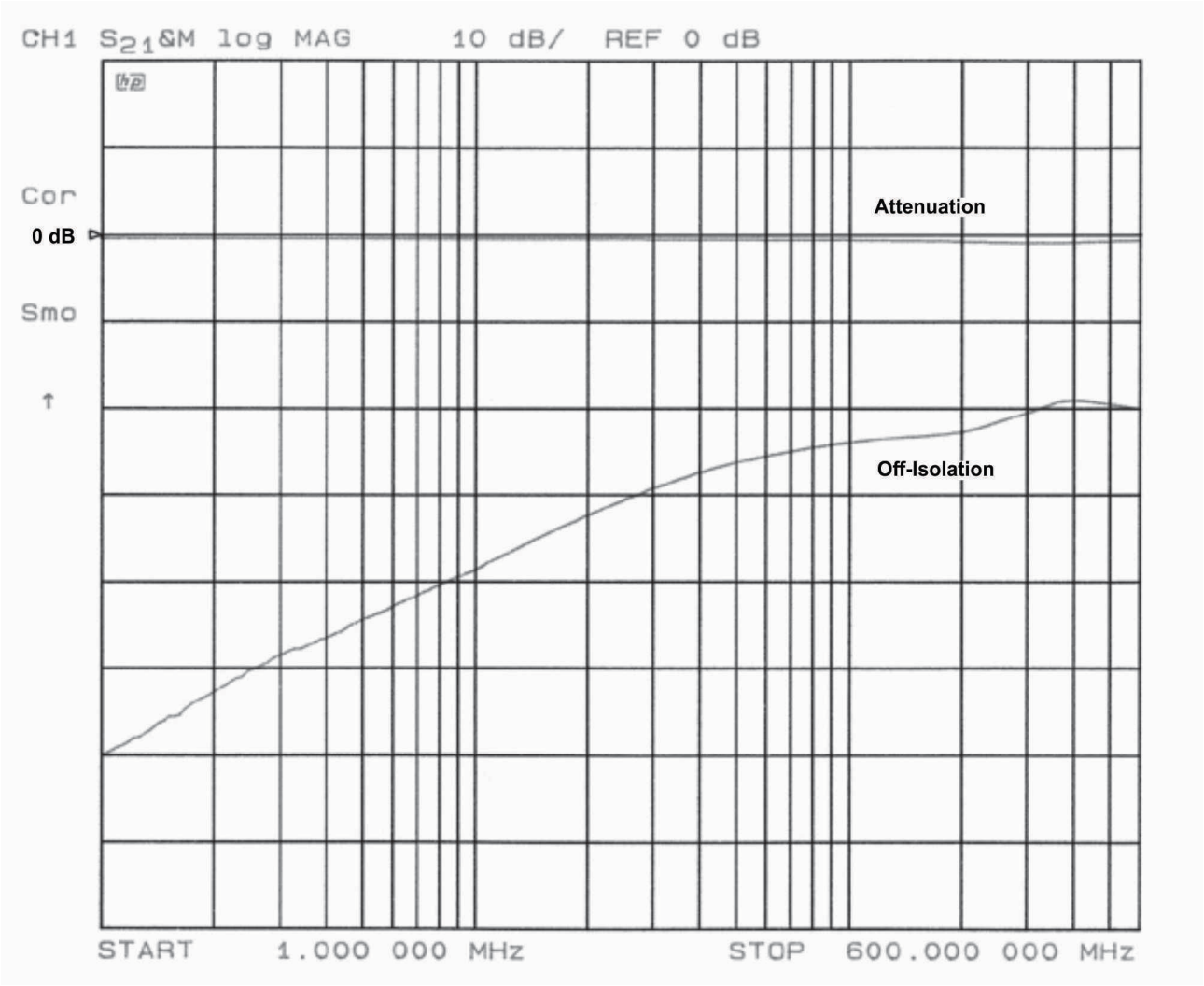


Figure 5-17. Attenuation and Off-Isolation for the CB3Q3306A at 3-pF (V_{CC} = 3.3 V)

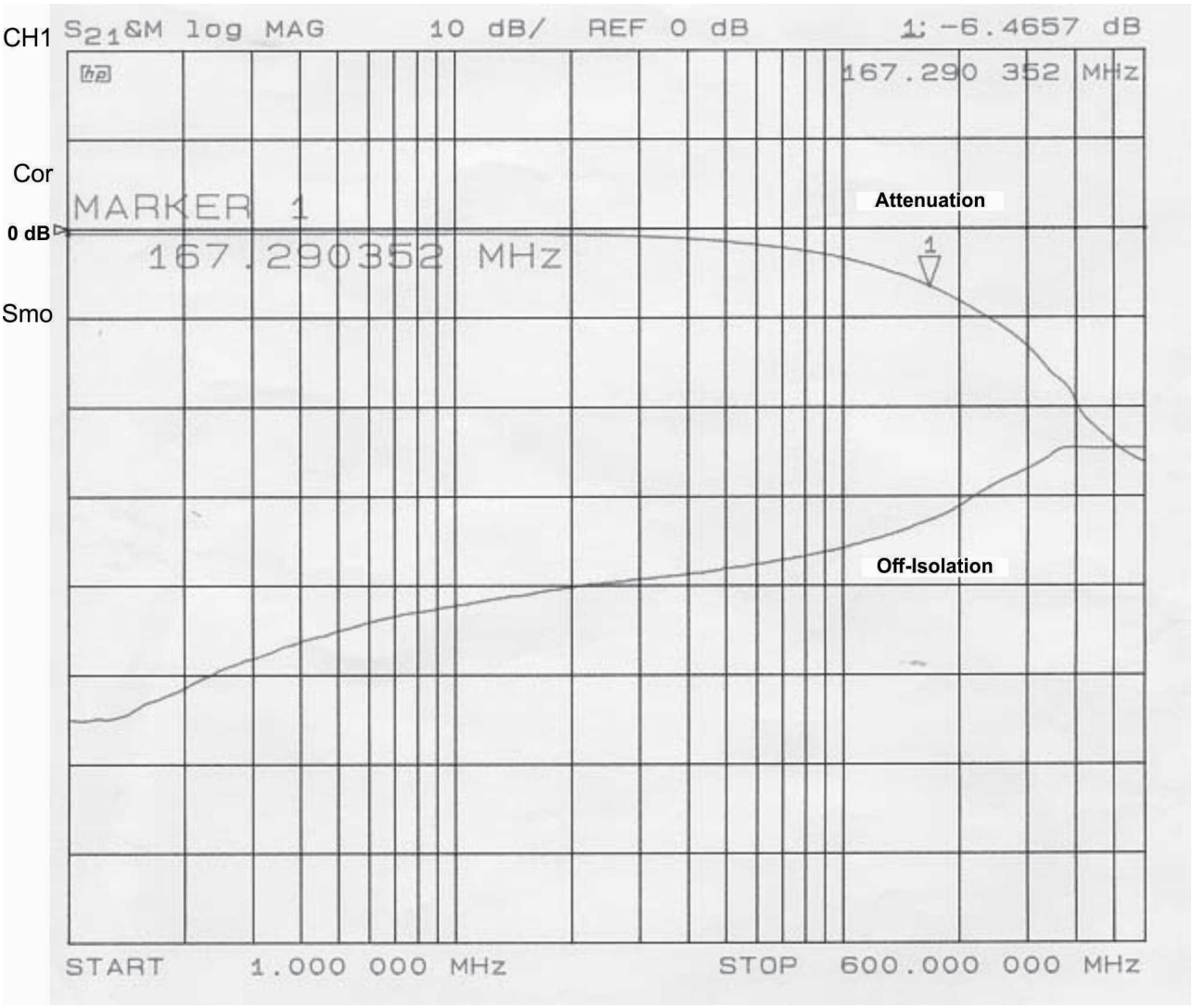


Figure 5-18. Attenuation and Off-Isolation for the CB3Q3306A at 50-pF (V_{CC} = 3.3 V)

5.3.1.6 Adjacent Channel Crosstalk

For some applications, crosstalk is an important parameter. Figure 5-19 shows the crosstalk between adjacent channels in the CB3Q3306A.

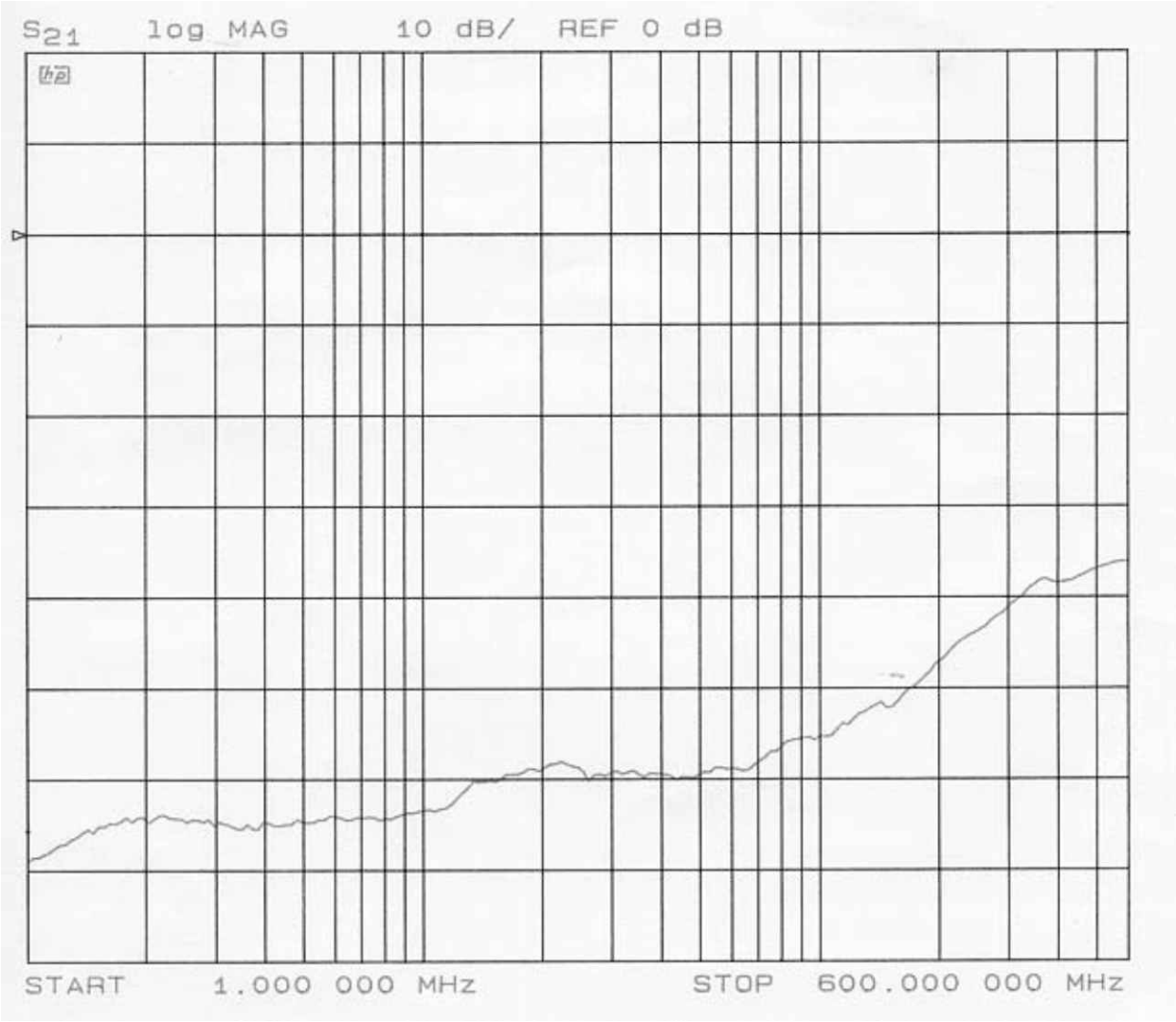


Figure 5-19. Crosstalk of the CB3Q3306A at 3-pF Load (V_{CC} = 3.3 V)

5.3.2 Application of the CB3Q Family

5.3.2.1 Multiplexer in USB Applications

Figure 5-20 shows a USB 2.0 application in which a bus-switch device can be used. The first switch in a notebook PC is used to isolate between a notebook PC and the docking station. The switches on the docking station are used as a multiplexer to provide two different paths for the DATA+ and DATA– signals. If the operating system is Windows 95, the USB 2.0 hub is not supported. Switches 1 and 2 are on, and the USB line is connected directly to Port 1. Figure 5-21 shows the use of a CB3Q3257 in this type of application.

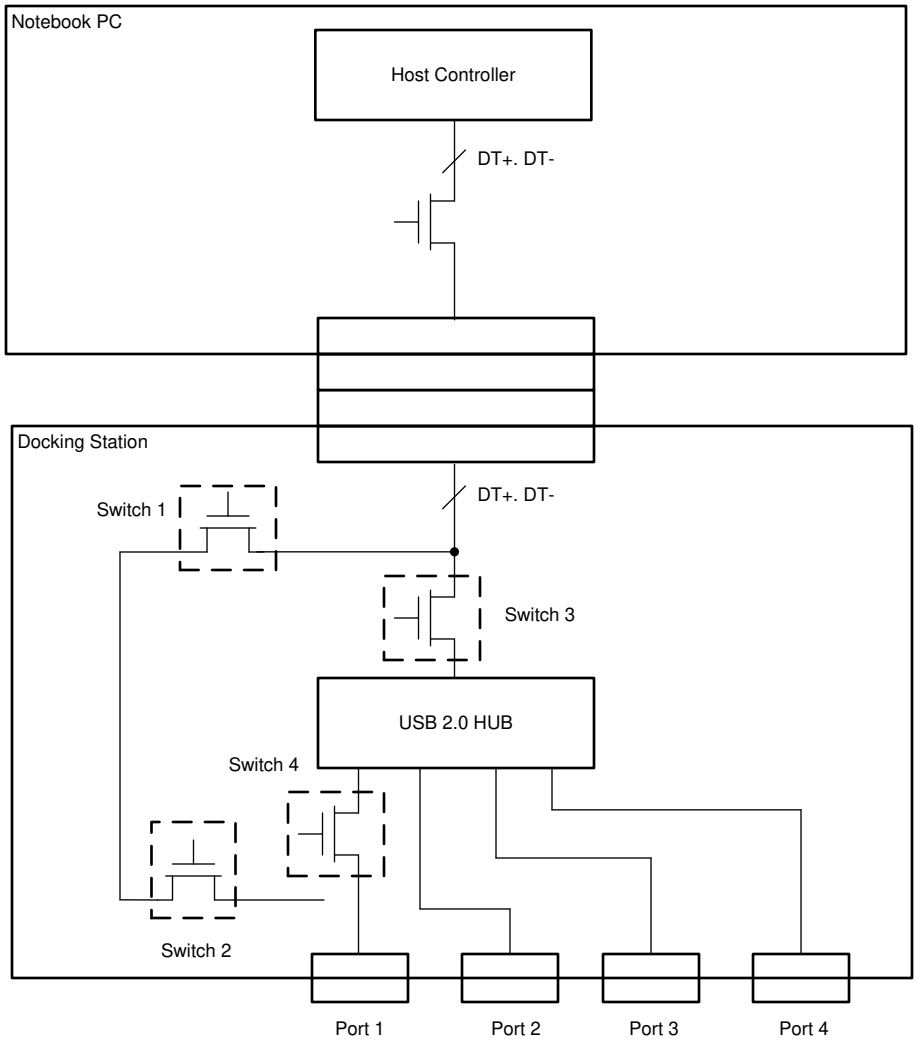
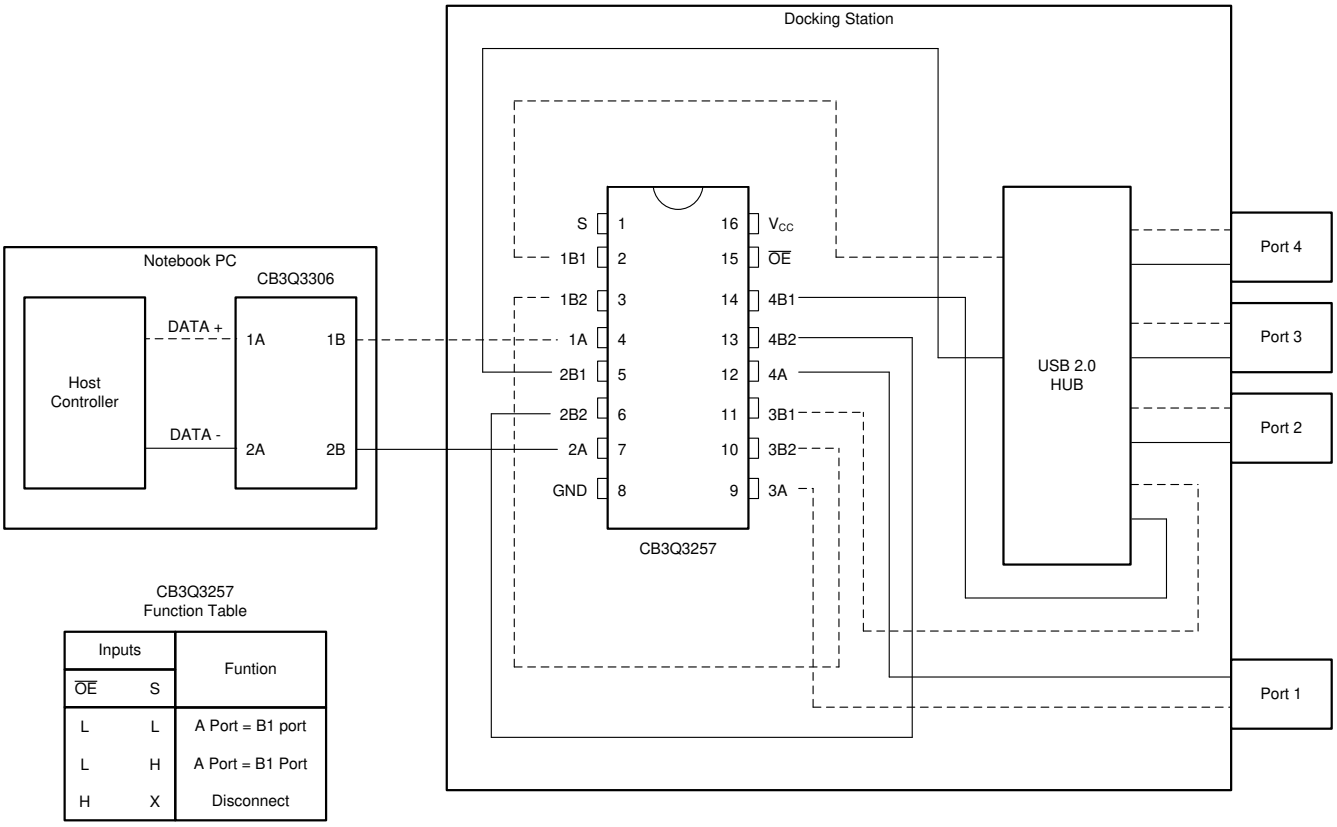


Figure 5-20. Multiplexing in a USB Application



CB3Q3257 Function Table

Inputs		Funtion
$\overline{OE}$	S	
L	L	A Port = B1 port
L	H	A Port = B1 Port
H	X	Disconnect

Figure 5-21. CB3Q3257 in a USB Application

DATA+ signal path is shown as a dotted line and the DATA– signal is shown as a solid line. The DATA+ signal goes to 1A. Depending on the select signal (S) levels, the output can be 1B1 or 1B2. When S is low, DATA+ from the host controller is connected to the port through the USB 2.0 hub (1A → 1B1 → USB 2.0 Hub → 3B1 → 3A → Port 1). When S is high, the DATA+ is connected to port 1 directly (1A → 1B2 → 3B2 → 3A). Similarly, DATA– uses the 2A, 2B1, 2B2 and 4A, 4B1, 4B2 switches for connecting to port 1.

5.4 CB3T Family

The CB3T (Cross-Bar Translating) family is a voltage-translation bus-switch family. This family can operate with a power-supply voltage range of 2.3 V to 3.6 V. When V_{CC} = 3.3 V, the device can translate from a 5-V input to a 3.3-V output. In addition, when V_{CC} = 2.3 V the device can translate from 5-V or 3.3-V inputs to a 2.3-V output. The CB3T family can be used for voltage translation at moderately high frequencies. Figure 5-22 shows the simplified structure of the CB3T3306.

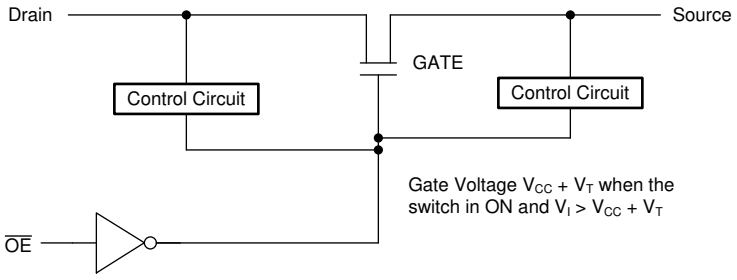


Figure 5-22. Simplified Structure of the CBT3306

When the switch is on, the voltage at the gate of the NMOS pass transistor in the CB3T3306 is biased at V_{CC} + V_T, where V_T is the threshold voltage of the NMOS. When input voltage starts to rise from low to high, the output follows the input voltage. As the input voltage reaches about one-half of V_{CC}, the control circuit senses this voltage and pulls the output voltage close to the V_{CC} level and keeps the voltage constant as the input voltage increases. When the input reaches V_{CC} + V_T, the output voltage again increases to V_{CC} and remains

nearly flat, as the input voltage continues to rise. Input voltages at which these transitions occur depend on the output current, power supply, temperature, and transistor characteristics. The level of output high voltage (V_{OH}) also depends on the output current.

5.4.1 Characteristics of the CB3T Family

The following paragraphs discuss some of the critical performance characteristics of the CB3T3306. The measurements setup is given in Appendix A.

5.4.1.1 V_O vs V_I

Figure 5-23 and Figure 5-24 show the output voltage vs input voltage (V_O vs V_I) characteristics of the CB3T3306 for different values of V_{CC}. The rapid increase in output voltage is due to the control circuit sensing the output voltage and pulling it high, close to the V_{CC} level. The slope of this rapid rise in the curve depends on the output current being drawn from the switch.

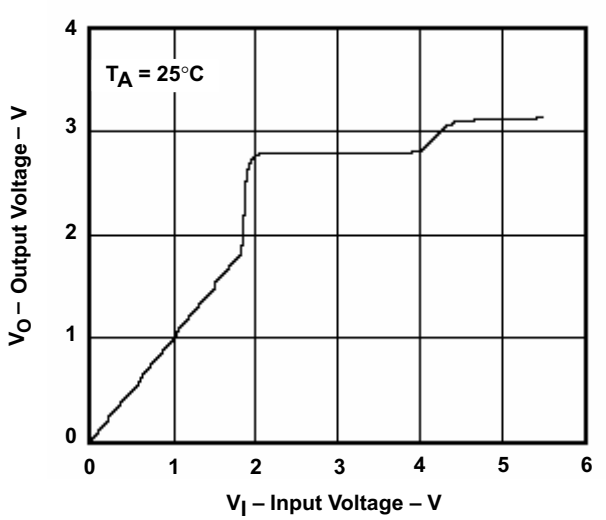


Figure 5-23. V_O vs V_I in the CB3T3306 at IO = –1 µA (V_{CC} = 2.3 V)

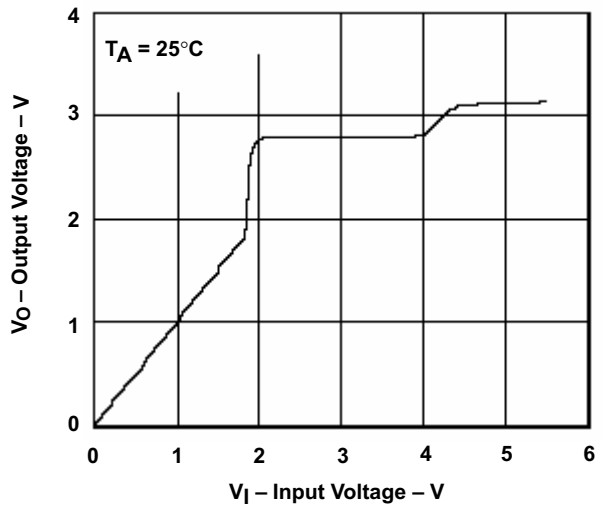


Figure 5-24. V_O vs V_I in the CB3T3306 at IO = –1 µA (V_{CC} = 3.0 V)

5.4.1.2 r_{on} vs V_I

Figure 5-25 and Figure 5-26 shows the r_{on} versus V_I characteristics of the CB3T3306 at different V_{CC} voltages. r_{on} increases rapidly when the input voltage crosses approximately one-half of V_{CC} and becomes flat above that voltage. The value of r_{on} above that voltage depends greatly on the output current. As the output current increases, r_{on} decreases.

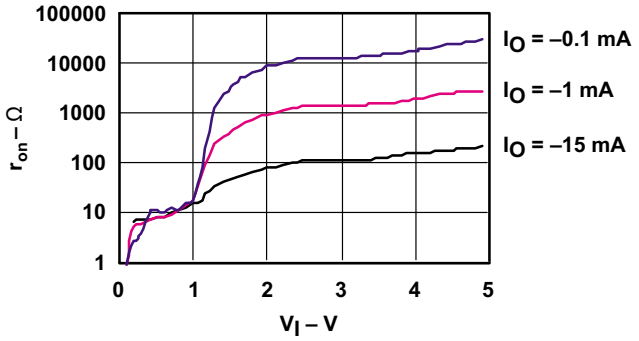


Figure 5-25. r_{on} vs V_I for the CB3T3306 at V_{CC} = 2.3 V

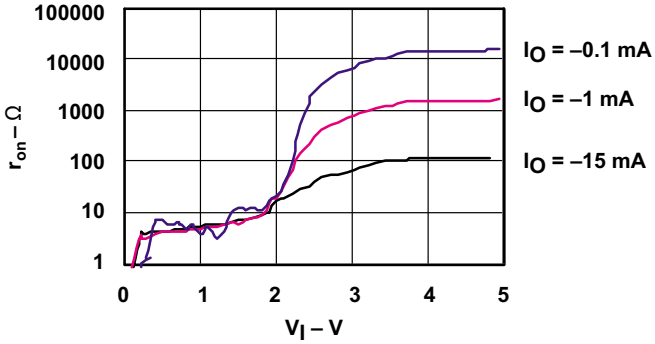


Figure 5-26. r_{on} vs V_I for the CB3T3306 at V_{CC} = 3.6 V

5.4.1.3 Operation at High Frequency

CB3T devices can be used for voltage translation at moderately high frequencies. Figure 5-27 shows the operation of the CB3T3306 at 200 MHz. The load is 500 Ω and 3 pF to ground. Like the CB3Q family, the maximum I/O switching frequency depends on various factors, such as type of load, input signal magnitude, input signal edge rates, type of package, and so forth with a larger package, the inductance and capacitance can form a resonant circuit that may cause phase and magnitude distortion. with a large capacitive load, the RC time constant becomes higher and limits the practical operating frequency.

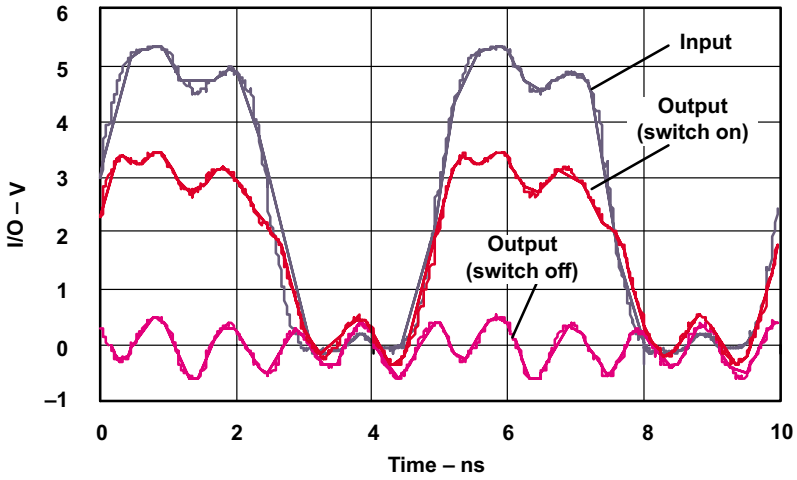


Figure 5-27. Input and Output Voltage Waveforms at 200 MHz (V_{CC} = 3.3 V)

5.4.2 Application of the CB3T Family

5.4.2.1 Voltage Translation for an External Monitor Terminal in a Notebook PC

Figure 5-28 shows a typical application for the level-translation feature of the CB3T3306. The CB3T3306 is used as a voltage translator between a monitor and a graphic controller. Data transfer between these two systems

is bidirectional, while the clock signal transfer is unidirectional and flows only from graphic controller to monitor. Pullup resistors are used for translating from low to high.

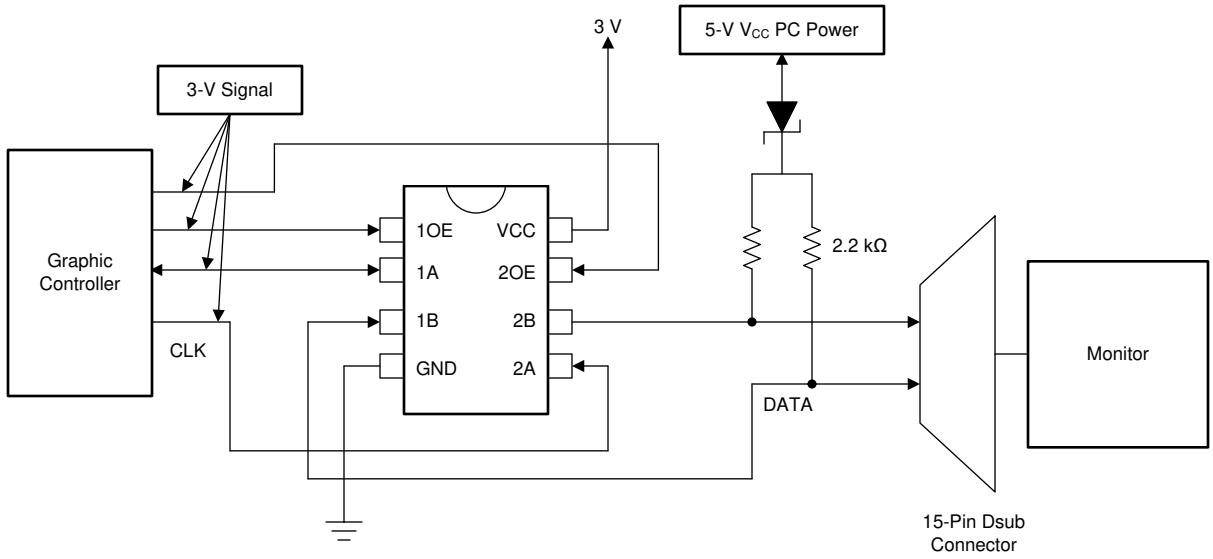


Figure 5-28. Data and Clock-Signal Data Transfer Using the CB3T3306

6 Applications

The digital bus switches offered in TI's portfolio of devices are offered in different configurations. Figure 6-1 shows the three main configurations of bus switches: a two-port configuration (A and B are either connected or isolated), a MUX/deMUX configuration (1A is connected either to 1B1 or 1B2), or bus exchange (buses 1 and 2 are either passed unchanged or are exchanged with each other).

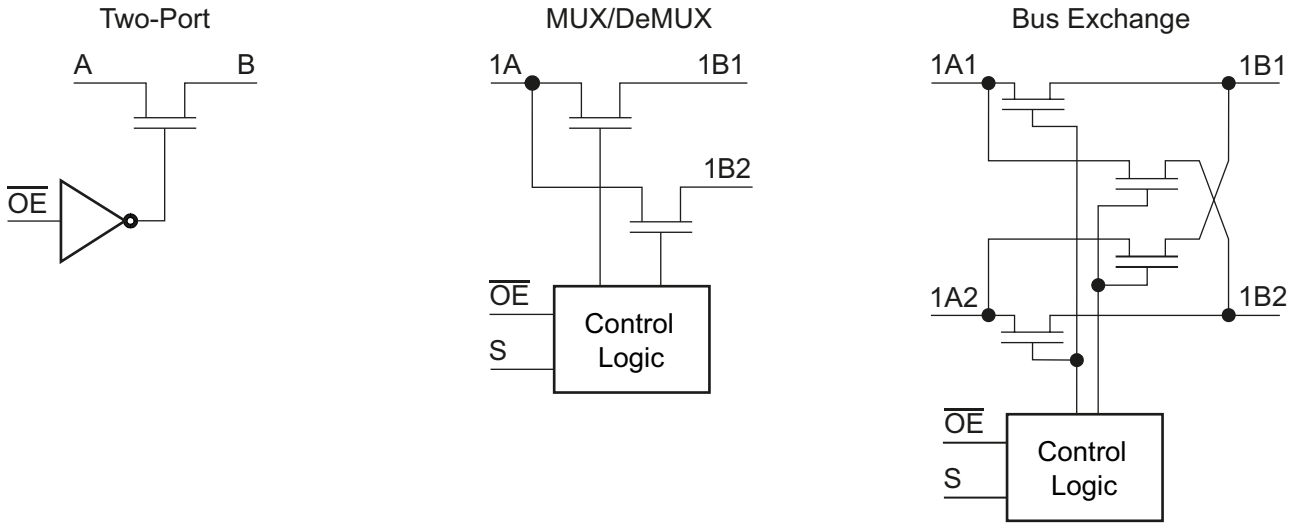


Figure 6-1. Bus Switch Functions

6.1 Multiplexing USB Peripherals

Figure 6-2 shows an application of the CB3Q3125 being used to switch two different USB peripherals.

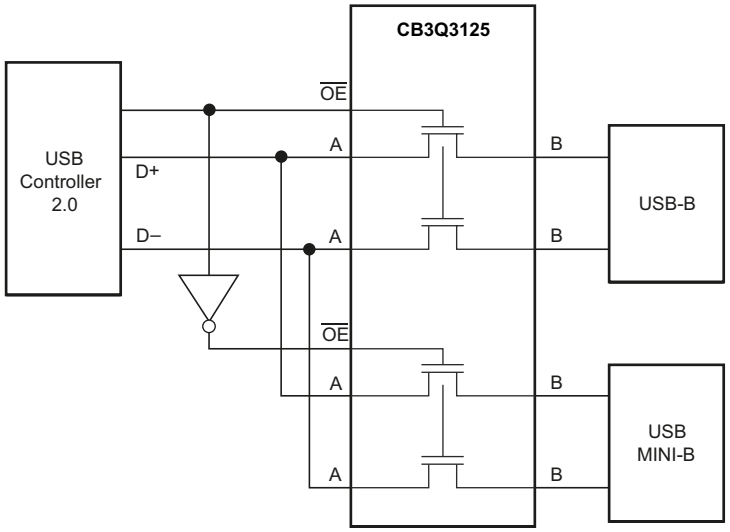


Figure 6-2. Multiplexing USB Peripherals

6.2 Multiplexing Ethernet

Figure 6-3 shows a fairly common application in telecom designs where two 16-bit/channel Ethernet buses are being MUXed and deMUXed to one commonly-shared Ethernet bus.

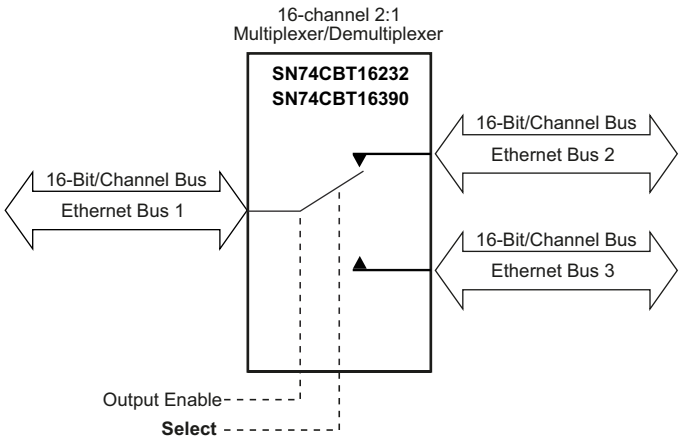


Figure 6-3. Multiplexing Ethernet

6.3 Notebook Docking Station

Bus switches are often used for docking notebook computers into their docking station. The CBTD16210 is optimized for this application with flow-through pin outs and dual 10-bit bus switches with separate enable inputs, which can be used as two 10-bit switches or on a 20-bit switch. The CBTD16210 provides 5 V to 3.3 V bidirectional level shifting for applications where the 5 V docking station chipset needs to interface with the lower-voltage 3.3 V notebook chipset. The CBTLV16210 could be used for pure 3.3 V systems. Figure 6-4 shows this implementation.

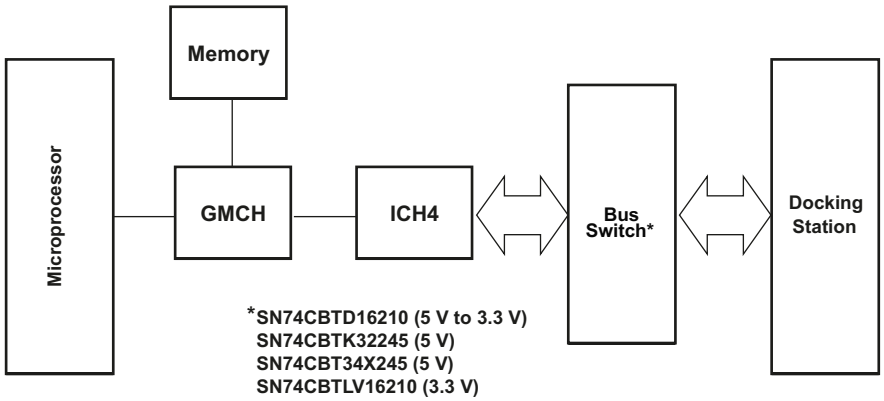


Figure 6-4. Notebook Docking Station

7 Conclusion

Along with the applications described above, TI's CBT-C and CB3Q signal switches can be used for various types of high-speed applications, such as hot insertion for PCI interface, LAN signaling, I^2C bus expansion, video switching, and more. CB3T devices can be used for high-speed voltage translation in a mixed-voltage system. This application report has discussed some of the application performance characteristics of TI's high-speed signal switches that are critical for the previously mentioned applications.

8 References

- Selecting the Right Texas Instruments Signal Switch, John Perry and Chris Cockrill.
- 5-V to 3.3-V Translation with the SN74CBTD3384, Nalin Yogasundram.
- Texas Instruments Solution for Undershoot Protection for Bus Switches, Nadira Sultana and Chris Graves.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (June 2021) to Revision C (November 2021)	Page
• Added Power and Control Voltage Requirements topic	7
• Added Rail-to-Rail Operation topic	7
• Updated title from *Enable and Disable Delays* to *Enable and Disable Delays and Propagation Delay*	10
• Added Characteristics of CBTLV Family topic	17
• Added Applications section	30

Changes from Revision A (June 2020) to Revision B (June 2021)	Page
• Updated the numbering format for tables, figures and cross-references throughout the document	3

Changes from Revision * (July 2003) to Revision A (June 2020)	Page
• Added link to SZZA030	1

A Test Measurement Circuits

A.1 Measurement Setup for r_{on}

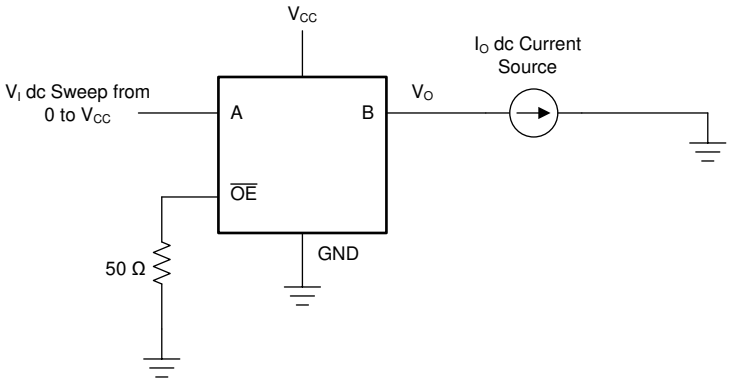


Figure A-1. r_{on} Measurement Setup

A.2 Measurement Setup for V_O vs V_I Characteristics

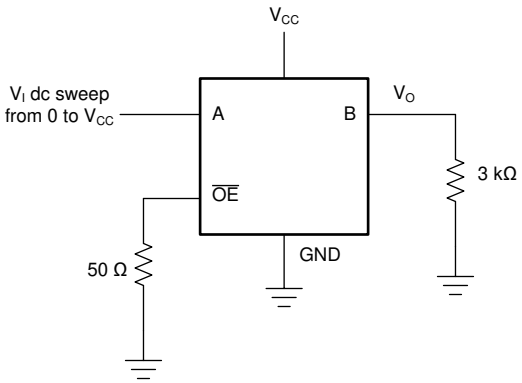


Figure A-2. V_O vs V_I Measurement Setup

A.3 Voltage-Time Waveform Measurement (Switch On)

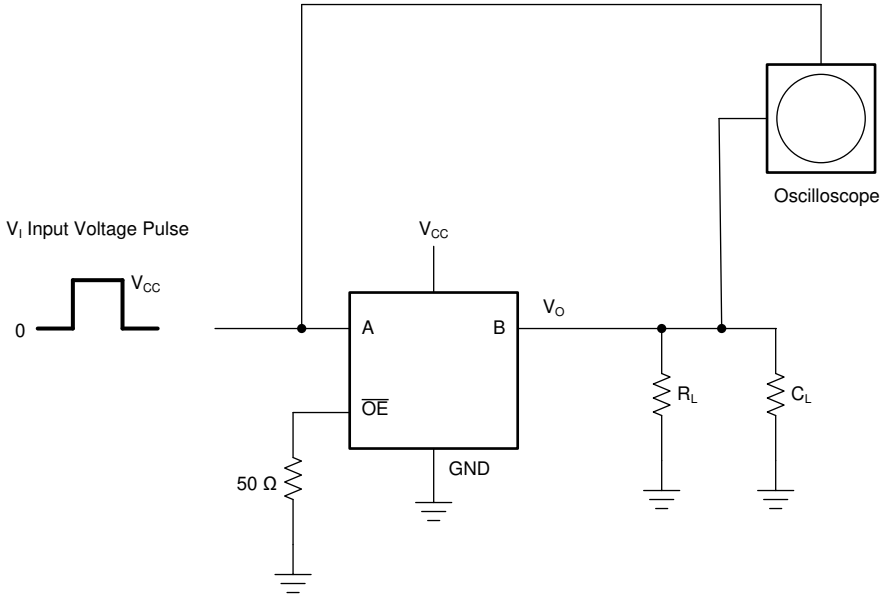


Figure A-3. Voltage-Time Waveform Measurement (Switch On)

A.4 Voltage-Time Waveform Measurement (Switch Off)

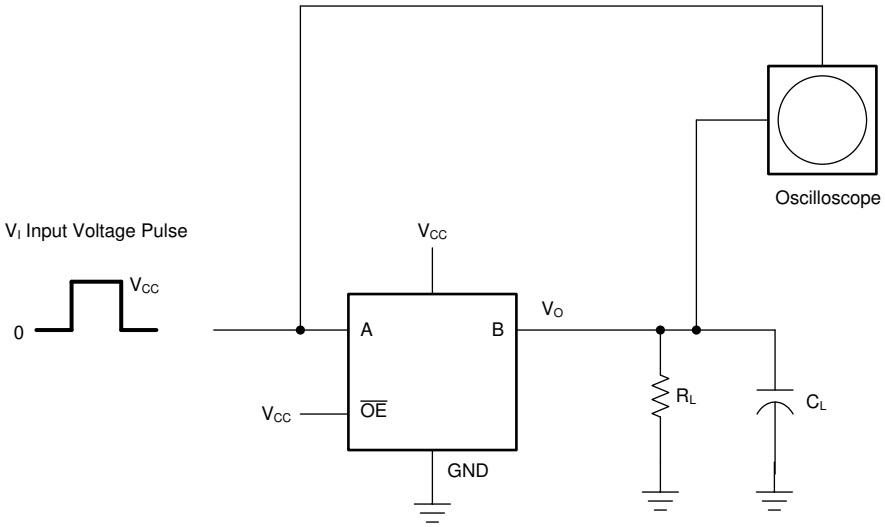


Figure A-4. Voltage-Time Waveform Measurement (Switch Off)

A.5 Output-Skew Measurement

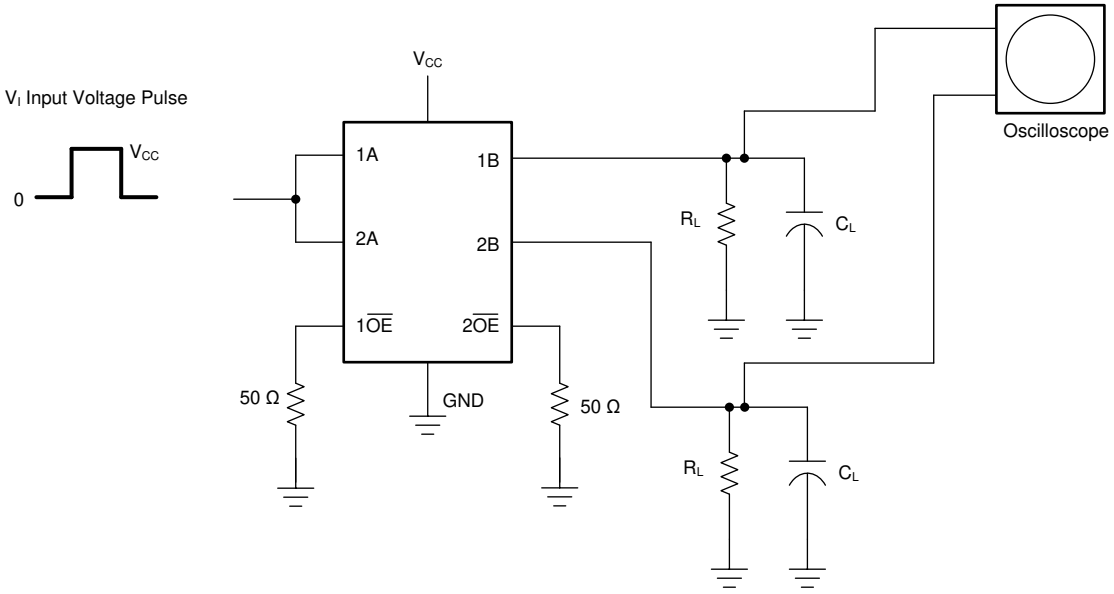


Figure A-5. Output-Skew Measurement Setup

A.6 Simulation Setup for Undershoot Measurement

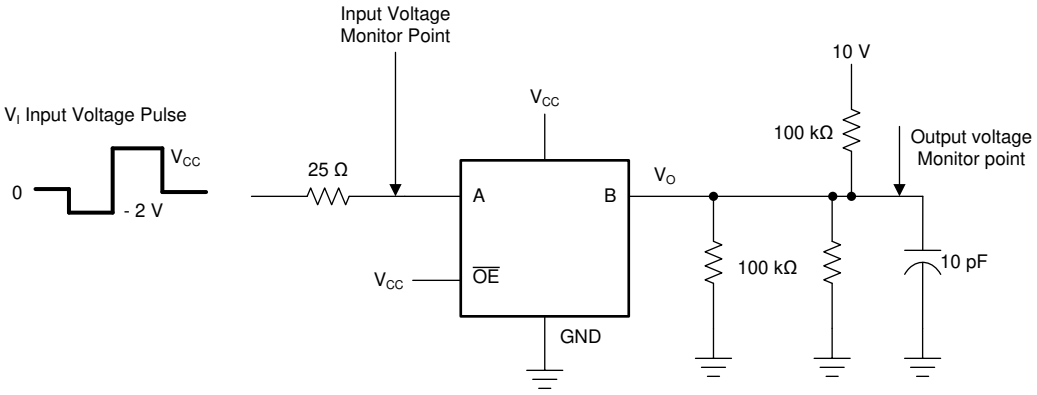


Figure A-6. SPICE Simulation Setup for Undershoot Measurement

A.7 Laboratory Setup for Attenuation Measurement

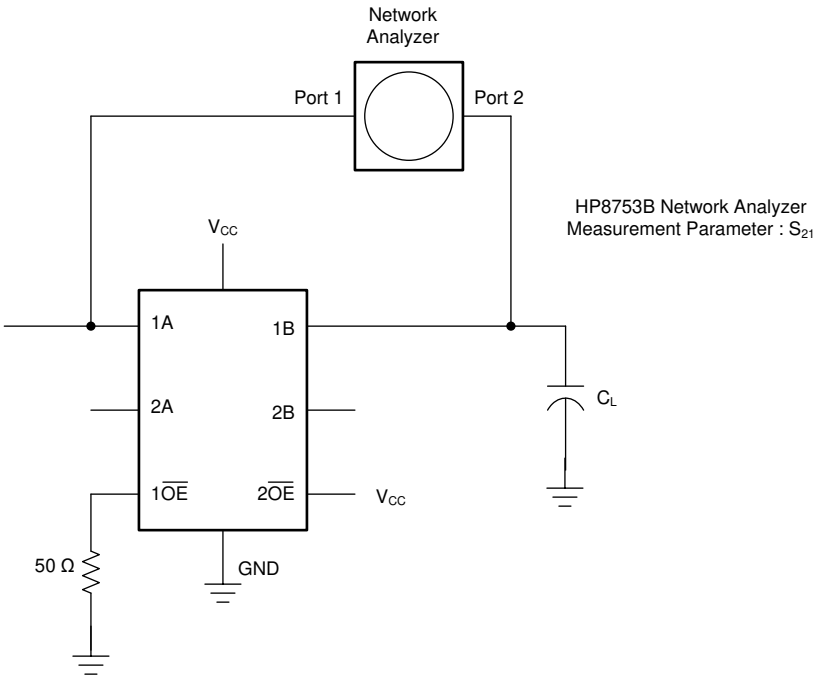


Figure A-7. Attenuation Measurement Setup

A.8 Laboratory Setup for Off Isolation Measurement

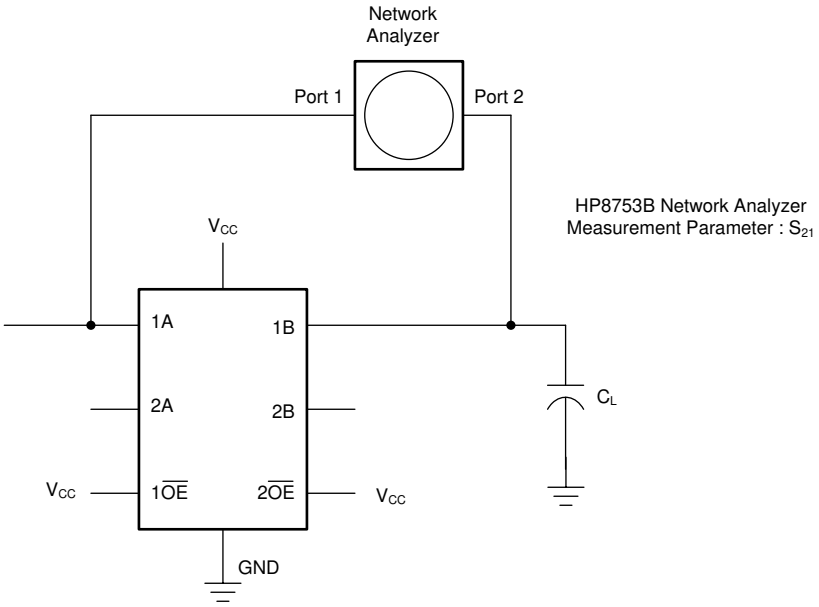


Figure A-8. Off Isolation Measurement Setup

A.9 Laboratory Setup for Crosstalk Measurement

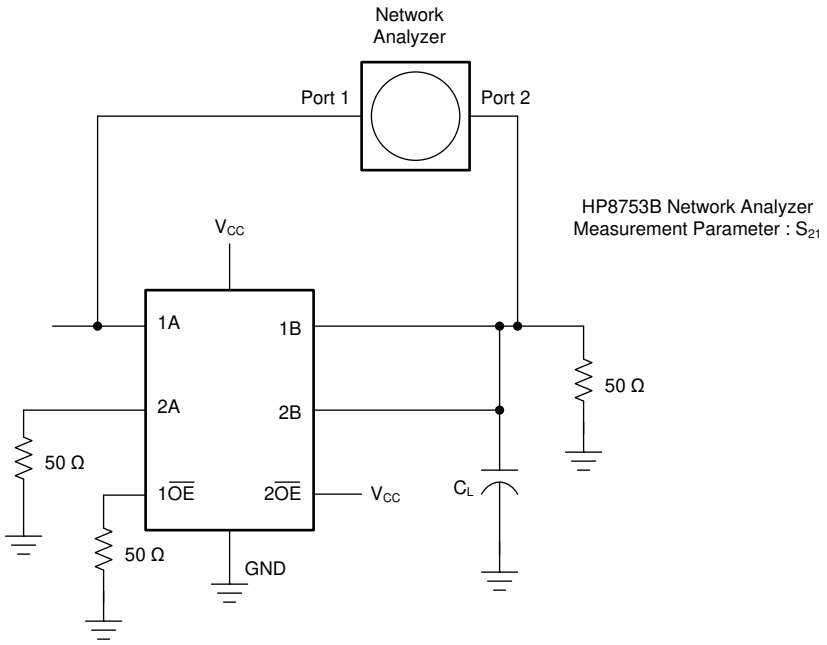


Figure A-9. Adjacent-Channel Crosstalk Measurement

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