bq24153A/56A/57/58/59 Fully Integrated, Switch-Mode, One-Cell, Li-Ion Charger With Full USB Compliance and USB-OTG Support EVM

The bq24153A/56A/57/58/59 evaluation module is a complete charger module for evaluating compact, flexible, high-efficiency, USB-friendly, switch-mode charge management solution for single-cell Li-ion and Li-polymer batteries used in a wide range of portable applications.

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1 Introduction

1.1 EVM Features

- Evaluation module (EVM) for bq24153A/56A/57/58/59
- High-efficiency fully integrated NMOS-NMOS synchronous buck charger with 3-MHz frequency
- Integrated power FETs for up to 1.55-A charge rate
- Programmable battery voltage, charge current, and input current via I^{2}C™ interface
- Input operating range 4 V – 6 V
- Boost-mode operation for USB OTG
- LED indication for status signals
- Test points for key signals available for testing purposes. Easy probe hook-up
- Jumpers available. Easy-to-change connections.

1.2 General Description

The bq24153A/56A/57/58/59 evaluation module is a complete charger module for evaluating compact, flexible, high-efficiency, USB-friendly, switch-mode charge management solution for single-cell Li-ion and Li-polymer batteries used in a wide range of portable applications.

The bq24153A/56A/57/58/59 integrates a synchronous PWM controller, power MOSFETs, input current sensing, high-accuracy current and voltage regulation, and charge termination, into a small WCSP package. The charge parameters can be programmed through an I^{2}C interface.

For details, see the bq24153A/56A/58/59 data sheet (SLUSAB0) and the bq24157 datasheet (SLUSAX5).

1.3 I/O Description

Jack	Description
J1–DC+	AC adapter or USB, positive output
J1–DC–	AC adapter or USB, negative output
J2–BAT–	Battery negative terminal; connect to DC-
J2-AUXPWR/CD	Connect to AUXPWR pin or CD pin
J2-BAT+	Charger positive output; connect to CSOUT pin
J3–SCL	I^{2}C clock; connect to SCL pin
J3–SDA	I^{2}C data; connect to SDA pin
J3–DC–	AC adapter or USB, negative output
J4–STAT	Status output; can be connected to STAT pin by JMP1 set to EXT (2-3)
J4–OTG/SLRST	Connect to OTG/SLRST pin
J4–DC–	AC adapter or USB, negative output

1.4 Control and Key Parameters Setting

Jack	Description	Factory Setting
JMP1	LED 1-2: Connect STAT pin to LED on EVM EXT 2-3: Connect STAT pin to J4-1	Jumper on LED (1-2)
JMP2	HI 1-2: OTG or SLRST high (input or battery voltage) LO 2-3: OTG or SLRST low (ground)	See Table 1
JMP3	J2-BAT+ connect to J2-AUXPWR/CD	
JMP4	AUXPWR/CD pin connect to high or low or float	
JMP5	OTG/SLRST pin 10-kΩ resistor to ground or float	Jumper ON

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1.5 Recommended Operating Conditions

		Min	Typ	Max	Unit
Supply voltage, V_{IN}	Input voltage from ac adapter input	4	5	6	V
Battery voltage, V_{BAT}	Voltage applied at VBAT terminal of J8	0	3-4.2	4.44	V
Supply current, I_{AC}	Maximum input current from ac adapter input	0.1	0.1–0.5	1.5	A
Charge current, I_{chrg}	Battery charge current	0.325	0.7	1.55	A
Operating junction temperature range, T_J		0		125	°C

2 Test Summary

This procedure details how to configure the HPA697 evaluation board for bench evaluation. An electronic load is used to simulate a battery.

2.1 Definitions

This procedure details how to configure the HPA697 evaluation board. The following naming conventions are followed. See the bq24153A/56A/57/58/59EVM (also know as HPA697) schematic for details.

VXXX :	External voltage supply name (VADP, VBT, VSBT)
LOADW:	External load name (LOADR, LOADI)
V(TPyyy):	Voltage at internal test point TPyyy. For example, V(TP12) means the voltage at TP12.
V(Jxx):	Voltage at jack terminal Jxx
V(TP(XXX)):	Voltage at test point XXX. For example, V(ACDET) means the voltage at the test point which is marked as ACDET.
V(XXX, YYY):	Voltage across point XXX and YYY.
I(JXX(YYY)):	Current going out from the YYY terminal of jack XX.
Jxx(BBB):	Terminal or pin BBB of jack xx
Jxx ON :	Internal jumper Jxx terminals are shorted
Jxx OFF:	Internal jumper Jxx terminals are open
Jxx (-YY-)	ON: Internal jumper Jxx adjacent terminals marked as YY are shorted
Measure: → A,B	Check specified parameters A, B. If measured values are not within specified limits the unit under test has failed.
Observe → A,B	Observe if A, B occur. If they do not occur, the unit under test has failed.

Assembly drawings have location for jumpers, test points, and individual components.

2.2 Recommended Test Equipment

2.2.1 Power Supplies

Power Supply #1 (PS#1): a power supply capable of supplying 5 V at 2 A is required.

2.2.2 Load #1

A 10-V (or above), 2-A (or above) electronic load that can operate in constant current mode.

2.2.3 Load #2

A 10-V (or above), 2-A (or above) electronic load that can operate in constant voltage mode or a source meter to simulate a battery.

2.2.4 Meters

Two equivalent voltage meters and two equivalent current meters. The current meters must be able to measure 2-A current.

2.2.5 Computer

A computer with at least one USB port and a USB cable. The bq24153_6_8 evaluation software must be properly installed.

2.2.6 HPA172 Communication Kit (USB TO GPIO)

A HPA172 USB to I2C communication kit.

2.2.7 Software

Download BQ24153_6_8Setup.zip from the charger's product folder, unzip the file and double-click on the "SETUP.EXE" file. Follow the installation steps.

2.3 Recommended Test Equipment Setup

1. Set Power Supply #1 for 5 V ± 100 mVdc, 2-A. ±0.1-A current limit, and then turn off supply.
2. Connect the output of Power Supply #1 in series with a current meter (multimeter) to J1 (DC+, DC−).
3. Connect a voltage meter across J1 (DC+, DC−).
4. Connect the Load #2 in series with a current meter (multimeter) to J2 (BAT+, BAT−). Ensure that a voltage meter is connected across J2 (BAT+, BAT−). Turn on the Load #2. Use the constant voltage mode. Set the output voltage to 2.5 V.
5. Turn off Load #2.
6. Connect J5 to HPA172 kit by the 10-pin ribbon cable. Connect the USB port of the HPA172 kit to the USB port of the computer. The connections are shown in Figure 1.
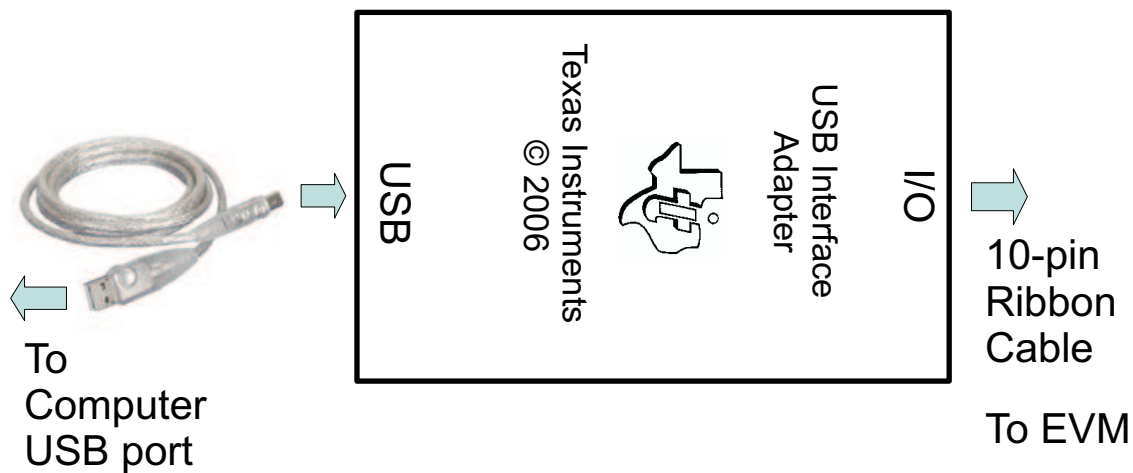

Figure 1. Connections of HPA172 Kit

7. Install jumpers per Table 1

Table 1. Factory Jumper Settings

Spin	JMP1	JMP2	JMP3	JMP4	JMP5
HPA256-001 (bq24153A)	(-LED-) ON	(-LO-) ON	OFF	(-LO-) ON	ON
HPA256-002 (bq24156A)	(-LED-) ON	(-HI-) ON	OFF	(-LO-) ON	ON

Table 1. Factory Jumper Settings (continued)

Spin	JMP1	JMP2	JMP3	JMP4	JMP5
HPA256-003 (bq24158)	(-LED-) ON	(-LO-) ON	OFF	(-LO-) ON	ON
HPA256-003 (bq24157)	(-LED-) ON	(-LO-) ON	OFF	(-LO-) ON	ON
HPA256-003 (bq24159)	(-LED-) ON	(-HI-) ON	OFF	(-LO-) ON	ON

8. After the preceding steps, the test setup for HPA697 is shown in Figure 2
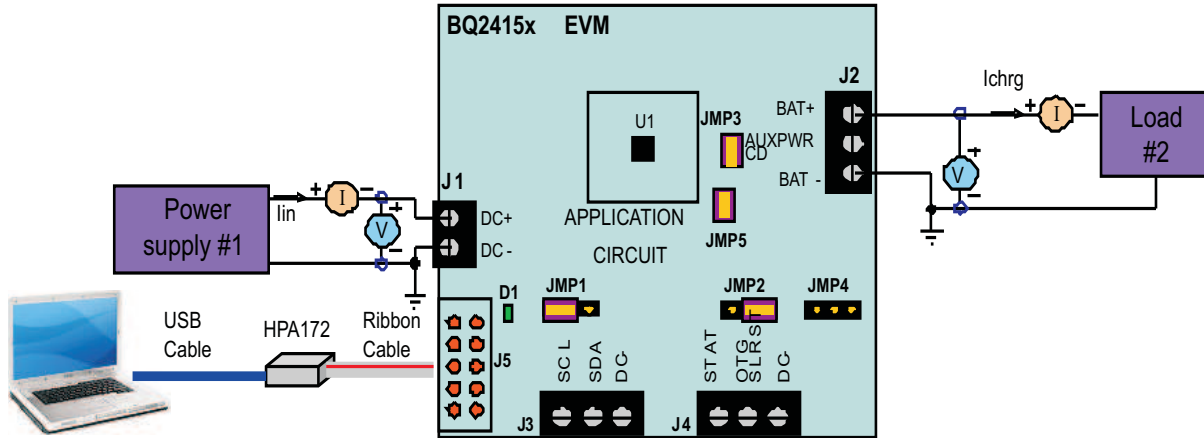

Figure 2. Charging Function Test Setup

9. Turn on the computer.

  •   Open the bq24153A_9 evaluation software. Select part number and click the GO button. The main window of the software is shown in Figure 3.
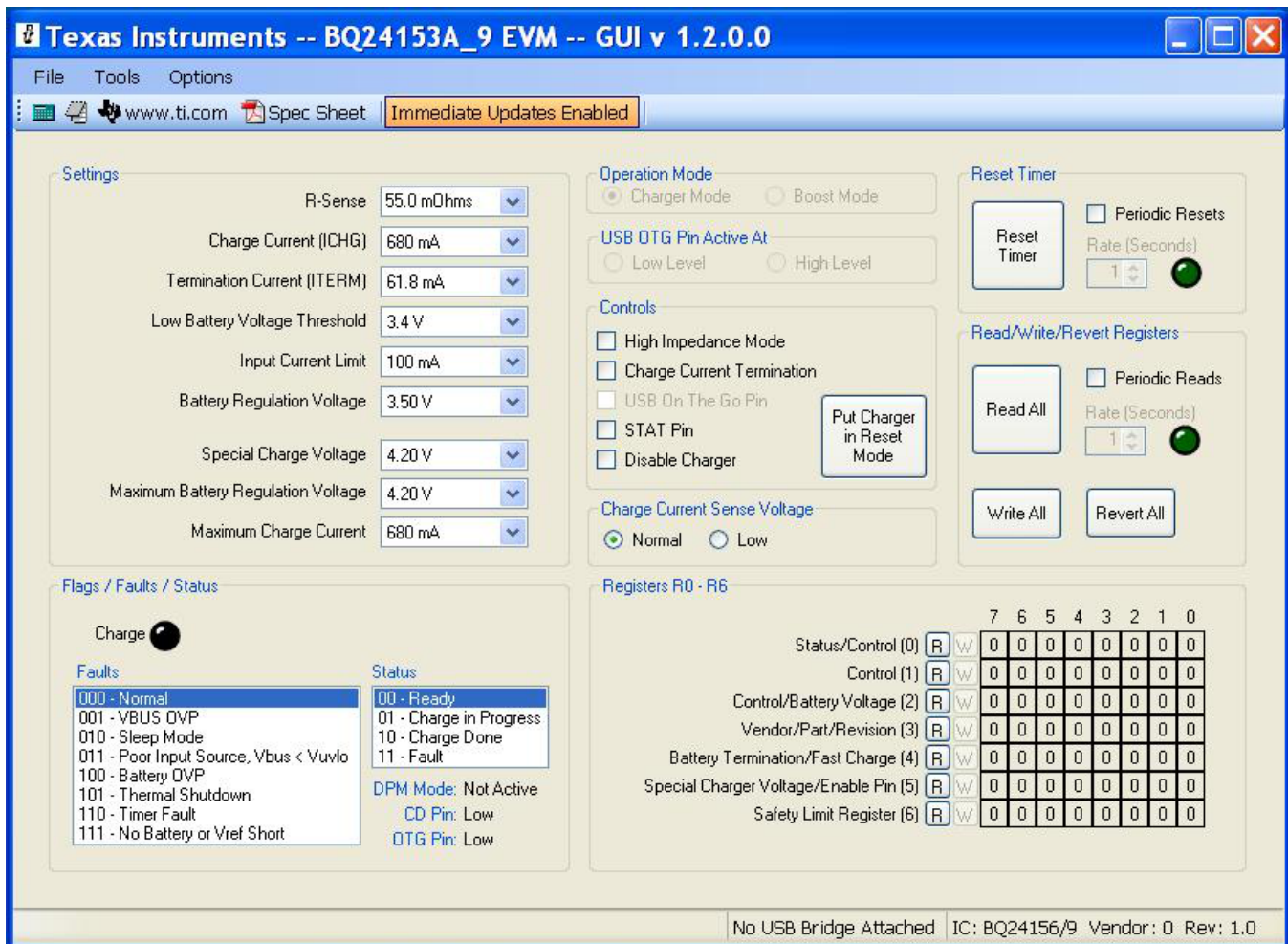
Figure 3. Main Window of bq24153A_9 Evaluation Software

2.4 Recommended Test Procedure

The following test procedure may be useful for evaluating the charger IC outside of a real system especially when no battery is available to connect to the output (i.e., Load#2).

2.4.1 Maximum Charge Current and Maximum Battery Regulation Voltage in The Safety Limit Register

The Maximum Charge Current and Maximum Battery Regulation Voltage values are stored in the Safety Limit Register. If the default values (950mA maximum charge current and 4.20V maximum charge voltage) are acceptable for your application, this step is unnecessary. If not, the Safety Limit Register bits are reset to default values and can be changed immediately after V(CSOUT) (i.e. V(BAT+)) transitions from below V_{SHORT} (2.05V typ) to above V_{SHORT} if the SLRST pin (bq24156A and bq24159 only) is logic high. In addition, on the bq24156A and bq24159, the Safety Limit Register bits are reset to default values and can be changed immediately after the SLRST pin transitions from logic low to logic high if V(CSOUT) is above V_{SHORT} (2.05V typ). Once a change (WRITE command) to any other register is made, the safety limit registers are locked until one of the previously explained transitions occur. The following steps are recommended to modify any of the Safety Limit Register bits.

1. Ensure that Section 2.3 steps are followed.
2. Turn on PS#1. Turn on Load#2 but set its constant voltage to below 2.05V. For the bq24156A and bq24159EVMs only, move the SLRST jumper shunt to LO.
3. With the software running, disable (uncheck) the Periodic Resets and Periodic Reads feature and also

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disable the Immediate Updates button in the toolbar.

4. Increase Load#2 constant voltage to 2.5V. For the bq24156A and bq24159EVMs only, move the SLRST jumper shunt to HI.

5. Use the drop down boxes to select the desired maximum charge current and/or the maximum battery regulation voltage. The Safety Limit Register in the register bank on the bottom right of the screen will change color indicating an update is pending.

6. Press the now-highlighted W button next to the register.

7. Re-enable the Periodic Resets, Immediate Updates and Periodic Reads features as previously recommended.

The Maximum Charge Current and Maximum Battery Regulation Voltages drop down boxes now display the updated values and the charger is ready for further evaluation.

2.4.2   Charge Voltage and Current Regulation

1. Ensure that the Section 2.3 steps are followed.

2. Turn on Load#2.

3. Turn on PS#1.

4. Software setup:

    - Ensure that Immediate Updates is enabled.
    - Check Periodic Resets, and set Rate to 1 second (except for bq24157).
    - Check Periodic Reads, and set Rate to 5 seconds.
    - Ensure that Rsense is set to 68 mΩ.
    - Ensure that Operation Mode is Charger Mode (except for bq24156A and bq24159).
    - Uncheck Charge Current Termination if checked.
    - Check STAT Pin.
    - Select Charge Current Sense Voltage to Normal.

5. Change Charge Current to 950mA and change Input Current Limit to 500mA.

    Measure → Ichrg = 650 mA - 850mA

    Measure → Iin = 440mA - 500mA

    Observe → Diode D1 is on (green)

6. Check Disable Charger. Turn off PS#1, turn off Load #2, and disconnect.

2.4.3   Boost Function for bq24153A, bq24157 and bq24158 Versions Only

1. Adjust PS#1 output to 3.7 V, and disable the output. Connect the PS#1 in series with a current meter (multimeter) to J2 (BAT+, BAT−). Ensure that a voltage meter is connected across J2 (BAT+, BAT−).

2. Set the Load #1 current to 200 mA ±20 mA, but disable the output. Connect the output of the Load #1 in series with a current meter (multimeter) to J1 (DC+, DC−). Ensure that a voltage meter is connected across J1 (DC+, DC−). The setup is now like Figure 4 for HPA256.

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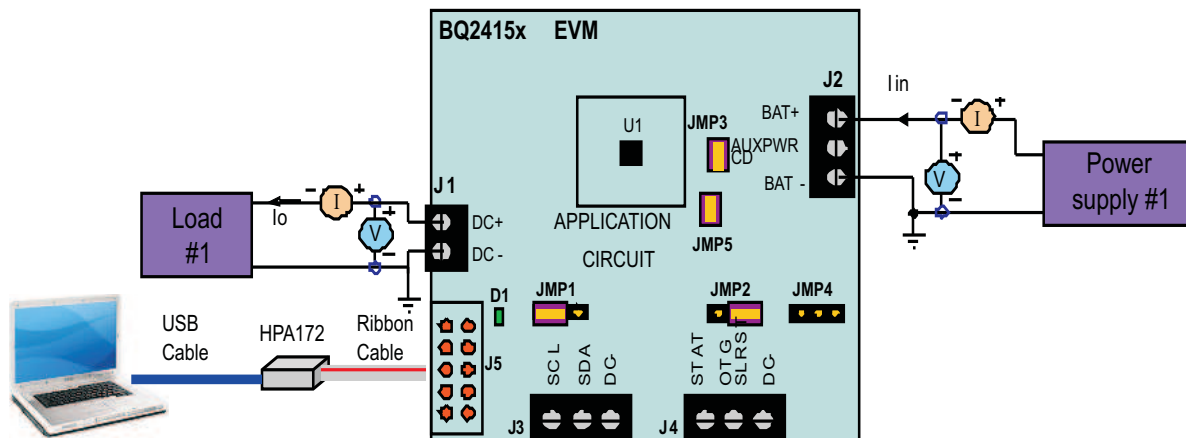
Figure 4. Boost Function Test Setup

3. Turn on PS#1 output.
4. Software setup: Change Operation Mode to Boost Mode.
    Measure → V(J1(DC+, DC–)) = 5 V ±0.2 V
5. Enable Load #1.
    Measure → V(J1(DC+, DC–)) = 5 V ±0.2 V
    Measure → Iin = 330 mA ±40 mA
    Measure → Io = 200 mA ±20 mA

3   Printed-Circuit Board Layout Guideline

1. To obtain optimal performance, the power input capacitors, connected from input to PGND, must be placed as close as possible to the integrated circuit (IC).
2. The output inductor must be placed close to the IC and the output capacitor connected between the inductor and PGND of the IC. The intent is to minimize the current path loop area from the SW pin through the LC filter and back to the PGND pin. To prevent high-frequency oscillation problems, proper layout to minimize high-frequency current path loop is critical.
3. The sense resistor must be adjacent to the junction of the inductor and output capacitor. Route the sense leads connected across the RSNS back to the IC, close to each other (minimize loop area) or on top of each other on adjacent layers (do not route the sense leads through a high-current path).
4. Place all decoupling capacitors close to their respective IC pin and as close as to PGND (do not place components such that routing interrupts power stage currents). All small control signals must be routed away from the high current paths.
5. The PCB must have a ground plane (return) connected directly to the return of all components through vias (two vias per capacitor for power-stage capacitors, two vias for the IC PGND, one via per capacitor for small-signal components). A star ground design approach is typically used to keep circuit block currents isolated (high-power/low-power small-signal) which reduces noise-coupling and ground-bounce issues. A single ground plane for this design gives good results. No ground-bounce issue occurs with this small layout and a single ground plane. Having the components segregated minimizes coupling between signals.
6. The high-current charge paths into VBUS, PMID, and from the SW pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces. The PGND pins must be connected to the ground plane to return current through the internal low-side FET.

4 Bill of Materials, Board Layout, and Schematics

4.1 Bill of Materials

Count					RefDes	Value	Description	Size	Part Number	MFR
53A	56A	58	57	59						
1	1	1	1	1	C1	1 µF	Capacitor, Ceramic, X5R, 16V, ±10%	0603	GRM188R61C105K	Murata
1	1	1	1	1	C2	4.7 µF	Capacitor, Ceramic, X7R, 16V, ±10%	0805	GRM21BR71C475K	Murata
1	1	1	1	1	C3	10 µF	Capacitor, Ceramic, X5R, 10V, ±10%	0805	Std	Std
2	2	2	2	2	C4, C5	1 µF	Capacitor, Ceramic, X5R, 10V, ±10%	0402	GRM155R61A105K	Murata
1	1	1	1	1	C6[1]	0.033 µF	Capacitor, Ceramic, X5R, 16V, ±10%	0402	GRM155R61C333KA01D	Murata
2	2	2	2	2	C7, C8	0.1 µF	Capacitor, Ceramic, X7R, 16V, ±10%	0402	GRM155R71C104K	Murata
1	1	1	1	1	C9	47 µF	Capacitor, Ceramic, X5R, 10V,±10%	1210	GRM32ER61A476KE20L	Murata
1	1	1	1	1	D1	Green	Diode, LED, Green, 2.1-V, 20-mA, 6-mcd	0603	LTST-C190GKT	Lite On
1	1	1	1	1	D2	BAT54C	Diode, Dual Schottky, 200-mA, 30-V	SOT23	BAT54C	Vishay-Liteon
1	1	1	1	1	J1	ED555/2DS	Terminal Block, 2-pin, 6-A, 3.5mm	0.27 x 0.25 inch	ED555/2DS	OST
3	3	3	3	3	J2, J3, J4	ED555/3DS	Terminal Block, 3-pin, 6-A, 3.5mm	0.41 x 0.25 inch	ED555/3DS	OST
1	1	1	1	1	J5	N2510-6002-RB	Connector, Male Straight 2x5 pin, 100mil spacing, 4 Wall	0.338 x 0.788 inch	N2510-6002-RB	3M
3	3	3	3	3	JP1, JP2, JP4	PEC03SAAN	Header, Male 3-pin, 100mil spacing,	0.100 inch x 3	PEC03SAAN	Sullins
2	2	2	2	2	JP3, JP5	PEC02SAAN	Header, Male 2-pin, 100mil spacing,	0.100 inch x 2	PEC02SAAN	Sullins
0	1	0	0	1	L1	1 µH	2.5mmx2mm, 1.0uH, ±30%, 1.6A	0.11x0.09 inch	LQM2HPN1R0MJ0 or CP1008	Murata or Inter-Technical
1	0	1	1	0	L1	1 µH	2.5mmx2mm, 1.0uH, ±30%, 1.3A	0.11x0.09 inch	LQM2HPN1R0MJ0 or MDT2520-CN1R0M or CP1008	Murata or TOKO or Inter-Technical
1	1	1	1	1	R1	0.068	Resistor, Chip, 125mW, 5%	0402	ERJ-2BWJR068X	Panasonic
1	1	1	1	1	R2	5.1k	Resistor, Chip, 1/16-W, 5%	0603	Std	Std
1	1	1	1	1	R3	10k	Resistor, Chip, 1/16-W, 5%	0603	Std	Std
2	2	2	2	2	R4, R5	200	Resistor, Chip, 1/16-W, 5%	0603	Std	Std
0	0	0	0	0	TP1–TP7	Open	Test Point, 0.020 Hole"			
1	0	0	0	0	U1	BQ24153AYFF	IC, Battery Charger for Single-Cell Li-Ion and Li-Polymer Battery	WCSP	BQ24153AYFF	TI
0	1	0	0	0	U1	BQ24156AYFF	IC, Battery Charger for Single-Cell Li-Ion and Li-Polymer Battery	WCSP	BQ24156AYFF	TI
0	0	1	0	0	U1	BQ24158YFF	IC, Battery Charger for Single-Cell Li-Ion and Li-Polymer Battery	WCSP	BQ24158YFF	TI
0	0	0	1	0	U1	BQ24157YFF	IC, Battery Charger for Single-Cell Li-Ion and Li-Polymer Battery	WCSP	BQ24157YFF	TI
0	0	0	0	1	U1	BQ24159YFF	IC, Battery Charger for Single-Cell Li-Ion and Li-Polymer Battery	WCSP	BQ24159YFF	TI
4	4	4	4	4		929950-00	Shorting jumper, 2-pin, 100mil spacing		929950-00	3M/ESD
1	1	1	1	1	–		PCB, 2.0 In x 2.0 In x 0.031 In		HPA697	Any

[1] PCBs prior to revision C have a 0.01 µF capacitor installed

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TABLE 1	
ASSEMBLY NO.	**TEXT**
HPA697-001	BQ24153AEVM-697
HPA697-002	BQ24156AEVM-697
HPA697-003	BQ24158EVM-697
HPA697-004	BQ24157EVM-697
HPA697-005	BQ24159EVM-697

4.2   Board Layout

Figure 5. Top Layer

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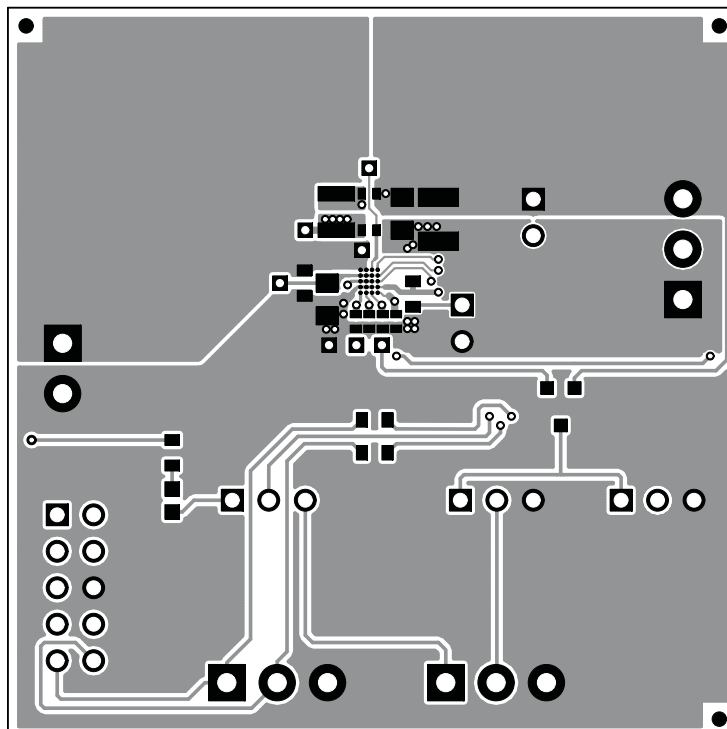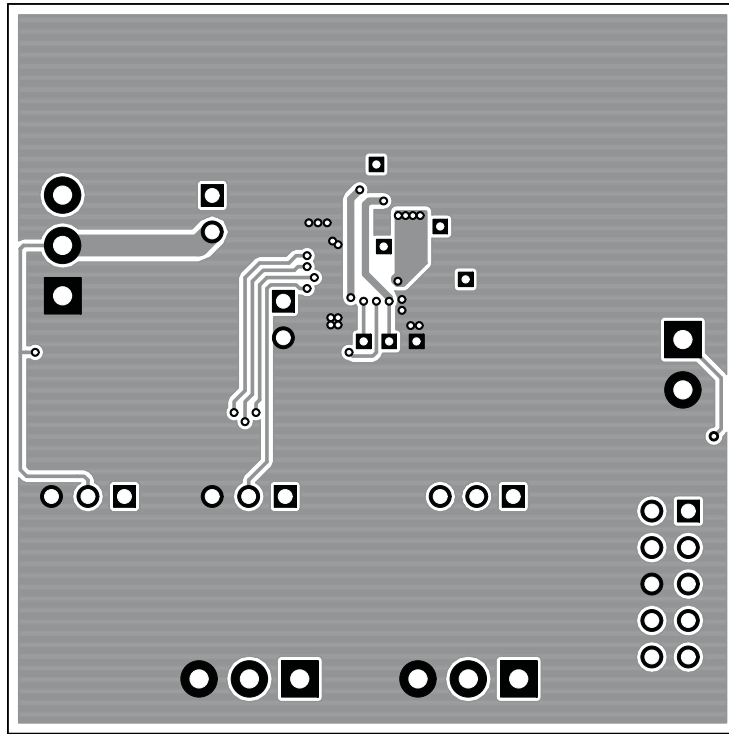
Figure 6. Bottom Layer

Figure 7. Top Assembly

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4.3 Schematic

EVM	IC	U1 Pin D4	JP1	JP2	JP3	JP4	JP5
HPA697-001	bq24153A	OTG					
HPA697-002	bq24156A	SLRST					
HPA697-003	bq24158	OTG					
HPA697-004	bq24157B	OTG					
HPA697-005	bq24159	SLRST					

△1 See table below for IC part number and jumper configuration.

△2 R4 and R5 are used for long communication cable.

Revision History

Changes from B Revision (September 2012) to C Revision   **Page**

- Changed C6 in the Bill of Materials, added table note 1. 9
- Changed C6 in schematic 12

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision History

Changes from A Revision (February 2012) to B Revision   **Page**

- Removed device number bq24157B.. 1
- Added SLUSA27 and SLUS931 technical references.. 2
- Changed From: J2–BAT+ 2
- Changed From: J2–CSOUT 2
- Changed From: J4–OTG 2
- Replaced table.. 2
- Added SOFTWARE section... 4
- Added Factory Jumper Settings... 4
- Changed Original Test Setup for HPA256 (bq2415x EVM) 5
- Updated lit item 9... 5
- Added New figure 6
- 7
- Changed title.. 7
- Removed bq24157B from the schematic 12

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision History

Changes from Original (November 2010) to A Revision   **Page**

- Changed the Maximum Charge Current and Maximum Battery Regulation Voltage in The Safety Limit Register section . 6
- Changed the schematic... 12

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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Certain Instructions. User shall operate EVMs within TI's recommended specifications and environmental considerations per the user's guide, accompanying documentation, and any other applicable requirements. Exceeding the specified ratings (including but not limited to input and output voltage, current, power, and environmental ranges) for EVMs may cause property damage, personal injury or death. If there are questions concerning these ratings, user should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the applicable EVM user's guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, some circuit components may have case temperatures greater than 60°C as long as the input and output are maintained at a normal ambient operating temperature. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors which can be identified using EVMs' schematics located in the applicable EVM user's guide. When placing measurement probes near EVMs during normal operation, please be aware that EVMs may become very warm. As with all electronic evaluation tools, only qualified personnel knowledgeable in electronic measurement and diagnostics normally found in development environments should use EVMs.

Agreement to Defend, Indemnify and Hold Harmless. User agrees to defend, indemnify, and hold TI, its directors, officers, employees, agents, representatives, affiliates, licensors and their representatives harmless from and against any and all claims, damages, losses, expenses, costs and liabilities (collectively, "Claims") arising out of, or in connection with, any handling and/or use of EVMs. User's indemnity shall apply whether Claims arise under law of tort or contract or any other legal theory, and even if EVMs fail to perform as described or expected.

Safety-Critical or Life-Critical Applications. If user intends to use EVMs in evaluations of safety critical applications (such as life support), and a failure of a TI product considered for purchase by user for use in user's product would reasonably be expected to cause severe personal injury or death such as devices which are classified as FDA Class III or similar classification, then user must specifically notify TI of such intent and enter into a separate Assurance and Indemnity Agreement.

RADIO FREQUENCY REGULATORY COMPLIANCE INFORMATION FOR EVALUATION MODULES

Texas Instruments Incorporated (TI) evaluation boards, kits, and/or modules (EVMs) and/or accompanying hardware that is marketed, sold, or loaned to users may or may not be subject to radio frequency regulations in specific countries.

General Statement for EVMs Not Including a Radio

For EVMs not including a radio and not subject to the U.S. Federal Communications Commission (FCC) or Industry Canada (IC) regulations, TI intends EVMs to be used only for engineering development, demonstration, or evaluation purposes. EVMs are not finished products typically fit for general consumer use. EVMs may nonetheless generate, use, or radiate radio frequency energy, but have not been tested for compliance with the limits of computing devices pursuant to part 15 of FCC or the ICES-003 rules. Operation of such EVMs may cause interference with radio communications, in which case the user at his own expense will be required to take whatever measures may be required to correct this interference.

General Statement for EVMs including a radio

User Power/Frequency Use Obligations: For EVMs including a radio, the radio included in such EVMs is intended for development and/or professional use only in legally allocated frequency and power limits. Any use of radio frequencies and/or power availability in such EVMs and their development application(s) must comply with local laws governing radio spectrum allocation and power limits for such EVMs. It is the user's sole responsibility to only operate this radio in legally acceptable frequency space and within legally mandated power limitations. Any exceptions to this are strictly prohibited and unauthorized by TI unless user has obtained appropriate experimental and/or development licenses from local regulatory authorities, which is the sole responsibility of the user, including its acceptable authorization.

U.S. Federal Communications Commission Compliance

For EVMs Annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant

Caution

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation. Changes or modifications could void the user's authority to operate the equipment.

FCC Interference Statement for Class A EVM devices

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at its own expense.

FCC Interference Statement for Class B EVM devices

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

Industry Canada Compliance (English)

For EVMs Annotated as IC – INDUSTRY CANADA Compliant:

This Class A or B digital apparatus complies with Canadian ICES-003.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Concerning EVMs Including Radio Transmitters

This device complies with Industry Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concerning EVMs Including Detachable Antennas

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication.

This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Canada Industry Canada Compliance (French)

Cet appareil numérique de la classe A ou B est conforme à la norme NMB-003 du Canada

Les changements ou les modifications pas expressément approuvés par la partie responsable de la conformité ont pu vider l'autorité de l'utilisateur pour actionner l'équipement.

Concernant les EVMs avec appareils radio

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante.

Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur.

Important Notice for Users of EVMs Considered "Radio Frequency Products" in Japan

EVMs entering Japan are NOT certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If user uses EVMs in Japan, user is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after user obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after user obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless user gives the same notice above to the transferee. Please note that if user does not follow the instructions above, user will be subject to penalties of Radio Law of Japan.

http://www.tij.co.jp

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日本テキサス・インスツルメンツ株式会社
東京都新宿区西新宿６丁目２４番１号
西新宿三井ビル
http://www.tij.co.jp

IMPORTANT NOTICE

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