Reducing crosstalk of an op amp on a PCB

By Randy Stephens

System Specialist, High-speed Amplifiers

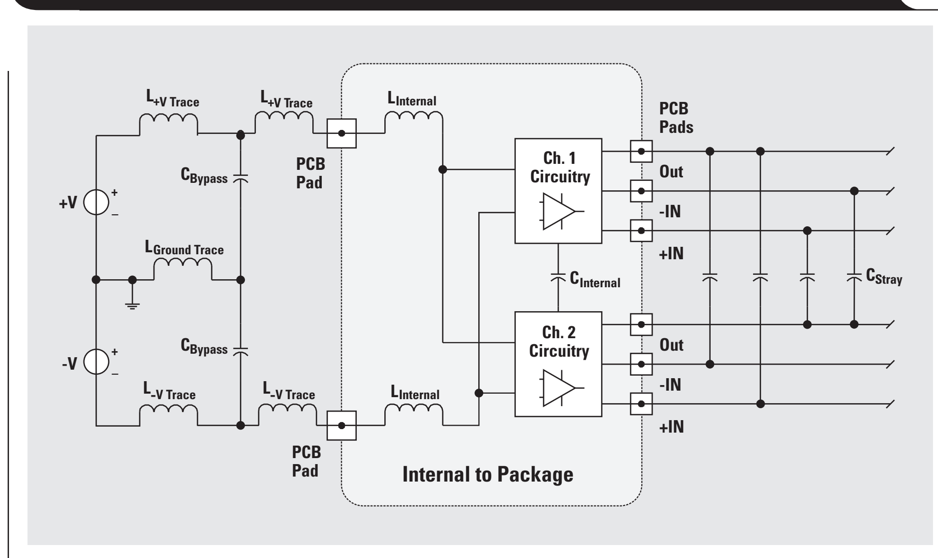
The use of operational amplifiers is common these days. In many instances, it can be advantageous to utilize a dual or quad op amp to save circuit board space and costs, but one of the drawbacks is that the signal from one amplifier may "talk" into the other amplifiers within the single package. This is commonly referred to as crosstalk. To measure crosstalk, a signal is applied to only one amplifier within the package while the outputs of all the remaining amplifiers are probed to determine how much of the source signal is feeding through (or crosstalking). There are several notes and papers on how to minimize crosstalk, but these typically deal only with the silicon and/or packaging. This is not much help to the user of a multi-channel op amp who has no control over what is going on inside the packaged part. The only thing the user can control is the external circuitry and the printed circuit board (PCB) layout. Numerous elements contribute to crosstalk, but the main contributors are shown in Figure 1. Design decisions are based on the measured results, and conclusions are drawn to provide real-world solutions to minimize crosstalk in the TI THS4052 dual-channel high-speed amplifier.

The internals of a dual-channel amplifier

It is helpful to understand what the user does and does not have control over with a dual-channel amplifier. When buying a packaged part, the user has no control over what is inside the package. This includes the lead frame, the silicon die, bond wires, etc. Figure 1 shows the important internal structures that lead to crosstalk within a dual-channel amplifier. Both internal inductors ($L_{Internal}$) on each power-supply line are comprised of the lead-frame pins on the package, the internal bond wires that interconnect the lead frame and the silicon die, and the metal traces within the silicon die itself. Inductors form a low pass filter element that has an impedance directly proportional to frequency ($Z_L = 2\pi fL$). Assume that Channel 1 of this amplifier is producing a signal with a current draw from the power supplies +V and –V. Because both internal inductors represent a high impedance at high frequencies (>1 MHz), the circuitry within Channel 2 most certainly will be affected by the demands of Channel 1. This includes fluctuations of the supply voltages and capacitive coupling into Channel 2's circuitry via the power-supply bus.

There are several ways to minimize these effects, including separate power supplies for each channel, minimizing the bond wire lengths, and using smaller lead frames and packages. Another thing that cannot be controlled by the user is the isolation between the two circuits. Whenever there are two electrical potentials separated by an insulator, a capacitor ($C_{Internal}$) is formed. This stray capacitance allows two signals to couple into each other. The impedance of a capacitor is indirectly proportional to the frequency of the signal ($Z_C = 1/2\pi fC$). Because this capacitance is typically in the low pF range, the coupling will typically start to appear at frequencies greater than 1 MHz. The silicon designer has numerous choices to help minimize this capacitive coupling, including trench isolation, silicon-on-insulator (SOI) topology, physical separation of the circuits, and circuitry geometry. The problem presented to the purchaser of this product is that he has no influence on what the silicon designer has done to minimize crosstalk. Now that we know what we cannot do to minimize crosstalk, let's look at what we can do.

Figure 1. Simplified crosstalk components of a dual op amp on a PCB



Power-supply rules

Figure 1 shows that the inductance of the power supplies could be a big factor associated with crosstalk. To make matters worse, in order to connect the op amp to a power source, traces must be used. These traces can run several inches. Since any piece of electrically conducting wire (like a PCB trace) has an inductance based on the length of the wire (around 15 nH per inch), the previous problem of

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inductance on the power supply only gets worse. In fact, the PCB trace can easily have much more inductance than that of the packaged part itself.

The cure for this inductance problem is easy to implement by using bypass capacitors. These capacitors should be located physically as close as possible to the op amp power-supply pins. When it comes to dealing with high-frequency amplifiers that have bandwidths exceeding 50 MHz, the distance between the pin and the bypass capacitor can be extremely critical. These bypass capacitors should have very good high-frequency characteristics, which usually precludes the use of large electrolytic or tantalum capacitors. Large "bulk" capacitors play an important role in supplying lower-frequency currents, but they do not perform very well with frequencies above 1 MHz.

The most common type of capacitor used for high-frequency bypass is the ceramic capacitor. Using surface-mount technology (SMT) components over leaded parts is also recommended. This will virtually eliminate the lead inductance of the capacitor, making the capacitor behave more like the "ideal" capacitor. To see the benefits, the ground side of the bypass capacitors should always be connected to the ground plane with vias or as short a trace as possible. The trace is an inductor at high frequencies, counteracting the good bypassing effects of the capacitor. There are numerous other ideas to improve power-supply decoupling, but they tend to cost more and consume precious board space.[1] For most circuits, though, the use of a simple 0.1-µF or 0.01-µF ceramic capacitor in parallel with a large tantalum or electrolytic capacitor will provide sufficient power-supply decoupling.

A few tests will illustrate the effects of power-supply decoupling. These tests were done using a THS4052 high-speed amplifier packaged in an MSOP PowerPAD™ package. Because this amplifier has a bandwidth of 70 MHz, the crosstalk frequency range was limited to 100 MHz. Refer to Figure 2 for the test set-up and amplifier configurations and to Figure 3 for the results.

As Figure 3 shows, removing the 0.1-µF capacitors made the crosstalk worse by almost 10 dB at 10 MHz and by over 20 dB at 100 MHz. For experimentation purposes, the 22-µF tantalum bypass capacitors were also removed to see the effects on crosstalk. As expected, the crosstalk became much worse across the entire frequency range.

Looking at Figure 1, we see that the supply voltages (+V and –V) should not cause any changes in crosstalk performance. To verify if this was true, the results for all the tests conducted throughout this application note were taken with ±15-V and ±5-V supplies. As expected, the crosstalk performances with different supply voltages were practically indistinguishable from each other. The power supplies do not play any significant role with respect to crosstalk issues and will be ignored for the remainder of this discussion.

Figure 2. Default test circuit set-up configuration

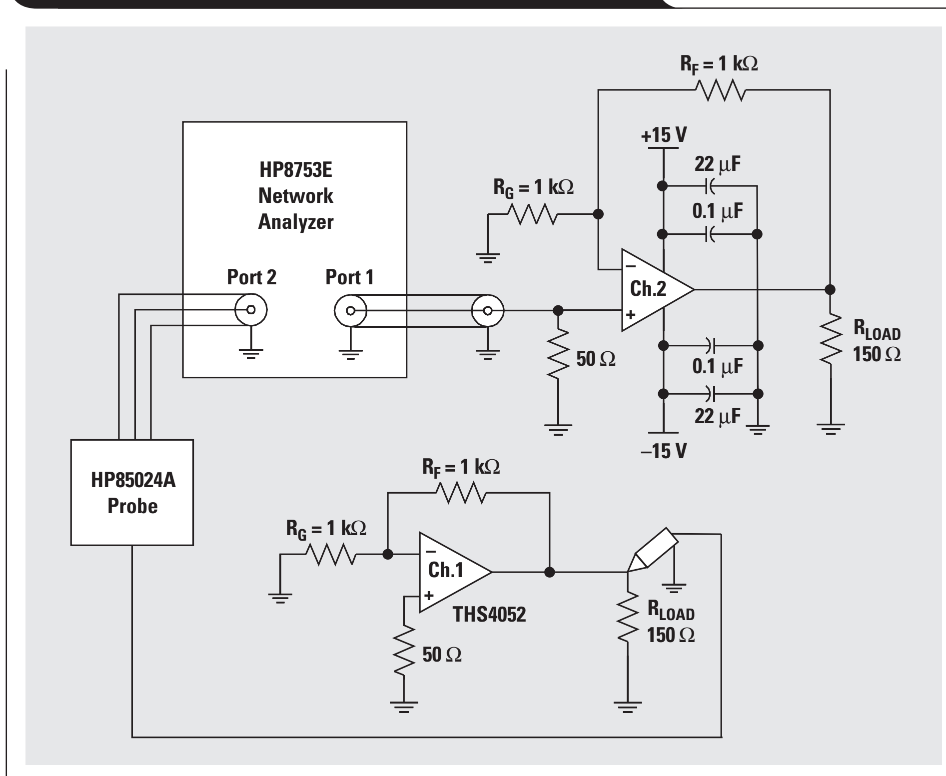
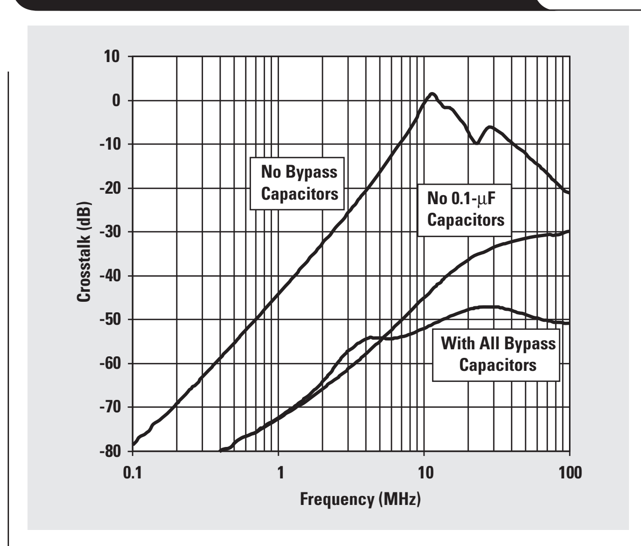


Figure 3. Power-supply decoupling crosstalk results



One question arises from this figure. Why does the crosstalk start dropping again at high frequencies when there are no bypass capacitors? There are two answers. The first is that since the amplifiers were connected with a gain of +2, the bandwidth of this voltage feedback amplifier will be around only 35 MHz (following the traditional gain-bandwidth product). Above this frequency, the amplitude of both amplifiers starts to drop off and the current demand on the power supply is also reduced, minimizing the effects of the trace inductances.

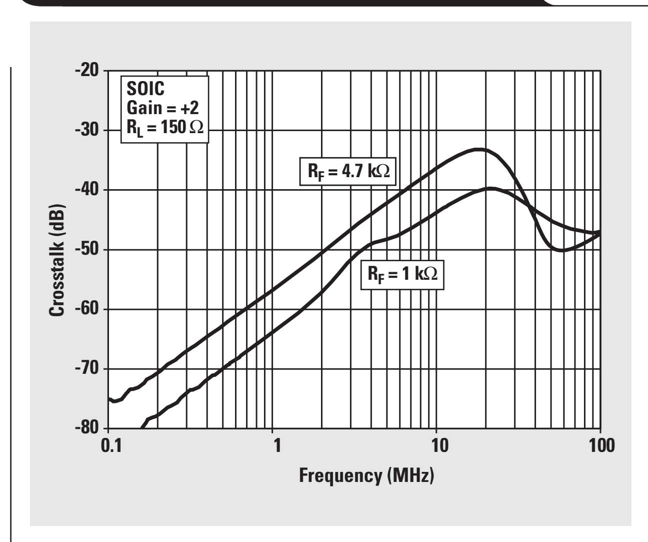
The second answer is that the utilization of a ground plane on the PCB helps minimize the lead inductance problem. As the power-supply trace runs on top of the ground plane, some distributed capacitance is formed. This capacitance performs exactly the same job as the small ceramic capacitors originally performed—not quite to the extent of the real 0.1-µF capacitor, because the equivalent capacitance value is much less.

Taking this idea the next step, a power plane for each supply voltage and at least one ground plane can significantly increase the high-frequency power-supply bypassing effects. The first thing this does is to minimize the trace inductance of the power supplies. The greater the surface area, the lower the inductance. The second benefit provided by power planes is a very large, uniformly distributed power-supply bypass capacitor. This capacitance can be extremely helpful when dealing with frequencies greater than 100 MHz. Not all PCB designs lend themselves to utilizing multi-layer PCBs, though. At the very least, a ground plane should be utilized on at least one side of a PCB to eliminate the $L_{Ground\ Trace}$ inductance. This can be easily accomplished by filling the unused portions of the PCB with a ground plane. Just make sure that there are no isolated “islands” on the board. They should be connected to the ground plane by PCB vias, or simply eliminated.

Amplifier resistor selection

No matter how an amplifier is used, resistors are used to give an amplifier a specific response. Sometimes designers have no choice in the resistances used to close the amplifier loop. But, if any resistor value can be chosen, there are some choices to make related to crosstalk performance.

Figure 4. Effects of feedback and gain resistors on crosstalk—SOIC



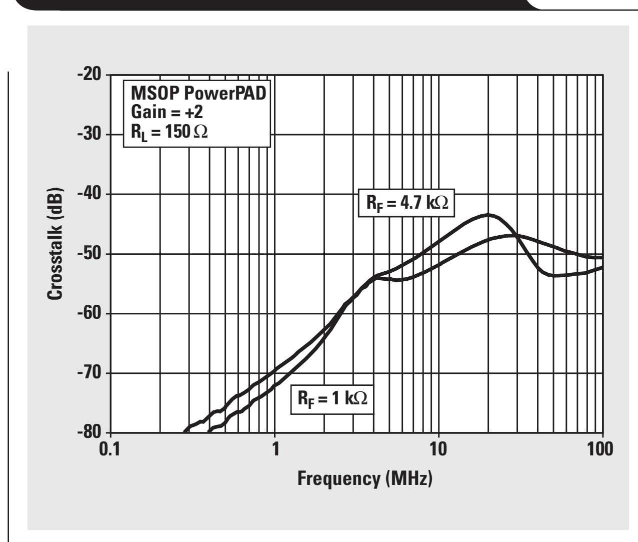
As shown in Figure 1, the output pins and input pins can couple into each other by stray capacitances. Notice that crosstalk directly into the output trace is usually not a problem. This is because the closed loop impedance of an amplifier is very small, allowing the amplifier to overcome just about any form of crosstalk coupling.

The same does not hold true when it comes to the inverting and non-inverting input pins of the amplifier. This is because the input impedance of these pins is generally very high. In the case of FET amplifiers, it can approach 10^{12} ohms. This is very important because the amount of stray capacitance required to inject a signal is tied indirectly to the impedance of a circuit node. When the impedance of a capacitor (Z_C) is equal to the nodal resistance, the amount of signal injection has reached the half-power point (–3 dB). If the frequency increases or if the capacitance is increased, it is obvious that the amount of signal injection will also increase. But if the nodal resistance can be lowered, the effects of the stray capacitance can be reduced.

This idea is the basis for the next design rule to help reduce crosstalk. Simply use smaller resistances for both the inverting and non-inverting nodes of an amplifier. For the inverting node, which must have a feedback resistor (R_F) and usually a gain resistor (R_G), the ac nodal resistance is equivalent to the parallel resistance of both of these resistors. Figures 4 and 5 illustrate this point for the THS4052 in both the standard SOIC package and the MSOP PowerPAD package. The test circuit shown in Figure 2 was also used for this test, with the resistor values as shown in the figures.

The amplifiers were placed into a gain of +2 by making the feedback (R_F) and gain (R_G) resistor values equal to each other. It can be seen that as the ac resistance value

Figure 5. Effects of feedback and gain resistors on crosstalk—MSOP



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at the inverting node decreased, the crosstalk also decreased, especially for the SOIC package. However, there may be some drawbacks to reducing the resistor values. In the case of high-speed amplifiers, the feedback resistor can play a very important role in determining the frequency response of the amplifier. Another thing that is typically overlooked is that the feedback resistor is also part of the load to the amplifier. What happens as the load is increased on the amplifier?

Amplifier loading effects

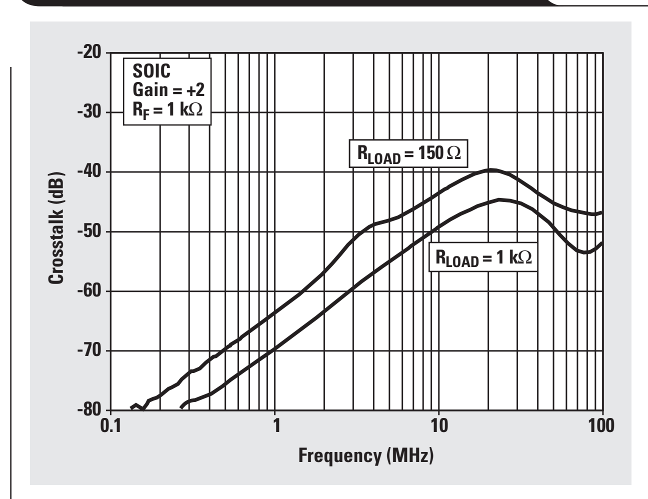
Recall from the first section that trace inductances, both internal and external, may play a key role in crosstalk. This happens when the current flowing through these inductances starts increasing. The main reason for an increase in current being drawn from the power supplies is that the amplifier is driving a low-impedance load. This load may be reactive and/or resistive, but only resistive loading is considered for comparison. Figures 6 and 7 show the effects of loading on the amplifiers. As the load resistance increases, the crosstalk decreases. At some point, increasing the load resistance may not decrease the crosstalk very much. This is due to the feedback resistor (R_F) becoming the dominant load to the amplifier. In general, the higher the load resistance on the amplifier, the lower the crosstalk will become.

Amplifier configuration considerations

Up to this point all of the results have been shown with the amplifiers in a non-inverting configuration with a gain of +2. This is done to maintain a constant point of reference while changing specific circuit parameters. The next step in the process is trying different amplifier configurations.

The first thing to try is changing the non-inverting gain from +2 to different values. This usually brings up some good questions about what will happen. Lower gains mean that the ac resistance at the inverting node will tend to be higher than with higher gains. But the amplifier

Figure 6. Effects of load resistance on crosstalk—SOIC



will be amplifying the crosstalk signal by only a small gain instead of a larger gain. The next configuration is an inverting configuration. This places the inverting node at a virtual ground, but to the amplifier, a gain of –1 is equivalent to a noise gain of +2. So the only thing that really changes is the source amplifier's input. The measured amplifier is held in the exact same configuration as a gain of +2.

Figures 8 and 9 show the results of different gains and configurations. For all gains shown, the feedback resistance (R_F) was held at 1 kΩ, and the gain resistor (R_G) was adjusted accordingly. Both amplifiers were also configured the same way such that if Channel 2 was set in a gain of +5, Channel 1 was also set in a gain of +5.

The results speak for themselves. It appears that as the gain increases, the crosstalk becomes much worse. It also appears that the inverting gain configuration is the best of

Figure 7. Effects of load resistance on crosstalk—MSOP

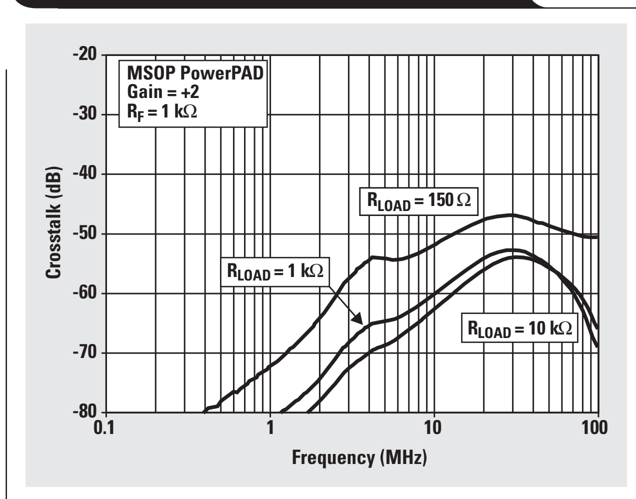
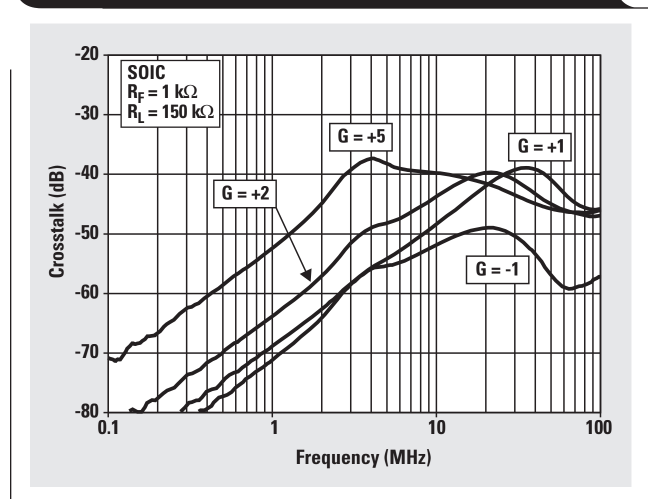


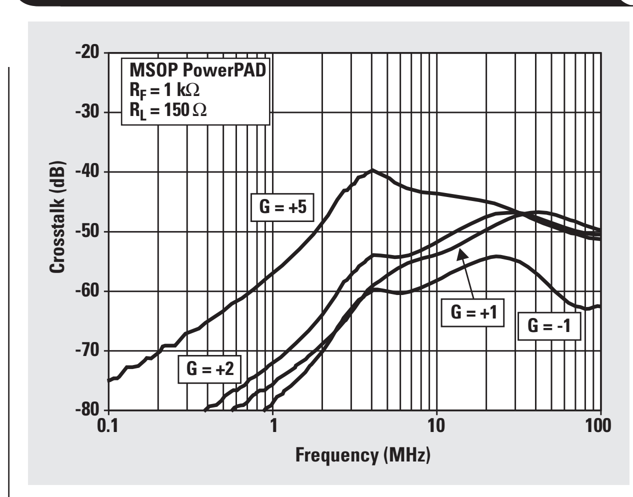
Figure 8. Effects of gain and configuration on crosstalk—SOIC



the test set, surpassing the gain of +2 by a fairly respectable margin. By the non-inverting node being held at ground and the inverting node being held at a virtual ground, the low input impedance appears to have an edge over the non-inverting gain set-up. This configuration also keeps the common-mode input of the amplifier at a fixed reference. Traditionally, this usually keeps the common-mode rejection ratio (CMRR) of the amplifier at its best performance. As long as the stray capacitances and noise levels are held fairly close to each other at both of the input nodes, the CMRR will help keep crosstalk out of the amplifier.

One last configuration to try was the non-inverting buffer configuration with no feedback resistance (R_F = 0 Ω). This will keep the inverting node impedance very small due to the direct connection to the output of the amplifier. Figures 10 and 11 show that this configuration is the absolute best when it comes to dealing with crosstalk issues. The problem with this configuration is that typically the frequency response of a high-speed amplifier will suffer with a 0-Ω feedback resistance. This is especially true for current feedback amplifiers that must have a feedback resistance for stability purposes. The intent of this application note is to show real-world situations, and this unity gain buffer configuration normally will not be used for high-frequency applications. Instead, there typically will be a feedback resistance that may significantly affect crosstalk performance.

Figure 9. Effects of gain and configuration on crosstalk—MSOP



Packaging and layout considerations

The next thing that plays a role in crosstalk is packaging. The choices may include PDIP, SOIC, MSOP, or TSSOP. The packages may give a clue as to which might perform better. Remember that the circuit designer has no control over the internals of the package, so selecting the smallest package possible will probably keep the inductances down to a minimum. In the case of the THS4052, there are two choices—the SOIC and the MSOP PowerPAD package, where the MSOP is substantially the smaller of the two.

In order to see the results of these packages, they must be placed on a circuit board. The PCBs used for all these tests were practically identical. Only the landing area for the chips was changed accordingly. The MSOP package has a PowerPAD on the bottom of the chip to improve heat dissipation of the small package. The advantage of this is that the pad is soldered onto the ground plane between all of the pins. This means that there is a low-impedance area to absorb the signals coming from the source amplifier via the ground plane, before the signal couples into the measured amplifier.

The SOIC-packaged amplifier, on the other hand, does not require a ground plane between the pins. The test PCB has a cutout only to minimize leakages between the pins of the amplifier. This does not represent a low-impedance sink to the crosstalk signals. To see if adding a ground area actually does anything, a piece of copper tape was soldered under the SOIC package and connected

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Figure 10. Crosstalk with unity gain buffer configuration—SOIC

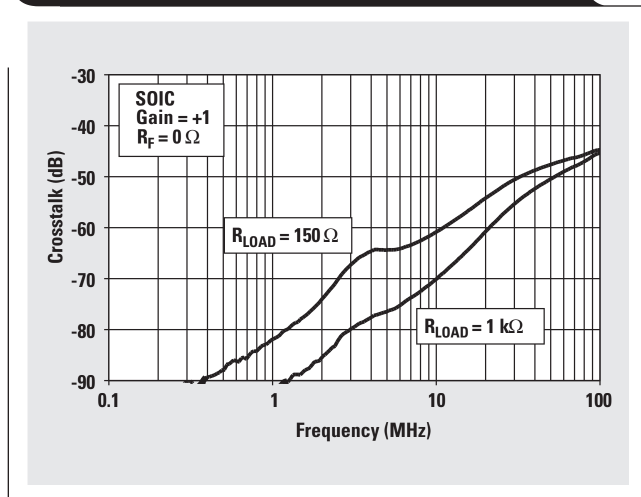
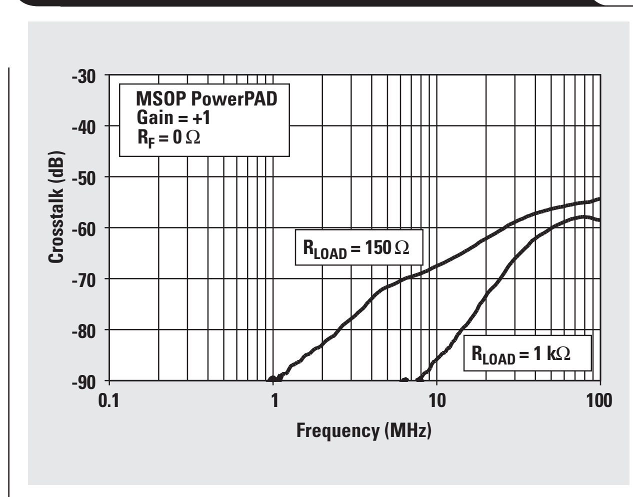


Figure 11. Crosstalk with unity gain buffer configuration—MSOP



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to the ground plane to simulate the MSOP PowerPAD configuration.

Figures 12 and 13 show the results of the different packages. Again, the gain of –1 configuration shows the best real-situation results. The addition of the ground plane under the SOIC package did help with crosstalk by about 5 dB across the entire test frequency range, but it is still not quite as good as the MSOP PowerPAD package.

There are two reasons for this. The first is the physical size of the MSOP PowerPAD package. It is smaller than the SOIC package, reducing inductances. Second, the PowerPAD keeps the substrate of the silicon at a ground reference. Thus the two channels inside the package have a low-impedance noise "sink" and do not allow the substrate to act as a noise-coupling device into the adjacent channel. The SOIC package, on the other hand, does not have this extremely low-impedance system. To keep the substrate at a fixed level, it is fairly common to connect one of the power-supply pins to the substrate. The drawback is that the pin itself has the same lead inductance as shown in Figure 1, reducing the effectiveness of this noise "sink."

It cannot be denied that a ground plane does improve the SOIC crosstalk response. Instead of placing a ground between the pins, it makes sense that power-supply traces between the leads would also serve the same purpose as the ground plane. Just keep in mind that usually the power-supply traces will not have as low an inductance, and hence impedance, as a true ground plane. Another concern is that power-supply noise also may be capacitively coupled into the chip by the traces being directly under the silicon die. A good power-supply plane should remedy all of these possible problems.

General design guidelines and conclusions

The results of this testing have shown several things to look for when crosstalk is an issue. Some things were not tested in detail but generally can be accepted as true based on experience and extrapolation of this data. The keys to attaining a high crosstalk rejection include:

1. Use 0.1-µF or 0.01-µF SMT ceramic bypass capacitors as close as possible to the power-supply pins on each and every amplifier.
2. Use a very large ground plane on the PCB.
3. Use a power-supply plane for each supply voltage if possible.
4. The best crosstalk performance is achieved with a gain of +1 configured with a 0-Ω feedback resistance. But, for most applications, use a gain of –1 if possible.
5. Keep the amplifier gain to a minimum.
6. Keep the feedback (R_F) and gain (R_G) resistances down to a minimum.
7. Use as high a load resistance as your design allows.
8. Pick a small surface-mount (SMT) package.
9. Consider the PowerPAD package with the pad soldered directly to the ground plane.
10. If using a non-PowerPAD package, place a ground pad or low-impedance traces between the pins.
11. Keep non-inverting and inverting pin traces to a minimum. The longer the trace, the more stray capacitance it will have.
12. If design allows, put guard traces around the input pins of the amplifier. This guard trace should be connected to the ground plane for high isolation.
13. Keep the ground return path of the load routed away from the amplifier's input traces.
14. Isolate the traces for each amplifier from the other amplifier(s) as much as possible.

Following these rules should minimize crosstalk issues in PCB design and allow the user of multi-amplifier packages to save PCB space and money.

Figure 12. Effects of packaging and PCB on crosstalk—Gain = +2

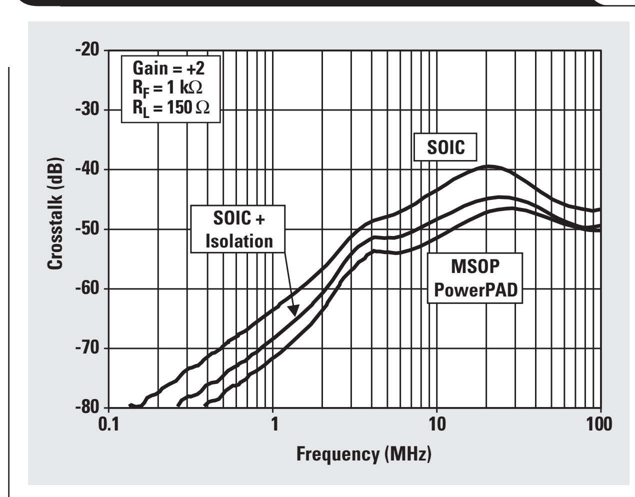
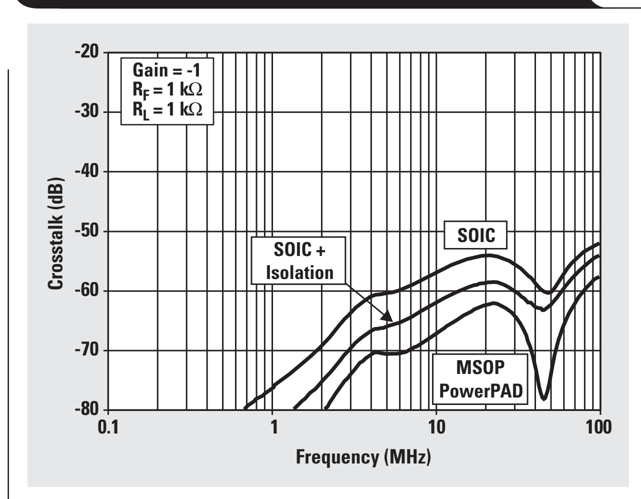


Figure 13. Effects of packaging and PCB on crosstalk—Gain = –1



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