Layout Review Techniques for Low Power RF Designs

By Suyash Jain

Keywords

- *Layout Review Techniques*
- *Board Stacking for RF Design*
- *CC1020, CC1021*
- *CC1100E, CC1101, CC1110, CC1111, CC1150*
- *CC2420, CC2430, CC2431, CC2480*
- *CC2500, CC2520, CC2510, CC2530, CC2533*
- *CC430*
- *CC2540, CC2541, CC2541S, CC2543, CC2544, CC2545*

1 Introduction

At radio frequencies, the wavelength of the RF signal can become comparable to the physical dimensions of the network and transmission lines can be a considerable fraction of the network. Lumped element models in such cases can no longer be applied, and it becomes important to consider the distributed models to account for the magnitude and phase shift of the signal over the length of the transmission lines [1]. If not, reflections occur and can cause significant loss (return loss) in the power transfer between various stages in a design. Impedance matching is critical for maximum power transfer. Additionally, electromagnetic radiation and capacitive coupling among the elements causes unintentional losses that may also significantly alter the performance of the circuit and must be considered while laying out the design. TI LPRF reference designs are designed taking into consideration all these effects for optimum performance and are recommended to be copied exactly/closely for any required application.

The purpose of this application note is to provide guidelines to copy successfully the reference designs for TI CCXXXX LPRF devices. This application note also illustrates important RF PCB design concepts for a successful RF PCB layout. It provides steps to lay out an RF PCB and review the final design before sending it to the manufacturer. These recommendations will assist having a working design on the first prototype. The application note then discusses commonly-made PCB design mistakes that will provide designers a clear understanding of things not to do.

SmartRF™ studio is a powerful tool for prototyping designs; this application note also describes how to include a test/debug port in the prototype design for easy and quick radio performance testing.

Table of Contents

KEYWORDS **1**
1 INTRODUCTION **1**
2 ABBREVIATIONS **2**
3 BASICS OF RF PCB DESIGN **3**
3.1 IMPEDANCE MATCHING 3
3.2 TRANSMISSION LINES 3
3.3 BOARD STACK-UP 4
3.4 POWER SUPPLY BYPASSING AND DECOUPLING 4
3.5 GROUND PLANE 5
3.6 COMPONENT ORIENTATION 6
4 COPYING TI REFERENCE DESIGN **7**
5 DEBUG SOCKET ON THE DESIGN **9**
6 EXAMPLES OF THINGS NOT TO DO **10**
6.1 LONG RF TRACE LENGTHS AND MISMATCHED TRACES IN DIFFERENTIAL RF SECTIONS 10
6.2 DIGITAL LINES NEAR/BELOW THE RF PATH 11
6.3 DIGITAL TRACES BELOW/NEAR THE CRYSTAL OSCILLATOR 11
6.4 BYPASS CAPACITOR PLACEMENT 11
6.5 PCB LAYERS SWAPPED WHILE MANUFACTURING 12
6.6 SILKSCREEN BELOW THE CHIP 13
6.7 POWER PAD LAYOUT 13
7 CONCLUSION **14**
8 REFERENCES **14**
9 GENERAL INFORMATION **14**
9.1 DOCUMENT HISTORY 14

2 Abbreviations

BOM	Bill of Materials
PCB	Printed Circuit Board
PER	Packet Error Rate
RF	Radio Frequency
SRF	Self Resonant Frequency
DD	Debug Data
DC	Debug Clock
NC	Not Connected
LPRF	Low Power RF

3 Basics of RF PCB Design

This section discusses important concepts for a RF PCB design.

3.1 Impedance Matching

The maximum power theorem states that maximum power is transferred when the internal resistance of the source equals the resistance of the load. When extended to alternating current circuits it states that to obtain maximum power transfer the load impedance must be complex conjugate of the source impedance. To maximize power transfer for optimum performance it is important that impedance matching is considered carefully in radio frequency designs. Texas Instruments reference design are optimized by presenting optimum load for maximum power transfer such that maximum (optimum) power transfer occurs in both transmit and receive modes and at different conditions such as at different supply voltages and temperatures. It is recommended that the reference design be copied for optimum performance.

3.2 Transmission Lines

PCB traces at radio frequencies have to be designed carefully, accounting for their distributed character as the physical length of the traces becomes a considerable fraction of the signal wavelength. The impedance of a PCB trace at RF frequencies depends on the thickness of the trace, its height above the ground plane, and the dielectric constant and loss tangent of PCB dielectric material. Assuming that the thickness of the trace, *t*, is small compared to the height *h* above the ground plane (*t*/*h* < 0.005), and that the ratio *w*/*h* <1, the impedance of the trace can be calculated as [1]:

$$Z_0 = \frac{60}{\sqrt{\varepsilon_{eff}}}.\ln\left(\frac{8.h}{w} + \frac{w}{4.h}\right)$$

and,

$$\varepsilon_{eff} = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}\left[\frac{1}{\sqrt{1 + \frac{12.h}{w}}} + 0.04\left(1 - \frac{w}{h}\right)^2\right]$$

Where,

h = height of the trace above the ground plane
w = width of the trace
ε_r = dielectric constant of the PCB board material
ε_{eff} = effective dielectric constant based on the width and height of the PCB trace

In Texas Instruments Low power RF designs it is recommended to carefully design the transmission line between the balun-filter section and the antenna which is of 50ohm characteristic impedance, as the impedance of the trace is critical factor for delivering maximum power out of the balun-filter section to the antenna. Also, the traces in the balun-filter section should be copied from reference design, i.e. trace-width and trace-length along with stacking height between signal plane and ground plane and dielectric properties of the PCB from the reference design.

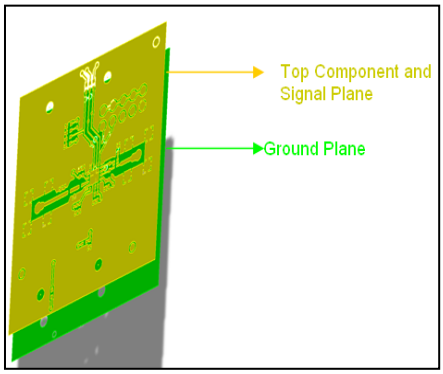
3.3 Board Stack-Up

RF PCB designs are usually designed on 2- or 4-layer boards. Two-layer PCB boards (Figure 1) are designed to have component and signal routing on the top layer, while the bottom layer is designed to be predominantly ground, providing the shortest path for return currents. The ground plane should be continuous; if it is divided, especially under the RF path, it can increase the return current's path length and can significantly affect the desired performance. A 2-layer PCB board design provides cost savings compared to a four layer PCB design and can provide comparable performance to a four layer design, but requires careful signal routing and component placement. These designs are generally limited to thicknesses of 0.8-1.0mm, as using a greater thickness micro-strip line causes the corresponding widths for common impedances (e.g., 50 ohms) to be too large for practical designs.

A 4-layer PCB (Figure 2) design provides easy routing for ground and power planes and relaxes routing considerations compared to a 2-layer PCB. It provides easy decoupling of the power plane placed between the ground plane and bottom layer, which is predominantly ground. In a 4-layer board it is recommended to have the layer structure as defined below.

1st Layer: Component and Signal
2nd Layer: Ground Plane
3rd Layer: Power Plane
4th Layer: Ground Plane and Signal Routing

Note that in any four-layer RF PCB design a ground plane must always be below the top component and signal plane. The increased thickness (~60mils) in 4-layer PCBs also provides mechanical strength to the PCB as compared to a 2-layer design.



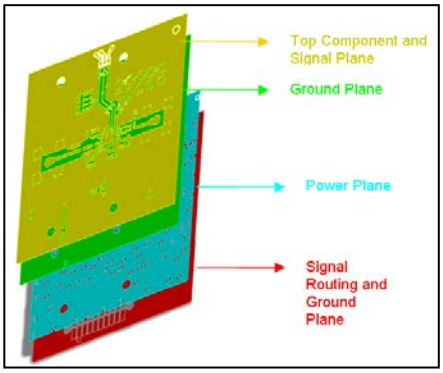


Figure 1: A two layer board stack-up. Figure 2: A four layer board stack-up

3.4 Power Supply Bypassing and Decoupling

Power supply routing is important in any RF design and, if not carefully planned, can affect the system performance undesirably. Proper routing, bypassing and decoupling avoid noise coupling into and/or entering the active device on board and affecting the performance of the system. A source of high frequency noise on a PCB can be the transient demand of current (power) by active devices, causing high frequency harmonics to be generated. The generated noise can travel to the power supply pins of the devices, producing undesired performance. To prevent this high frequency noise from reaching the power supply pins of the devices it is bypassed to the ground plane using a capacitor which provides a low impedance path to the high frequency noise.

Also, the digital section of the design switches rail to rail rapidly, which generates high frequency harmonics. These high frequency harmonics can couple on the power supply lines if the power supply is not routed and decoupled properly. Also, there may be undesired coupling between the power supply lines. The power supply lines and digital lines must be

routed away from the RF section, and decoupling must be done to isolate the corresponding power supply pin from the high frequency noise on other sections. Additionally, the bypass/decoupling capacitor must be carefully selected taking into consideration the self resonance frequency (SRF) of the capacitor. Above the SRF the capacitor behaves as an inductor, and thus a capacitor is effective only up to SRF. Figure 3 represents the capacitor characteristics. It is recommended to keep decoupling/bypass capacitors as close as possible to the supply pins. TI reference designs are designed to take into effect the above considerations, and it is recommended to copy them as closely as possibly in any application design.

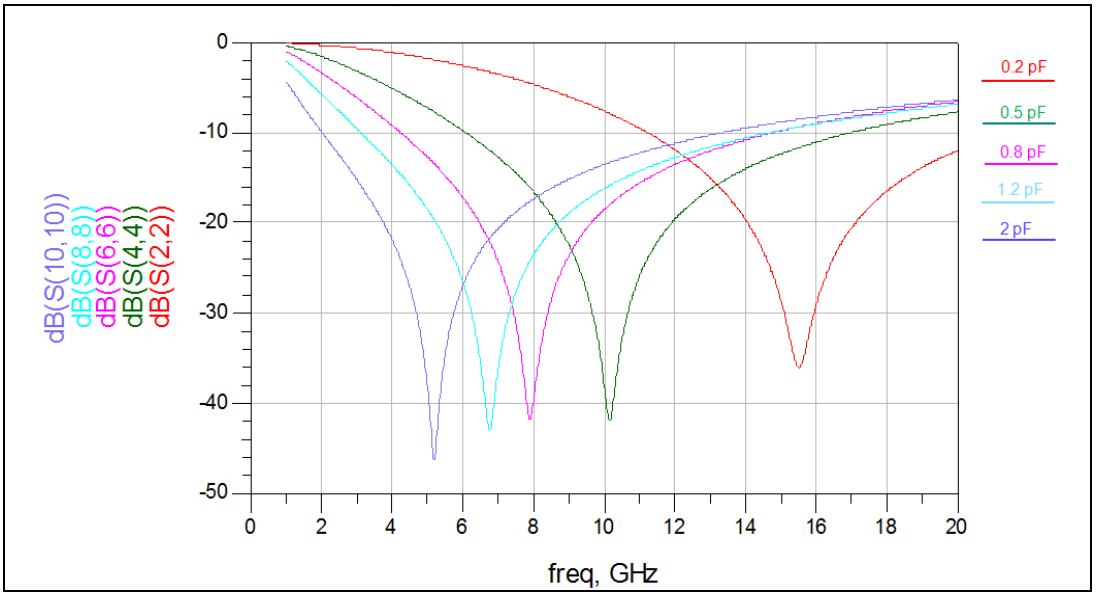


Figure 3: SRF vs. Capacitor Value (This is a general representation of SRF variation with capacitor values but capacitor of different types and from different vendors will have different SRF)

3.5 Ground Plane

It is highly recommended to have a continuous/un-interrupted ground plane in any RF design. If the ground plane is divided, especially under the RF section, then the return current paths may become longer, adding undesired inductance and leading to undesired performance. A continuous ground plane underneath the design also provides for easy connection to the ground by allowing one to drop vias from the pads to be grounded. This also eliminates the need for any additional traces that would otherwise have to be drawn to connect to the ground plane that would have added additional and unwanted inductance, leading to undesired performance.

Additionally, on the top component plane it is usually a good idea to fill the unused area with ground plane and then connect this top fill with the ground plane below with several vias. It is recommended to have these vias spaced about $1/10^{th}$ of the wavelength apart. Having a ground shield as in Figure 4 will protect the RF section from coupling to other sections on a larger board or from nearby interfering sources.

In a four-layer design a continuous ground plane also provides isolation from the power plane.

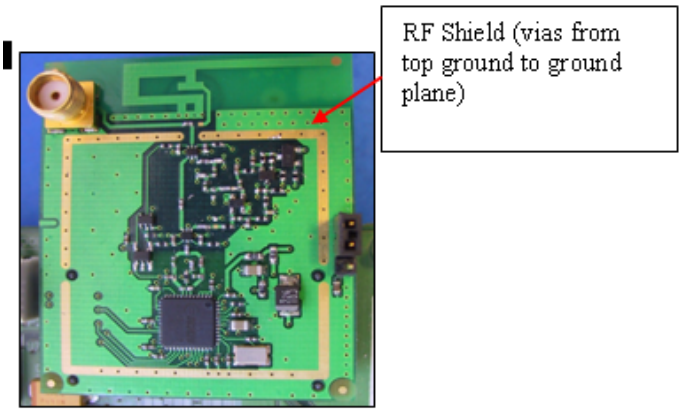


Figure 4: Showing RF design with Grounded Via Shield

3.6 Component Orientation

Inductors on the PCB have associated with them a magnetic field which can couple with other components and can affect the design performance in undesired manner, if not taken into account. TI reference designs are designed carefully considering such coupling effects, and thus it is recommended to follow the component placement and orientation as suggested in the TI reference designs.

4 Copying TI Reference Design

The first step to start a RF PCB layout is to understand the PCB board properties, i.e. the PCB stack-up and dielectric properties (dielectric constant and loss tangent). TI reference designs include a document describing PCB board stack-up and board properties such as stacking heights, dielectric constant and loss tangent of the board's dielectric. Check the TI reference design-specified board parameters and confirm with your board manufacturer if you can use these recommended specifications. If not, then refer to the application note AN068 [2] on how to adapt the reference designs for the board stack-up changes. Then copy the schematic and layout as closely as possible.

Also, if the design requires translating a two-layer TI reference design to a four-layer PCB design, then the height between the top layer and ground plane may change. This changes the impedance of the RF path. The change in the impedance in the RF path must be accounted for by adjusting the widths of the traces as explained in the application note AN068 [2].

Additionally, to make it easier to copy the reference designs, many TI reference designs includes a white box silkscreen that shows the extent of RF layout. Everything inside the box should be copied exactly for optimum performance. Anything outside the box can be changed freely.

The checklist below provides important RF PCB design considerations to be followed, and it is highly recommended that the designers verify their designs with the suggested points below. Following these points in the checklist will help to achieve optimum performance from the designs.

1. Ensure that you follow the datasheet layout recommendation unique to the part (CCXXXX).
2. 0603(mils) discrete parts are not recommended because of size and parasitic values.
3. Verify that bypassing capacitors are as close as possible to the power supply pins that they are meant to bypass.
4. Ensure each decoupling capacitor only decouples the specific pins recommended on the reference design and that the capacitor is correct value and type.
5. Ensure that decoupling is done pin<>capacitor<>via.
6. Verify the stack-up matches the reference design. If the design is a 4-layer PCB; verify that ground plane is layer two right below top/component side.
7. Changing the layer spacing/stack-up will affect the matching in the RF signal path and should be carefully accounted for as explained in AN068 [2].
8. Verify that the ground plane matches the reference design. There should be a solid ground plane below the device and the RF path. There should be no ground plane below the antenna unless you are using an antenna whose manufacturer recommends a ground plane (for example, a whip antenna).
9. Verify that RF signal path matches the reference design as closely as possible. Components should be arranged in a very similar way and oriented the same way as the reference design.
10. The crystal oscillator should be as close as possible to the oscillator pins of the part. Long lines to the oscillator should be avoided if possible.
11. Verify that the top ground pours are stitched to the ground plane layer and bottom layer with many vias around the RF signal path. Compare to the reference design. Vias on the rest of the board should be no more than $\lambda/10$ apart.
12. If the part has a differential output, ensure that the traces in the differential section are symmetrical as in the reference design.
13. If the design uses a battery (such as a coin cell), the battery will act as a ground plane and should therefore not be placed under the antenna.
14. If the reference design specifies using T-Lines (Transmission Lines), it is very critical to ensure that the T-Lines match the reference design exactly.

15 Verify that the under-the-device power pad layout is correct. The solder pads and mask should match and the opening size should ensure correct amount of paste. Vias should be the correct number and masked/tented to ensure that they don't suck up all the solder, leaving none to solder the chip to pad. (Refer to the datasheet for layout recommendation for the corresponding part.)
16 The board should specify impedance controlled traces. That is, the layer spacing and FR4 permittivity should be controlled and known.

Important considerations for Antennas:

17 If using an antenna from a TI reference design, be sure to copy the design exactly and check if the stack-up in the reference design matches your stack-up.
18 Changes to feed line length of antenna will change input impedance match.
19 Any metal in close proximity, plastic enclosure, and human body will change the antenna's input impedance and resonance frequency, which must be considered in the design.
20 For multiple antenna on same board, use antenna polarization and directivity to isolate.
21 For chip antennas verify that the spacing from and orientation with respect to the ground plane is correct as specified in antenna's datasheet.
22 It is a good practice to add a pi-network after the balun filter network for antenna impedance matching. Component values can be calculated after the PCB is fabricated and impedance measurement looking into antenna and the balun network as made at the desired frequency. If not required, the shunt components can be left un-mounted and a 0 ohm resistor can be used as series component.

5 Debug Socket on the Design

A good method to perform quick RF performance checks of a design, such as PER, range, etc., is to attach the designed board to a PC through a SmartRF04EB board, SmartRF05EB board, or CC-Debugger. The SmartRF™ Studio application can then be used to verify the design performance. The SmartRF04EB and SmartRF05EB boards provide a debug connector to interface to custom designs which do not have connectors as provided on the EM boards. The pin out of this 10-pin connector is given in table 1. Adding a 10-pin connector on the board with connections to the pins specified in Table 1 will allow easy connection to the SmartRF04EB, SmartRF05EB, or CC-Debugger and allow for RF performance checks. Usually the designs lack space for a 10-pin connector; in those cases the required pins to interface a LPRF transceiver are CSn, SCLK, SI, SO, VDD and GND, while for the TI LPRF RF SoC devices, these are DD, DC, Reset_N, VDD and GND. These pins can be routed to a test port on the board and can be connected to the corresponding pins on the SoC debug connector on the SmartRF04EB and SmartRF05EB, or to the debug connector on the CC-Debugger, for easy and quick RF performance checks of the design.

Pin	Function	Note
1	GND	
2	VDD	Used to set correct voltage for voltage level converter
3	Debug Clock (DC)	
4	Debug Data (DD)	
5	CSn	
6	SCLK	
7	Reset_N	
8	MOSI	
9	3.3V VDD, alt NC	Delivers VDD from SmartRF04EB
10	MISO	

Table 1: SoC debug connector pin-out

6 Examples of things not to do

This section details commonly-made mistakes on a RF layout.

6.1 Long RF Trace lengths and mismatched traces in differential RF sections

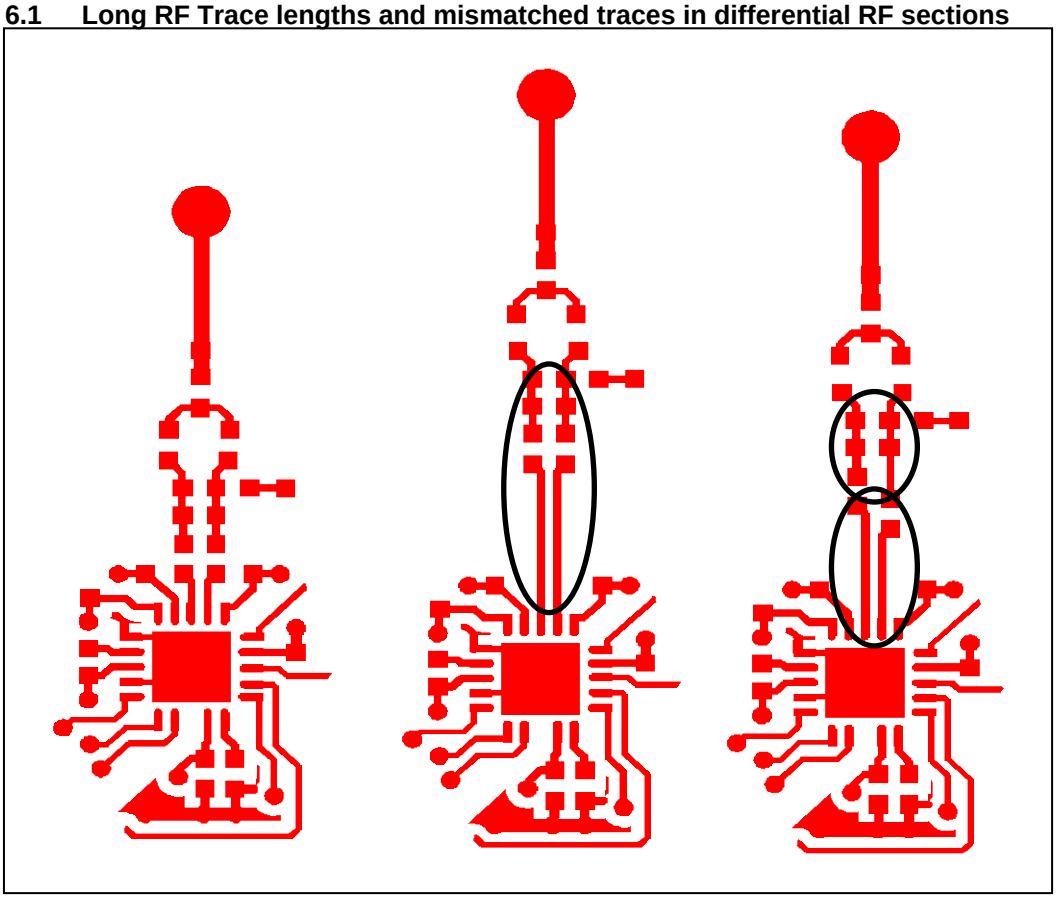


Figure 5: (a) Ideal Case (b) Extended RF Transmission Lines (c) Mismatched RF Lines

The TI reference designs for LPRF Devices with balanced outputs (RF_P and RF_N) show simple, low cost matching and balun networks on the printed circuit board. It is recommended to follow the reference layout to avoid commonly made mistakes as shown below for optimum performance.

As shown in the Figure 5(a) it is recommended to keep RF traces short, unlike cases 5(b) and 5(c). Longer traces as in 5(b) introduce undesired impedance changes and affect the matching network, leading to undesired performance. Additionally, on devices with differential outputs, it is critical that the traces to the balun network and within the balun section be symmetrical as in the reference designs. Figure 5(c) shows a commonly made mistake in layouts where the RF traces are long and unsymmetrical, which distorts the performance of the differential balun, leading to undesired performance.

6.2 Digital lines near/below the RF path

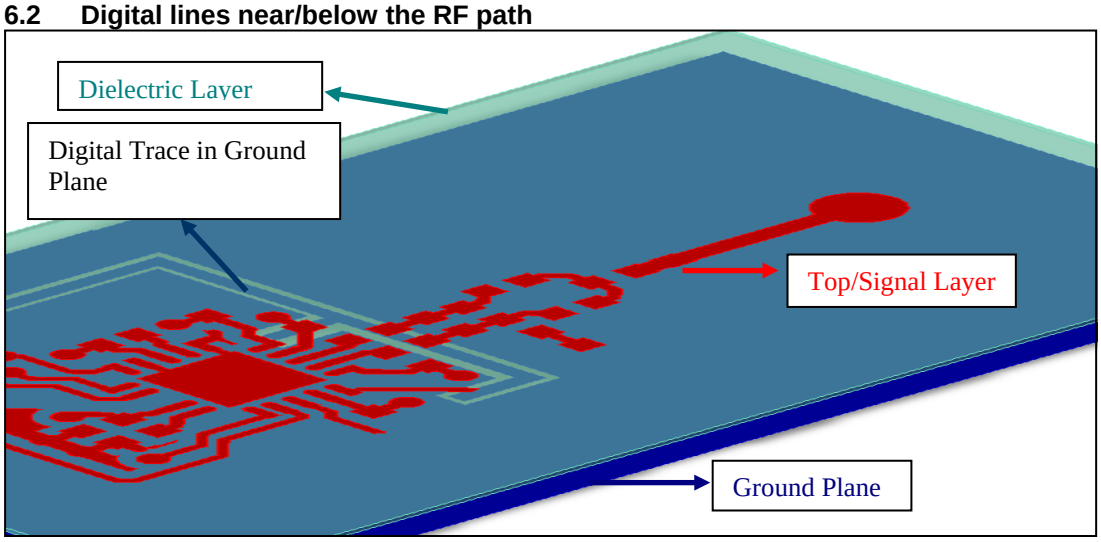


Figure 6: Digital Lines directly below the RF path

As shown in the Figure 6 this layout has digital traces near/below the RF path. The transition on digital lines are rail to rail and have high frequency harmonics which can couple into the RF lines where the signal amplitude is very small and superimpose on the small RF signal, giving undesired operation.

Also, dividing the ground plane under the RF section introduces longer return paths for RF current, introducing undesired performance. It is recommended to have a solid ground plane, especially under the RF section.

6.3 Digital Traces below/near the crystal oscillator

It is recommended not to place any digital trace below/near the crystal oscillator and the traces from the oscillator to the chip as the coupling can be very strong and lead to undesired performance.

6.4 Bypass Capacitor Placement

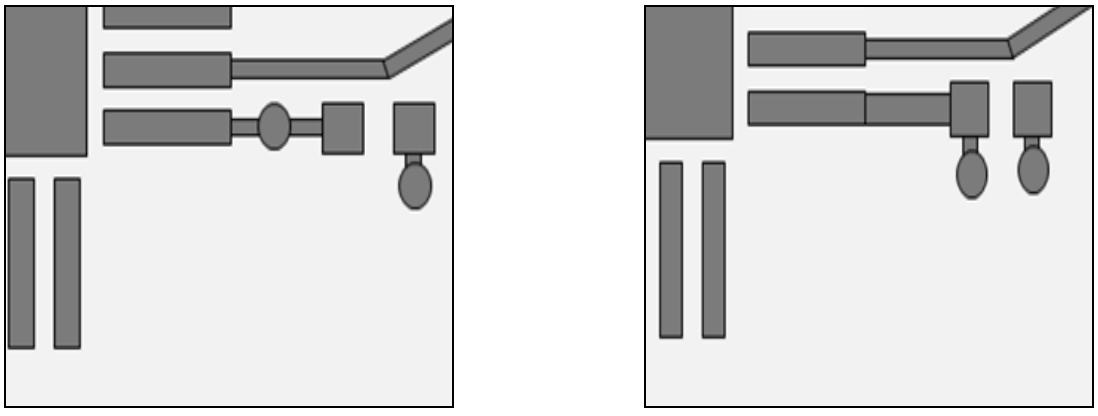


Figure 7: (a) Poor Bypassing Layout **(b) Good Bypassing Layout**

Bypassing: Do not have vias between the capacitor and active devices, as shown in Figure 7(a). The layout should be via followed by capacitor connected close to the pin on the CCXXXX (Figure 7 (b))

6.5 PCB layers swapped while manufacturing

One common mistake may occur when giving the final PCB design to the board manufacturing house by not defining the layer mapping (i.e., the positioning of the layers on the PCB stack) clearly. As a result the power and ground planes may be swapped by the manufacturer during fabrication. This can cause significant effects on the performance of the design. This is due to the change in the trace impedance caused by the increased distance between the top signal plane and the ground plane. Also, the power plane will have increased coupling with the signal plane, causing performance degradation. Solving the problem requires re-manufacturing the board, increasing the development time for the design.

To avoid the undesired mapping of the planes on the board, or giving special information for the board such as desired permittivity, layer spacing, etc., for the board, it is advised to send a readme file (e.g., as included with the TI reference designs) or fabrication notes to the manufacturer. Also, several manufacturers have online forms that ask the information, and the forms must then be filled in carefully, mapping all the layers in the design carefully.

Simulation using the Advanced Design System's Momentum was performed to show the impedance change when the power and ground planes get swapped.

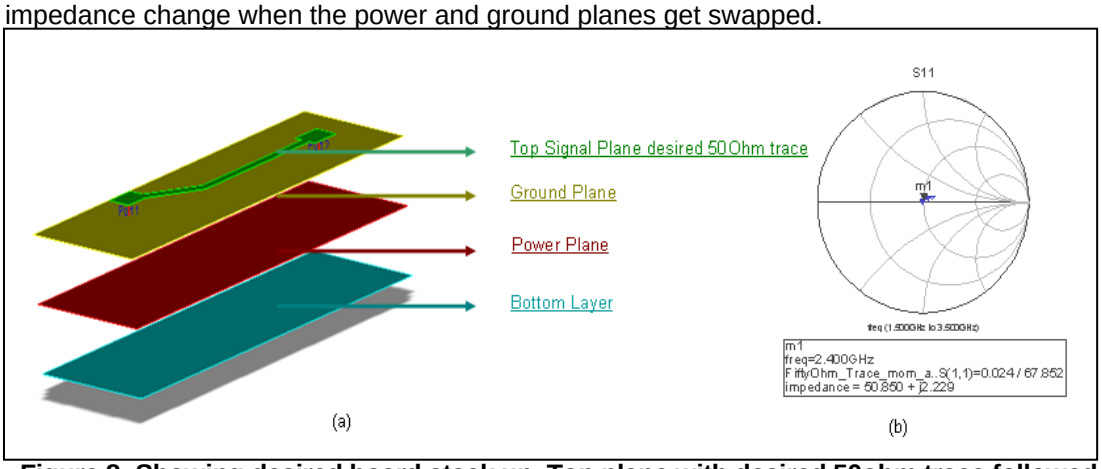


Figure 8: Showing desired board stack up. Top plane with desired 50ohm trace followed by ground, power and then bottom layer. The simulated impedance of the trace is shown in (b) to be 50.85+j2.229 at 2.4GHz

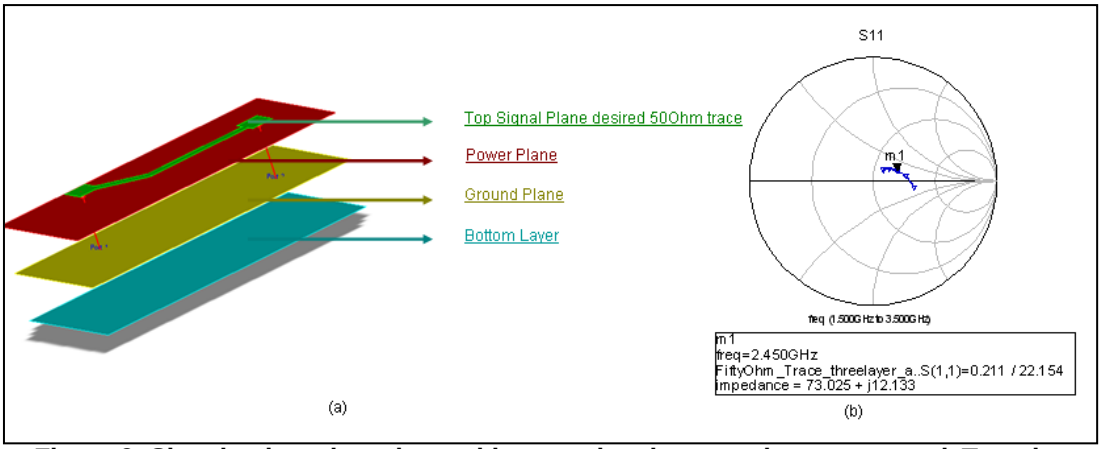


Figure 9: Showing board stack up with ground and power planes swapped. Top plane with desired 50ohm trace followed by ground, power and then the bottom layer. The simulated impedance of the trace is shown in (b) to be 73.025+ j12.133 at 2.4GHz

6.6 Silkscreen below the chip

It is recommended not to place the silkscreen markings below the area where the chip is to be placed as it provides obstructions for the chip to be soldered properly to the PCB pads, leading to undesired performance.

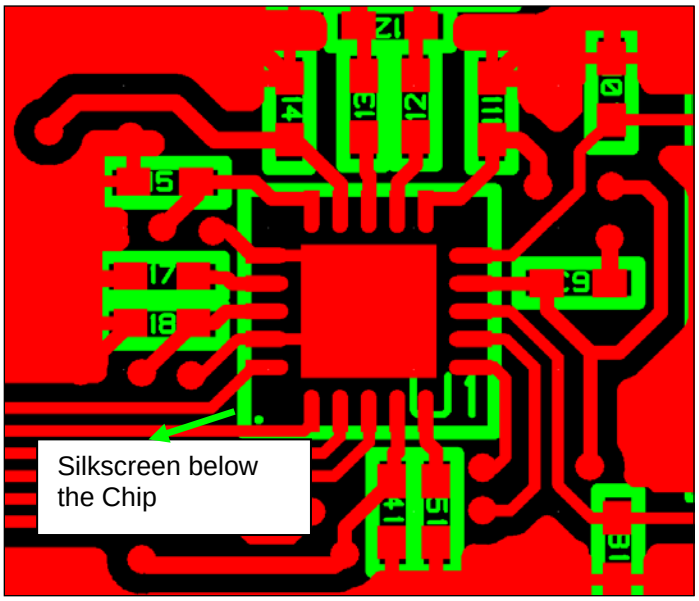


Figure 10: Showing Silkscreen markings in the area under the chip

6.7 Power Pad Layout

Power pad layout is critical for successful operation of a RF design using CCXXXX devices. The area under the chip on CCXXXX devices is used for ground connection and shall be connected to the ground plane with several vias for good thermal performance and sufficiently low inductance to ground. The datasheet (e.g., Figure 11) and the reference designs specify the layout for this section, specific to each part, describing number of vias, their placement, solder mask and solder resist layout. It is recommended to follow the recommendations and have these vias “tented” (covered with solder mask) on the component side of the PCB to avoid migration of solder through the vias during the solder reflow process. The solder paste coverage should not be 100%; if it is, out gassing may occur during the reflow process, which may cause defects (splattering, solder balling). Use of “tented” vias reduces the solder paste coverage below 100%.

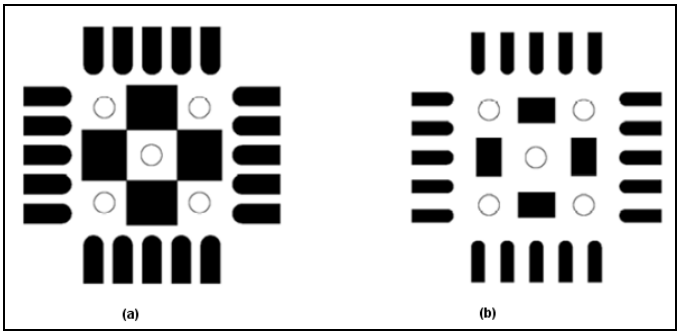


Figure 11: Showing an example of power pad layout given in the CC1101 datasheet [3]._(a) Top Solder Resist Mask (Negative), (b) Top Paste Mask. Circles are Vias

7 Conclusion

The application note provides guidelines and a checklist to copy TI reference designs for optimum performance. It also provides various commonly-made RF PCB design mistakes. Following the suggested recommendations will allow the designers to have designs with optimum performance on their first board fabrications reducing design time and cost involved.

8 References

Cited references

[1] David M. Pozar “Microwave Engineering – Third Edition”, John Wiley 2005

General references

[2] AN068 - Adapting TI LPRF Designs for Layer Stacking (SWRA236)

[3] CC1101 Single-Chip Low Cost Low Power RF-Transceiver (SWRS061)

9 General Information

9.1 Document History

Revision	Date	Description/Changes
1.0	05/06/2011	Initial release.
1.1	08/01/2012	Keywords added CC254x devices

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46C and to discontinue any product or service per JESD48B. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products		**Applications**	
Audio	www.ti.com/audio	Automotive and Transportation	www.ti.com/automotive
Amplifiers	amplifier.ti.com	Communications and Telecom	www.ti.com/communications
Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
OMAP Mobile Processors	www.ti.com/omap	**TI E2E Community**	e2e.ti.com
Wireless Connectivity	www.ti.com/wirelessconnectivity		

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265