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Input and Output Characteristics of Digital Integrated Circuits at 2.5-V Supply Voltage

Application Report

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Abstract

This application report contains a comprehensive collection of the input- and output-characteristic curves of integrated circuits from various 2.5-V logic families. These curves go beyond the information given in data sheets by providing additional details regarding the characteristics of the devices. This knowledge is particularly useful, for example, when choosing a device for use in a bus system, or when the waveforms expected in a transmission system must be predicted using a Bergeron chart. These oscillograms assist in generating models for simulation programs that analyze the dynamic behavior of the devices in a particular environment.

1 Introduction

For a long time, a 5-V supply voltage was standard for the design of new systems. However, with the reduction of the supply voltage, system power consumption can be reduced directly, as shown by the general formula for power consumption:

$$P_{STAT} = V_{CC} \times I_{CC} \quad (1)$$

Compared to a 5-V system, 3.3-V systems save about one-third and 2.5-V systems save about one-half of the consumed energy. However, with the reduction of the supply voltage, drive capability of the logic circuit also is reduced.

The parameters in the data sheet give only a very limited indication of a device's behavior in a system. For example, data sheets generally give only information regarding the behavior over the input and output (I/O) voltage range of 0 to 5 V, 3.3 V, and 2.5 V. The output currents specified over this range provide an incomplete picture of in-system performance.

Behavior of the device outside the usually accepted operating conditions is often of interest. For example, this is true when the characteristic curves are needed to predict signal waveforms resulting from line reflections.

By using the I/O characteristics and the Bergeron method, along with a knowledge of the load resistance, the amplitude of the line reflections can be determined.

This report presents I/O characteristics of integrated logic circuits that operate at V_{CC} = 2.5 V, mainly those that originally were designed for 3.3-V V_{CC}. However, many modern logic families are specified at multiple supply voltages. For example, AHC logic can be used at 5-V, 3.3-V, or 2.5-V supply voltage. Because three main voltages are used, I/O characteristics are provided for each voltage level. This application report deals exclusively with devices operated at 2.5 V.

Two other application reports regarding this topic are available:

- *Input and Output Characteristics of Digital Integrated Circuits at 5-V Supply Voltage*, literature number SZZA008
- *Input and Output Characteristics of Digital Integrated Circuits at 3.3-V Supply Voltage*, literature number SZZA010

With the wide range of devices available, information in this application report is limited to typical characteristics. In Sections 2 and 3, the I/O characteristics of the following devices are shown as being representative of other components that behave similarly in operating circuits:

’00 The characteristic curves of this NAND gate are representative of all logic devices having normal drive capability, such as gates, flip-flops, counters, multiplexers, etc.

’240/’244 The output characteristics of these bus-interface devices are of particular importance in deciding which family should be used for a specific system requirement. As mentioned elsewhere in this application report, the available output current has a decisive influence on the distortion of signals on bus lines.

’16240/’16244 The output characteristics of these bus-interface devices correspond with the ’240/’244 functions regarding the electrical behavior. However, these devices have 16 drivers within one package. This feature meets the market requirements, because modern designs are based on wider buses using 16 bits, 32 bits, or more bits on the backplanes. Further, the noise behavior of Widebus™ devices shows a significant improvement over the standard octal packages.

Table 1 lists representatives of the different logic families and gives an overview of I/O characteristics presented in Sections 2 and 3.

Table 1. Representatives of the Different Logic Families

FAMILY	TYPE		
	’00	’240/’244	’16244
SN74AHC	√	√	
SN74AC	√	√	
SN74LV	√	√	
SN74LVC	√	√	
SN74ALVC			√
SN74ALB			√
SN74ALVT			√
SN74LVT		√	

Because the input characteristics depend exclusively on the technology used, not on the logical function of the device, only one representative per logic family is shown (gate function ’00 or driver function ’240) in Section 2.

Section 4 shows how to calculate line reflections using the Bergeron method and data from the SN74ALVCH16240 device.

Measurement results demonstrating different switching behaviors of the various logic families are given in Section 5. For these measurements, the devices under test were loaded with a 1.3-m-long coaxial cable having a characteristic impedance of 50 Ω; the end of the line was not connected, i.e., open circuit. These waveforms provide good insight into the dynamic behavior of the devices.

Texas Instruments (TI™) offers the advanced very low-voltage CMOS (AVC) logic family as an optimized solution for the next low-voltage node with 2.5-V supply voltage. The TI application report, *AVC Logic Family Technology and Applications*, literature number SCEA006A, discusses the features and benefits of 2.5-V logic.

2 Input Characteristics

The high impedance of the input stage of the logic circuit determines the input characteristics of logic circuits in the positive range (see Figures 1 through 5).

All logic families that are discussed in this report have CMOS input stages and use technologies based either on the CMOS or BiCMOS manufacturing process. In both cases, CMOS input stages are used. CMOS input stages are controlled exclusively by the applied voltage so there is no current flowing into the input stage. Therefore, the input impedance of CMOS and BiCMOS devices is in the megohm range. Negative-voltage peaks are limited by a protection diode.

The bus-hold circuit represents a special circuit in the input stages of the LVT and ALVT logic families and, optionally, is available in the LVC and ALVC devices. Inputs of devices that have the bus-hold circuit hold the last valid logic state. This feature is useful if an input stays undefined, for example, during a high-impedance state on the bus. Using the bus-hold circuit eliminates the need for pullup or pulldown resistors. Devices with the bus-hold circuit have H in their part number, for example, SN74LVTH245.

A more detailed application report, *Bus-Hold Circuits*, literature number SDZAE15, is available from TI.

Other application reports and literature are listed in Section 7.

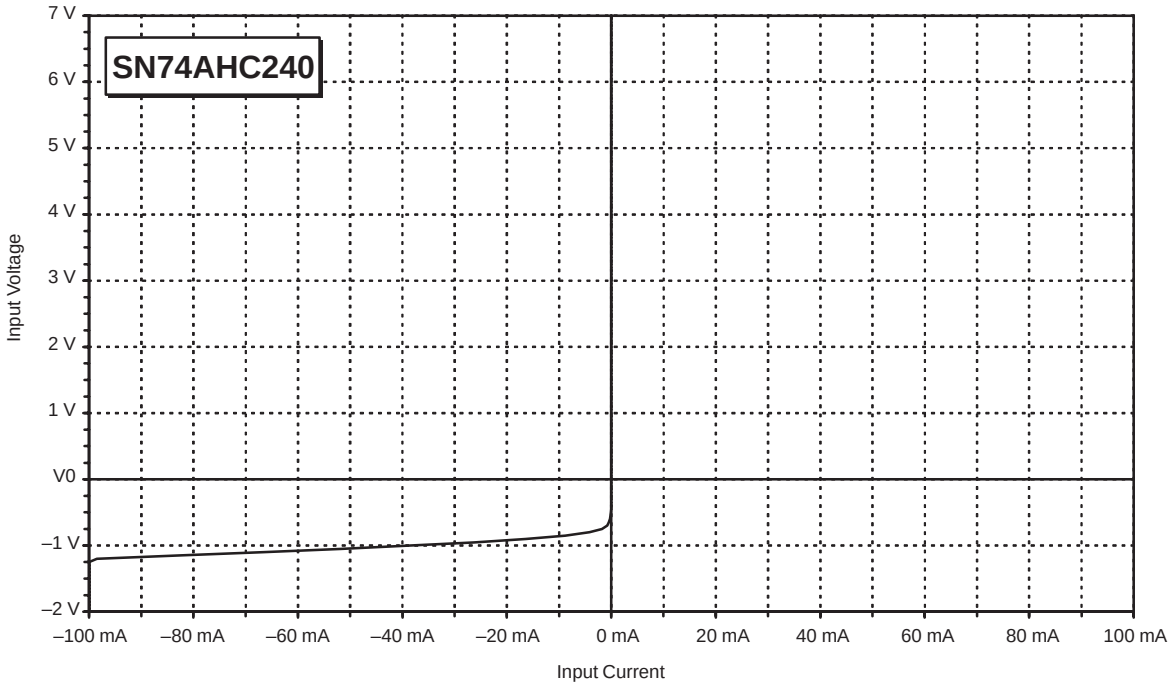


Figure 1. Input Characteristic of the SN74AHCxxx Series

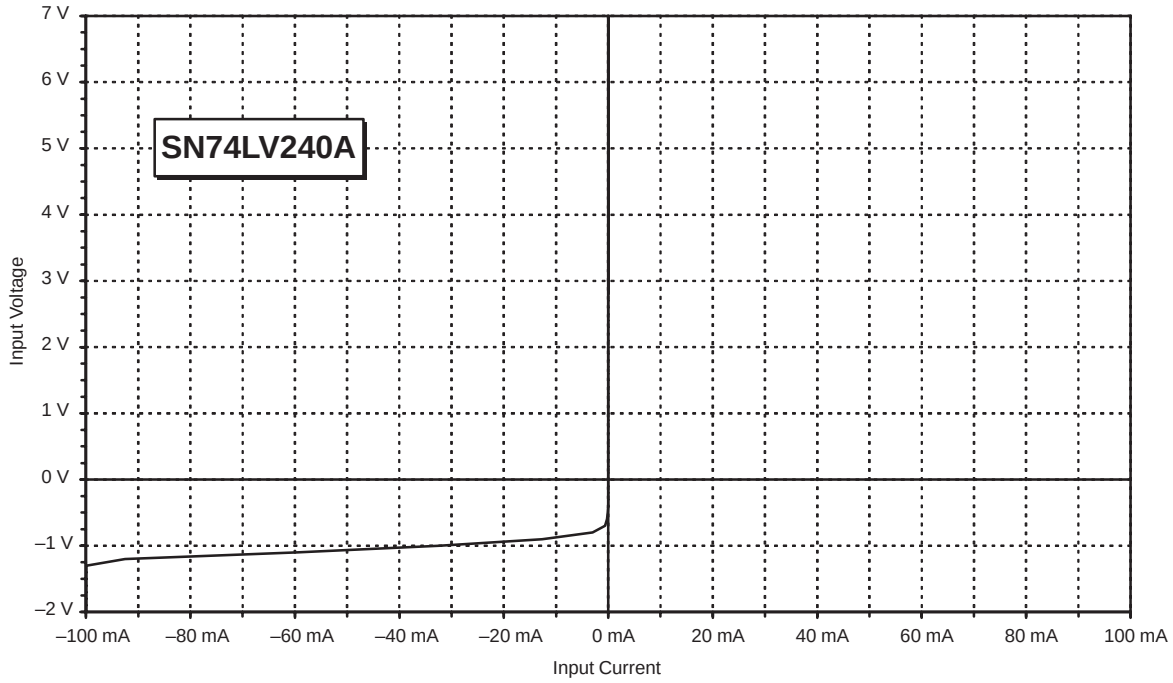


Figure 2. Input Characteristic of the SN74LVxxx Series

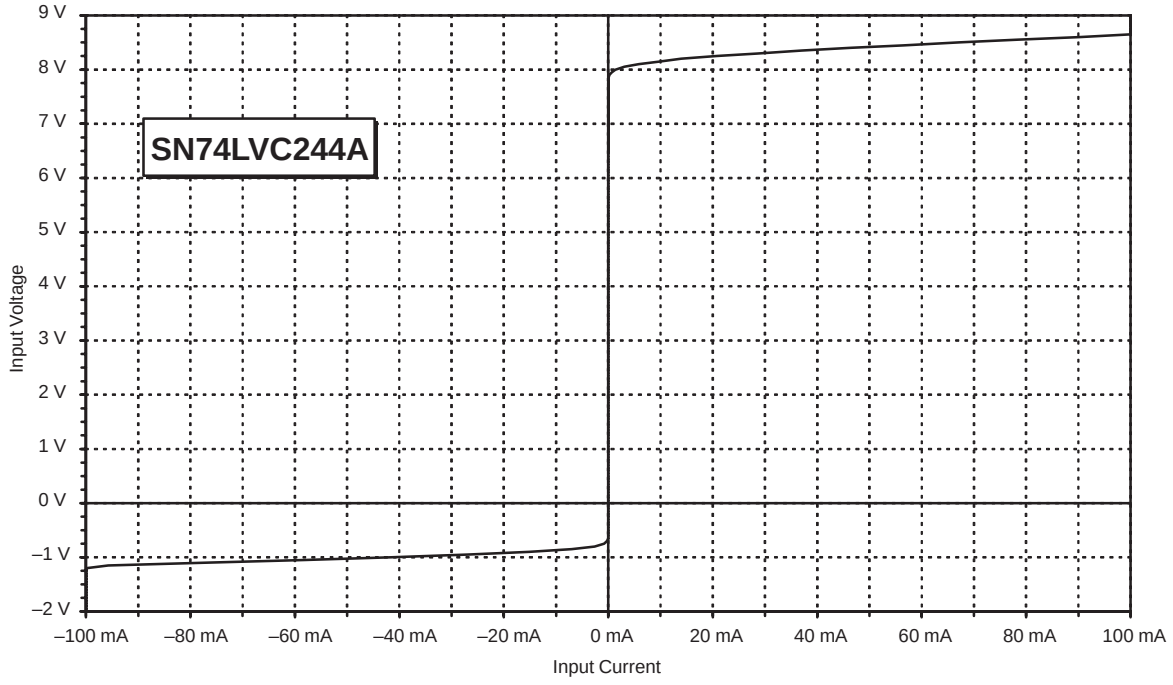


Figure 3. Input Characteristic of the SN74LVCxxx Series

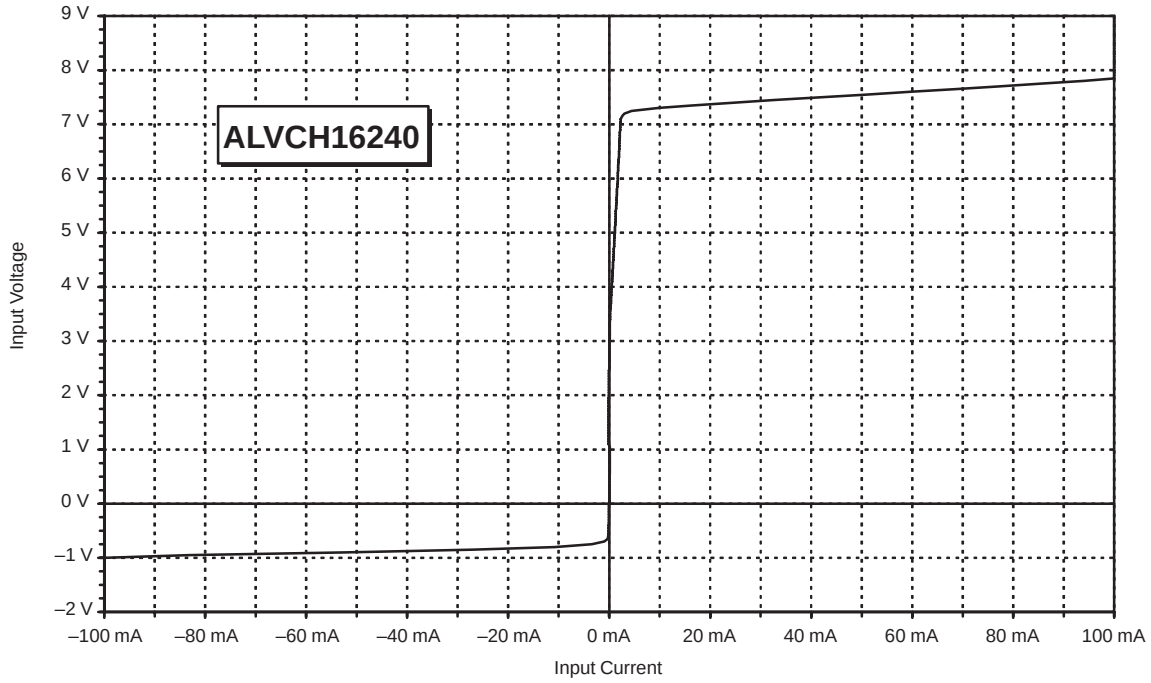


Figure 4. Input Characteristic of the SN74ALVCHxxx Series

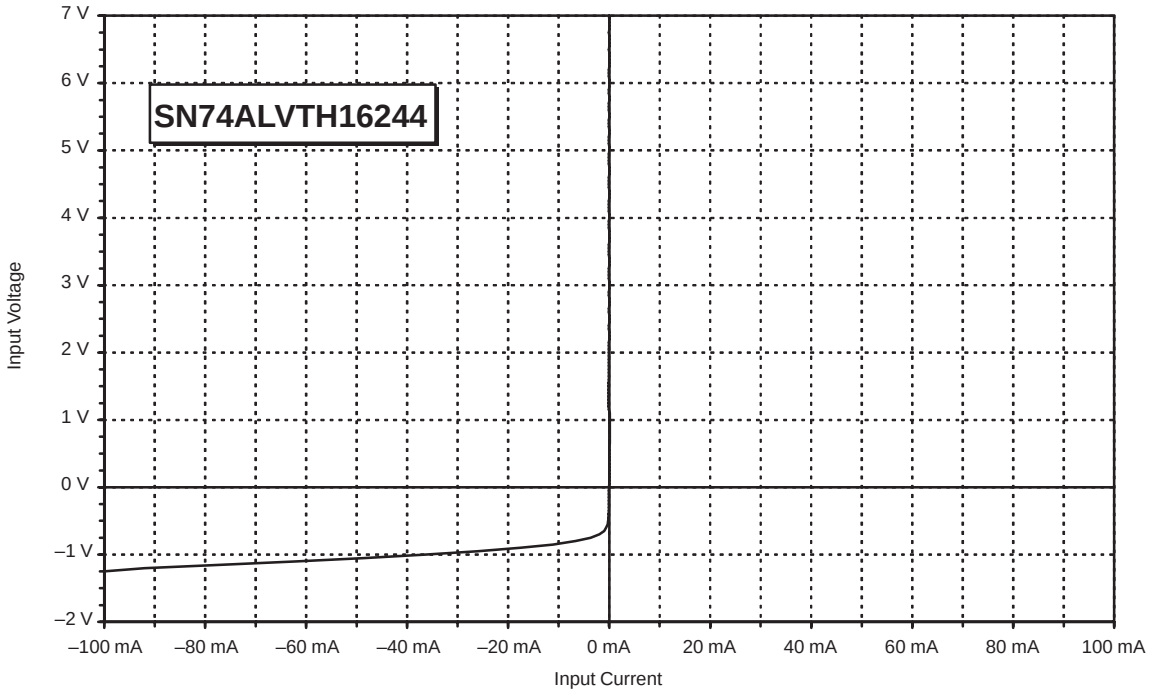


Figure 5. Input Characteristic of the SN74ALVTHxxx Series

3 Output Characteristics

The output stage of a logic device in the high logic state behaves like a voltage source with an open-circuit voltage of V_{CC} for CMOS logic, low-voltage BiCMOS logic, respectively. The internal resistance for the high state is inversely proportional to the drive capability of the device. The internal resistance for standard logic families is 15 Ω to 60 Ω.

In the low logic state for positive voltages, the output resistance is based on the internal resistance of the conducting transistor, i. e., collector-emitter for BiCMOS technologies and drain-source resistance for CMOS technologies. Negative-voltage peaks are again limited by a protective diode. The output stages of some CMOS logic families (e.g., SN74AHC) also have an output protective diode that is connected to V_{CC}. This diode limits the positive output voltage to V_{CC} + 0.7 V.

3.1 Series Damping Resistors (SN74XXX2xxx, SN74XXXR2xxx Devices)

In the LVC, ALVC, LVT, and ALVT families, TI offers driver options with integrated series resistors of about 25 Ω.

With damping resistors in the output stage, the effective output impedance of the driver is about 50 Ω. If the value of the line impedance is also in the range of 50 Ω, no line reflections are observed at the output of the device. In this case, the beginning of the line is terminated perfectly. This option is especially beneficial in memory applications where overshoots and undershoots can cause malfunctions. In point-to-point applications, near-ideal signal shapes can be achieved. The 2 in the part number indicates the series damping resistor on the output port, for example, SN74ALVCH162244. The R indicates series damping resistors on both ports of bidirectional devices, for example, the SN74ALVCHR16245.

Further information about series damping resistors is given in the TI application report, *Bus-Interface Devices With Output Damping Resistors or Reduced-Drive Outputs*, literature number SCBA012.

Other application reports and literature is listed in Section 7.

3.2 Auto3-State Output of the ALVT Family

The auto3-state function, which is implemented in the output stages of the ALVT family, represents a specialty. The principle is shown in Figure 6. Output characteristics of representative devices are shown in Figures 7 through 14.

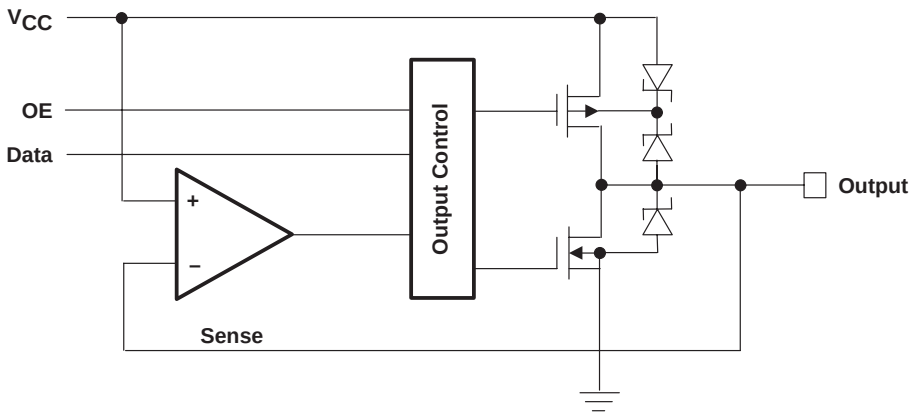


Figure 6. Simplified Auto3-State Output Stage of ALVT Devices

Assume that the output is in the active-high state and a comparator monitors the voltage at the output and compares it with the supply voltage. If the voltage that is applied externally to the output exceeds the supply voltage, the output stage is switched to the high-impedance state. In this case, the logic levels applied to the data and control input pins of the device are irrelevant.

A current of about 30 mA is needed to trigger the auto3-state circuit so that bus contentions are prevented, but switching noise does not trigger the protective circuit. However, this also implies that the auto3-state cannot be implemented by using a simple pullup resistor.

Current can flow into the output only in the case of an active high. If the output is set to high impedance by the OE control pin, no current flows.

The series-opposed Schottky diodes always connect the back gate of the pullup transistor of the output stage to the higher voltage that is either V_{CC} or the voltage that can be applied externally to the output. In this way, current flow from the output to V_{CC} is suppressed.

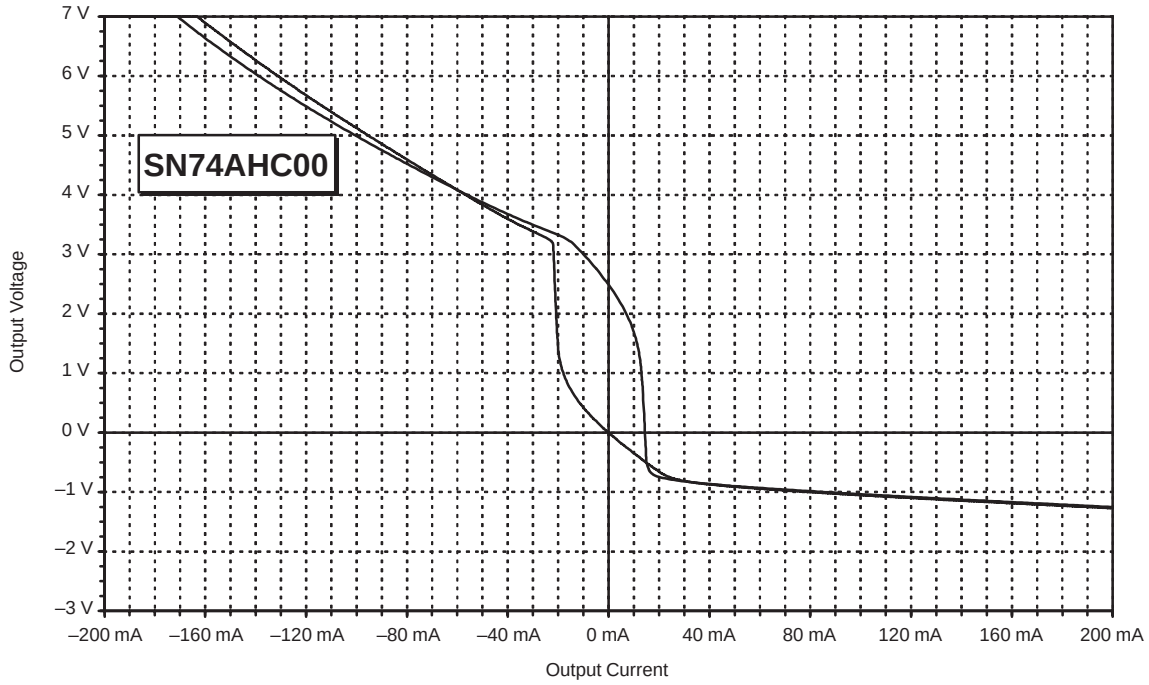


Figure 7. Output Characteristics of the SN74AHC00

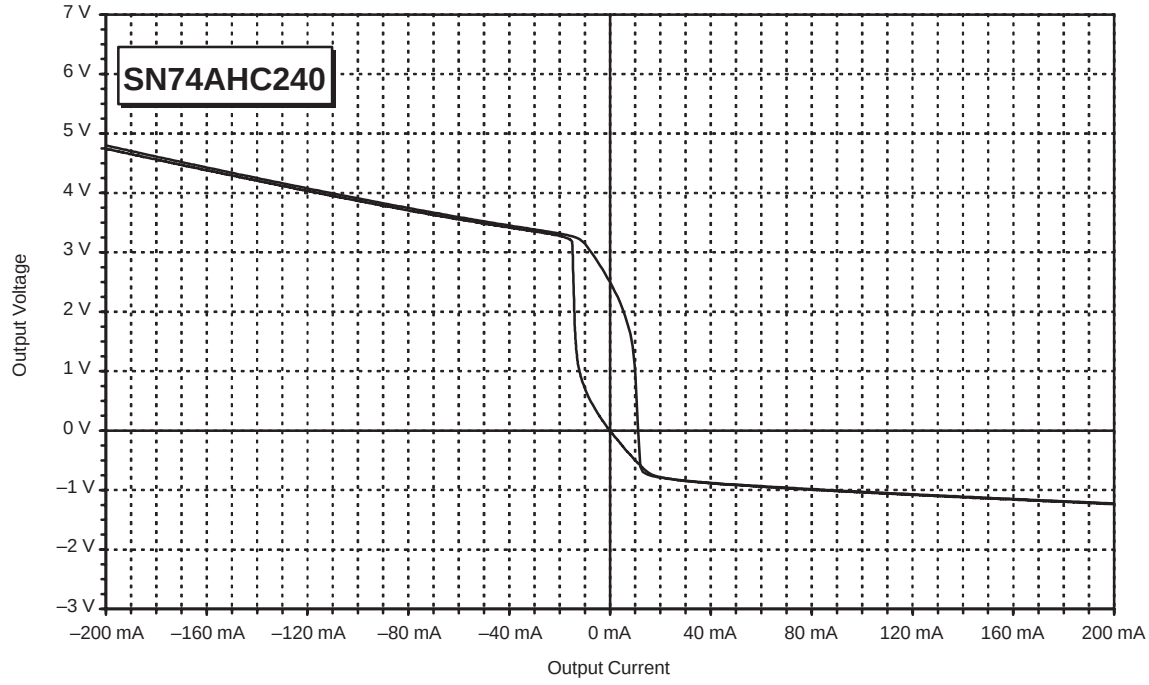


Figure 8. Output Characteristics of the SN74AHC240

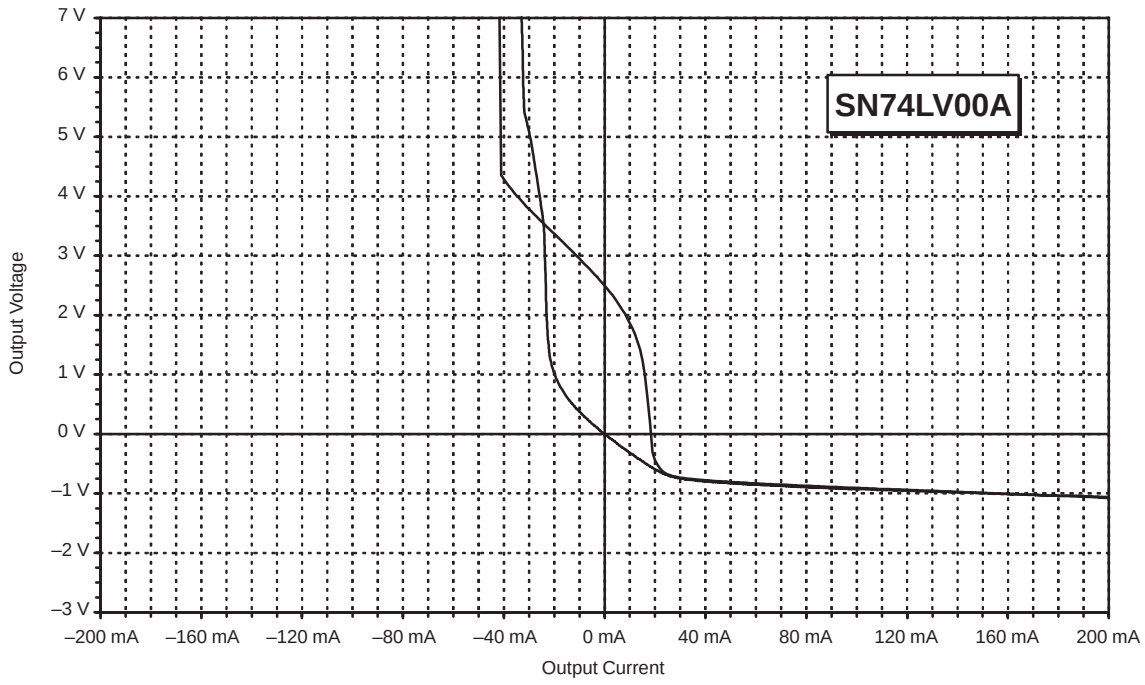


Figure 9. Output Characteristics of the SN74LV00A

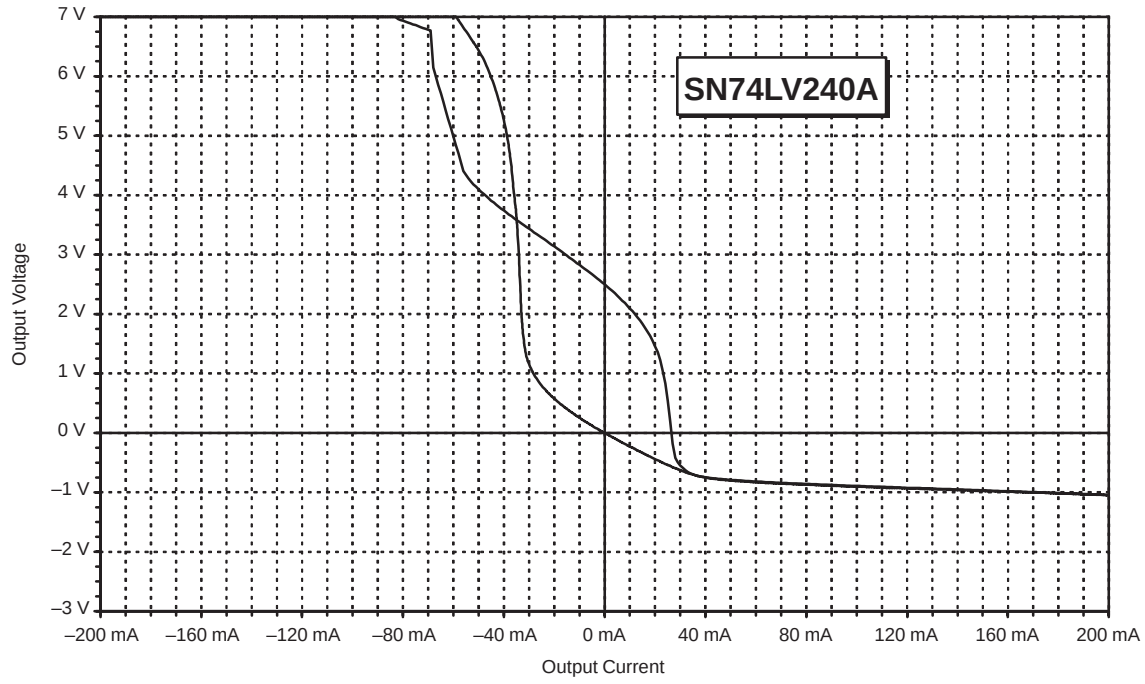


Figure 10. Output Characteristics of the SN74LV240A

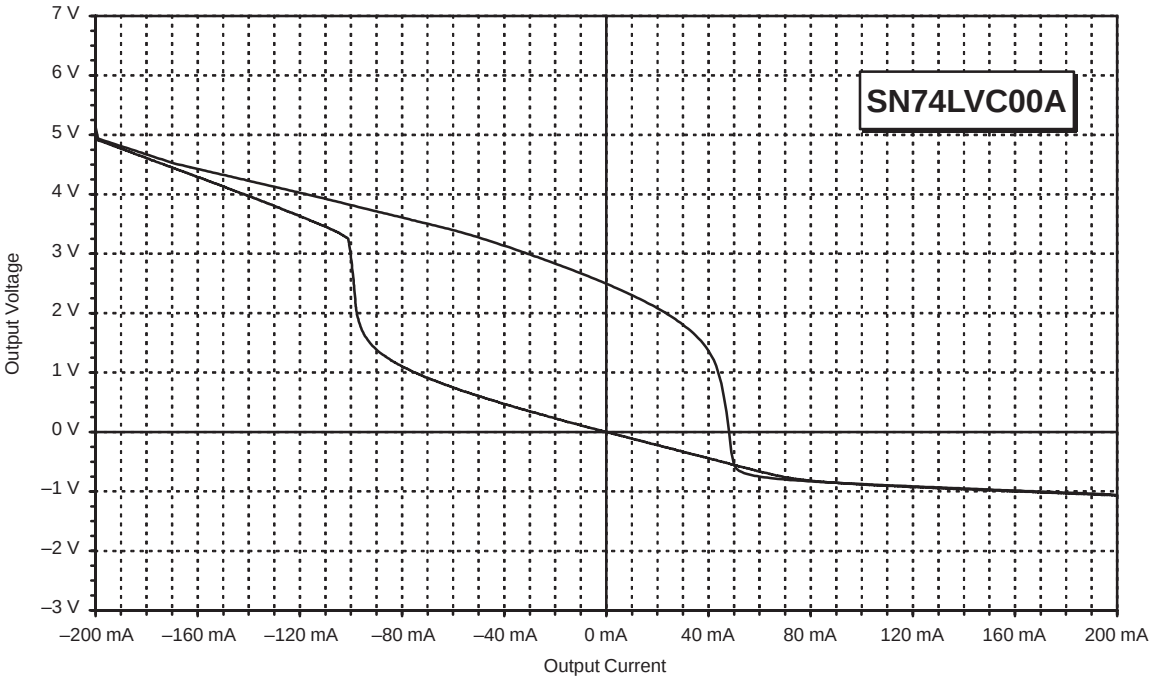


Figure 11. Output Characteristics of the SN74LVC00A

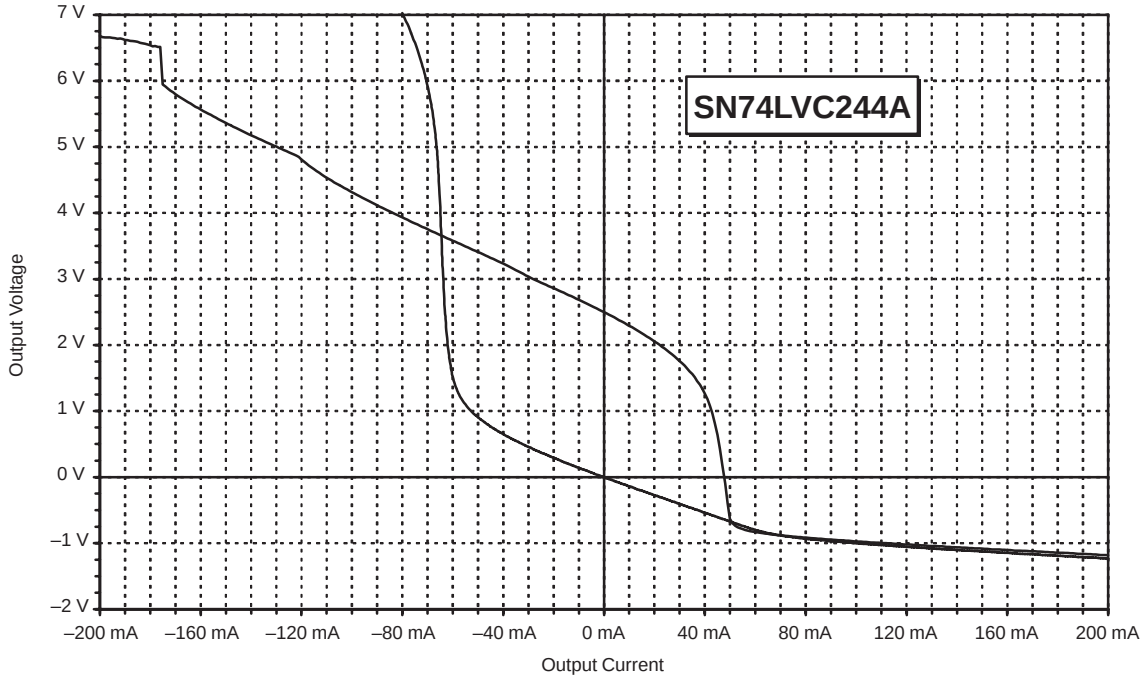


Figure 12. Output Characteristics of the SN74LVC244A

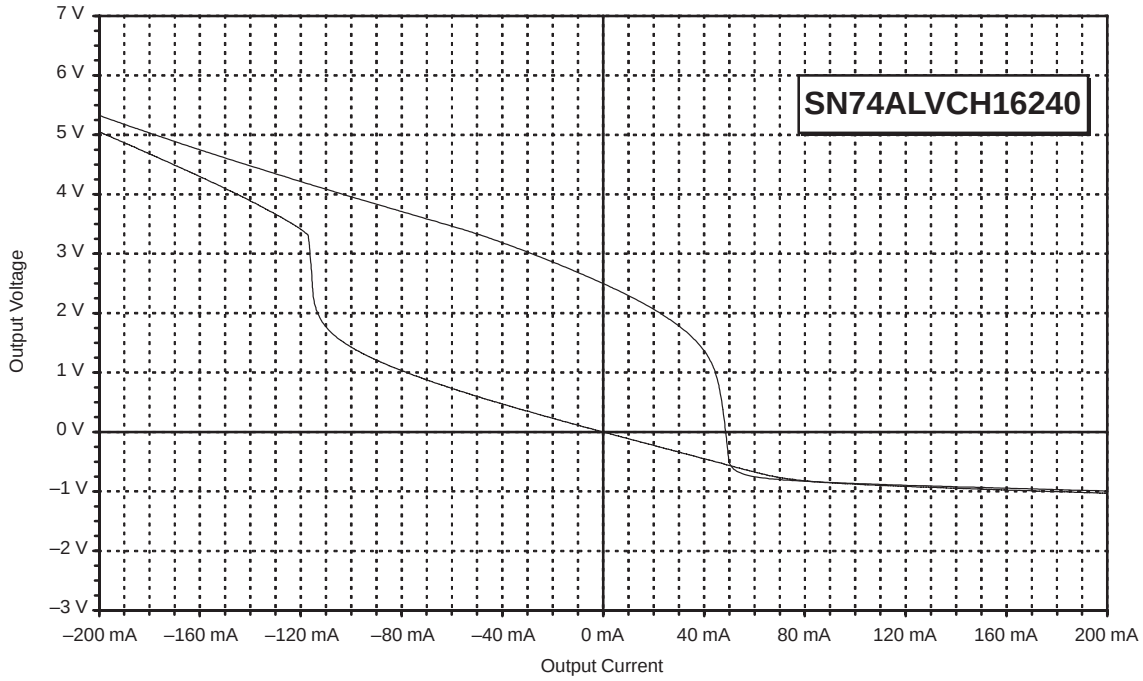


Figure 13. Output Characteristics of the SN74ALVCH16240

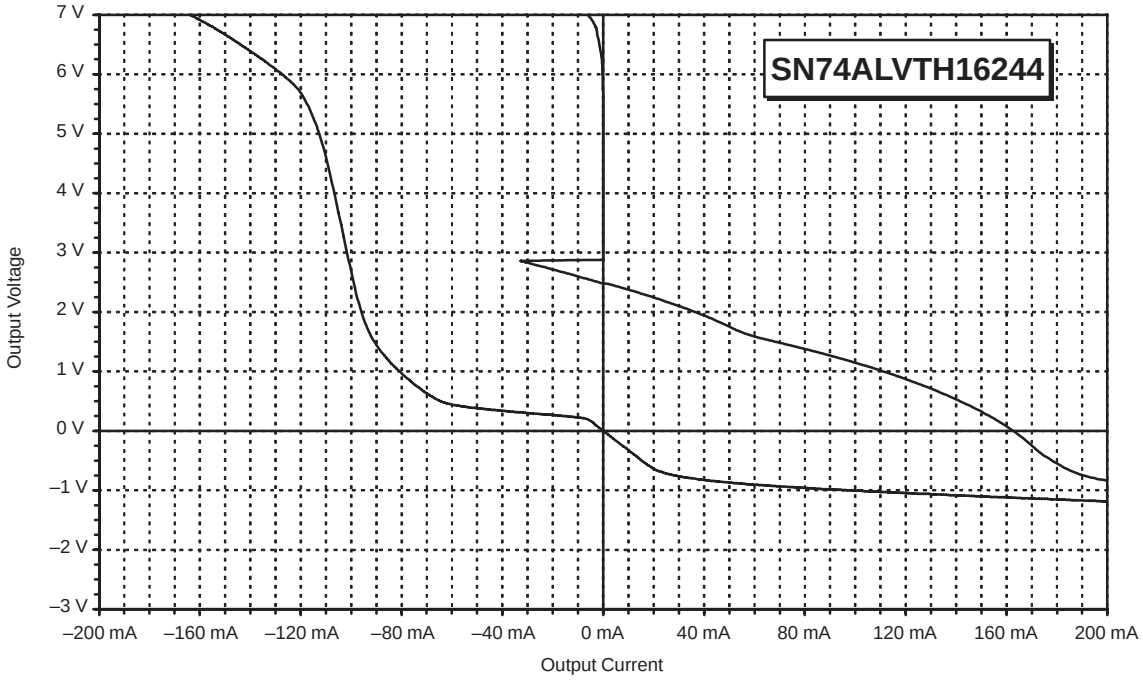


Figure 14. Output Characteristics of the SN74ALVTH16244

4 Bergeron Method Applied to the SN74ALVCH16240

The input and output characteristics, shown in Sections 2 and 3, can be used to determine the signal reflections within a certain application by using a graphical procedure known as the Bergeron method.

The prerequisite for the use of the Bergeron method is that the lines exceed a certain length:

> *If the rise time or the fall time of a signal is shorter than twice the propagation delay on the line, the line theory must be applied.*

In practice, for a line with a signal propagation of 5 ns/m and a signal with a rising or falling edge of 2 ns, starting with a line length that exceeds 20 cm [2 ns / (5 ns/m × 2)], the line theory must be applied.

For a bus line, the signal propagation delay increases to 25 ns/m, so that, in this case, the line theory must be applied for a line length that exceeds 4 cm [2 ns / (25 ns/m × 2)].

The SN74ALVCH16240 device was tested, using the measurement setup shown in Figure 15. The Bergeron method was used to predict the signal shape.

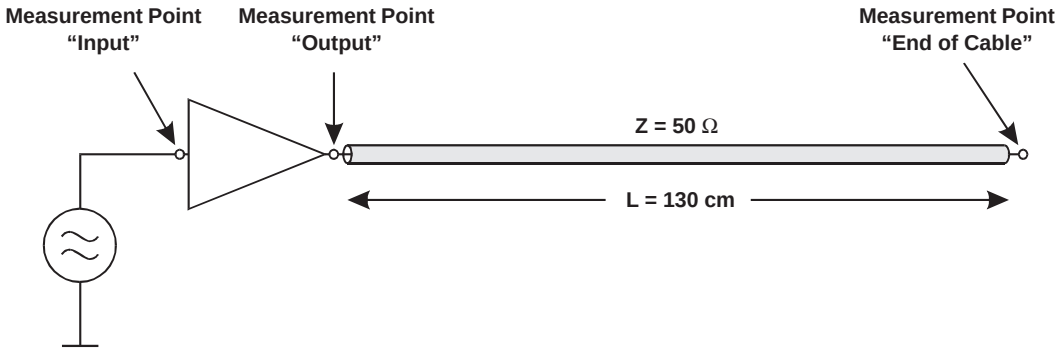


Figure 15. Measurement Setup for the Bergeron Method

The first step in the graphical solution using the Bergeron method is to draw the following characteristics in a voltage-versus-current diagram:

- Output characteristics of the SN74ALVCH16240 device
- Load characteristic at the end of the line

The output characteristics are taken directly from Figure 13. The load characteristic equals the Y axis for the investigated case because no resistor is connected to the end of the line ($R_L = \infty$).

The intersection between the load characteristic and the output characteristic represents the steady states, the current and voltage values at the line start, and the end of the line at the time $t < 0$, respectively.

4.1 Voltage Value at the Output of the Driver

For the low-to-high transition, draw a straight line, starting at the intersection of the output-low characteristic and the load characteristic. For the high-to-low transition, start the straight line at the cross point of *output-high* characteristic and the load characteristic.

The line impedance, Z_O, determines the steepness of this line. In the example, the line impedance is 50 Ω.

The intersection of this straight line and the output characteristics equals the voltage and current values at the beginning of the line at the time $\tau = 0$.

4.2 Voltage Value at the End of the Line

Now, a straight line with the steepness $-Z_O$ is drawn through this point. The intersection between this line and the load characteristics results in the voltage values at the end of the line after one propagation delay time of the line, that is, after $\tau = 1$.

Afterward, the procedure is repeated, applying straight lines to the output characteristics and the load characteristics.

The steepness of the straight line is:

- $-Z_O$ from the output characteristics to the load characteristics
- Z_O from the load characteristics to the output characteristics

In this way, current and voltage values are obtained:

- At the end of the line, at the times $\tau = 1, 3, 5 \ldots$
- At the line start, at the times $\tau = 2, 4, 6 \ldots$

The Bergeron diagram is shown in Figure 16. The related diagram (see Figure 17) shows the line reflections.

The calculated values of the Bergeron procedure match very well with the measured signal shapes. Another TI application report, *The Bergeron Method: A Graphic Method for Determining Line Reflections in Transient Phenomena*, literature number SDYA014, describes the graphic procedure in more detail

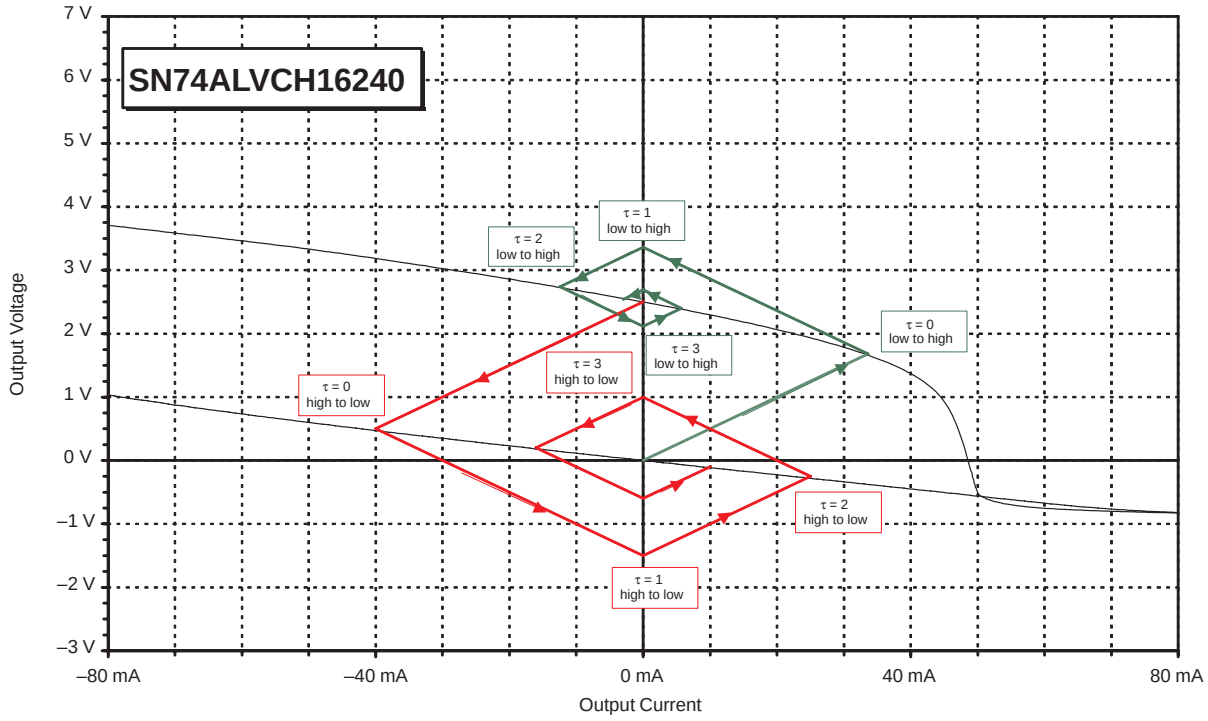
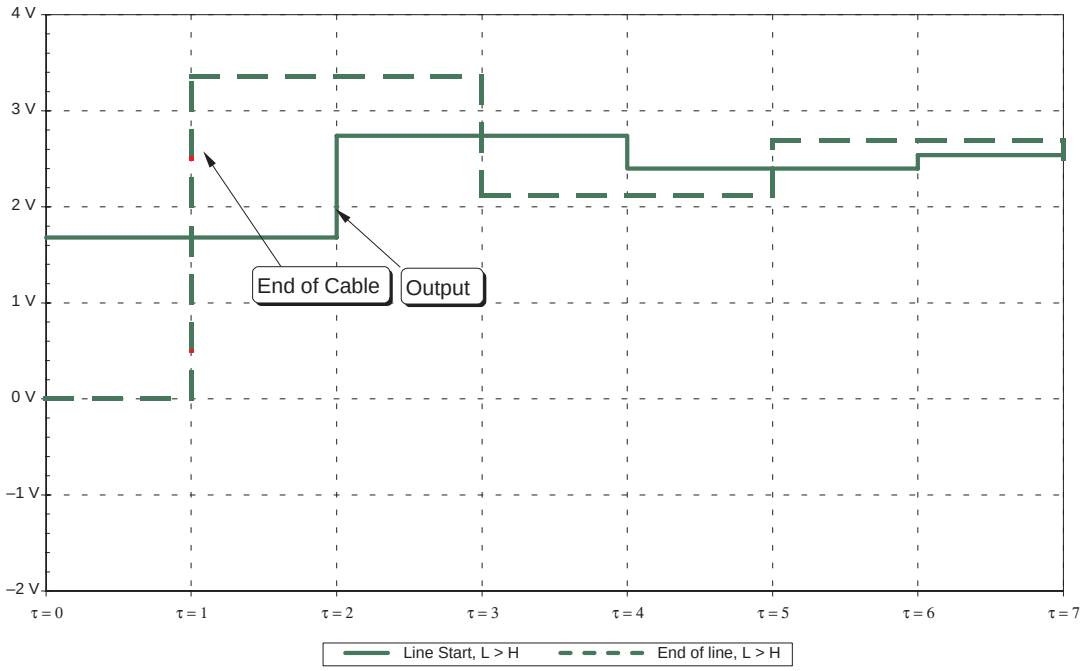


Figure 16. Bergeron Diagram for the SN74ALVCH16240



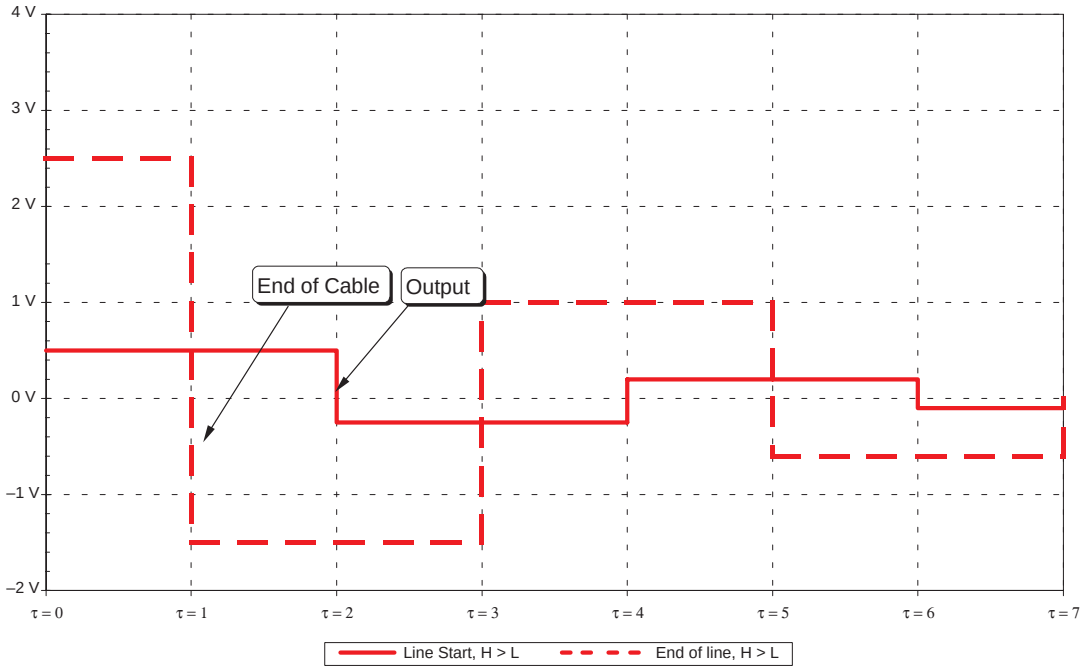


Figure 17. Diagram of Line Reflections for the SN74ALVCH16240

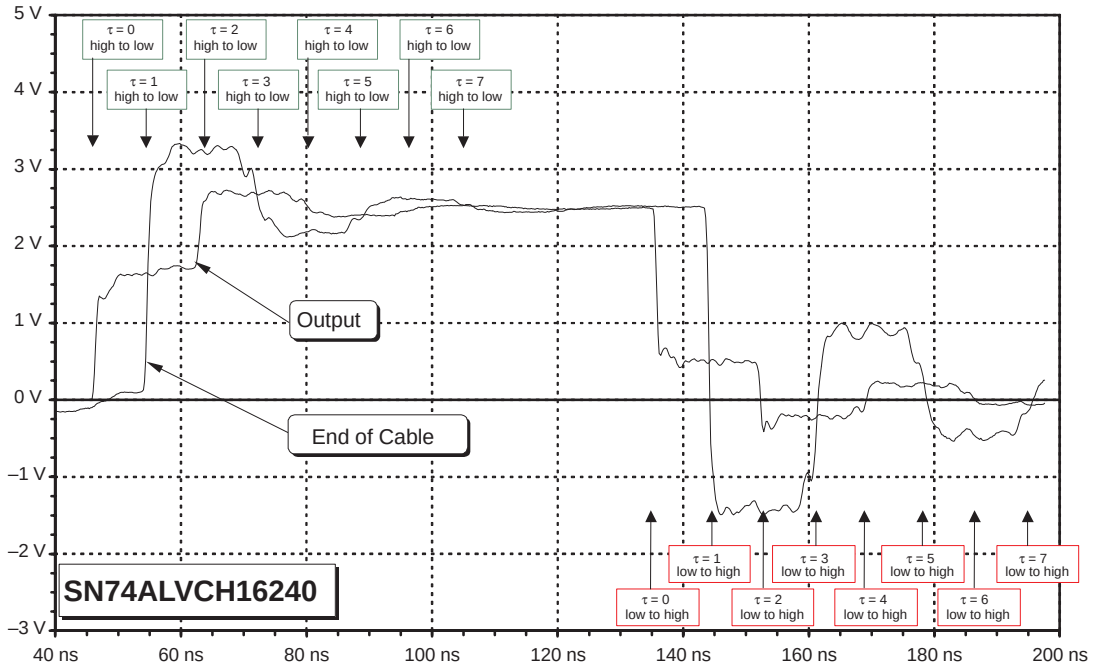


Figure 18. Signal Shape of the SN74ALVCH16240

5 Output Waveforms

Figures 19 through 25 show the measured voltage waveforms of typical output stages. Figure 15 shows the measurement setup. For these measurements, the devices under test were loaded with a 1.3-m coaxial cable having a characteristic impedance of 50 Ω; the end of the line was not connected, i.e., open circuit.

These waveforms provide good insight into the dynamic behavior of the devices. In particular, the oscillograms provide information regarding drive capability with a low-resistance load, together with an indication of the line reflections that can be expected.

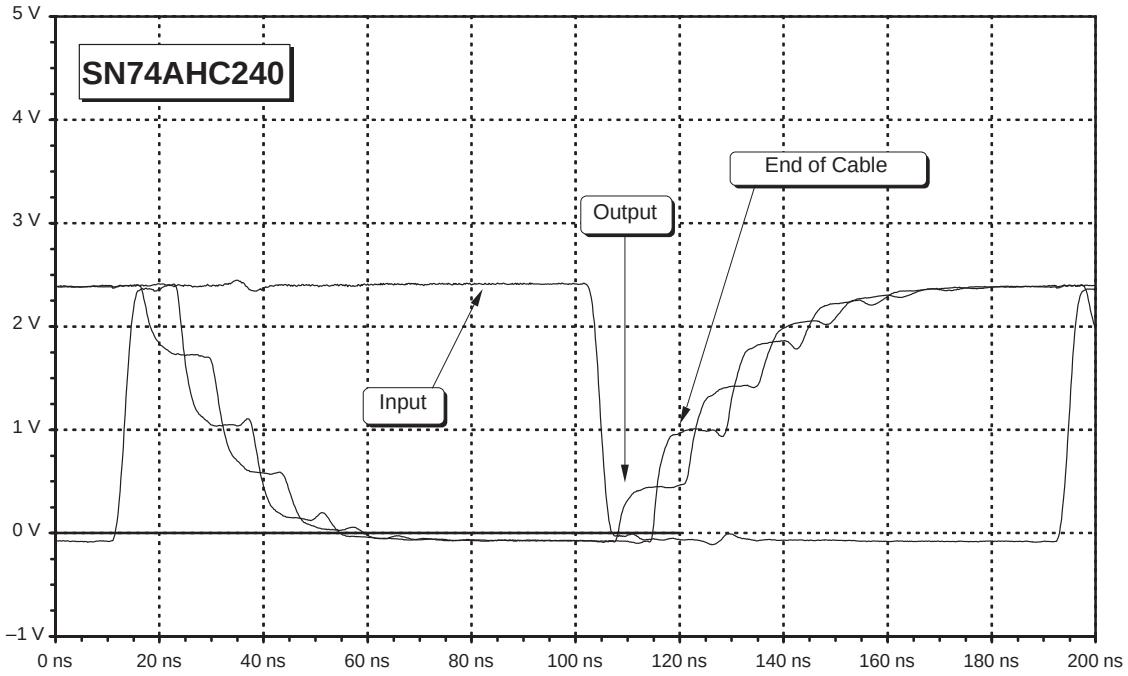


Figure 19. Output Waveforms of the SN74AHC240

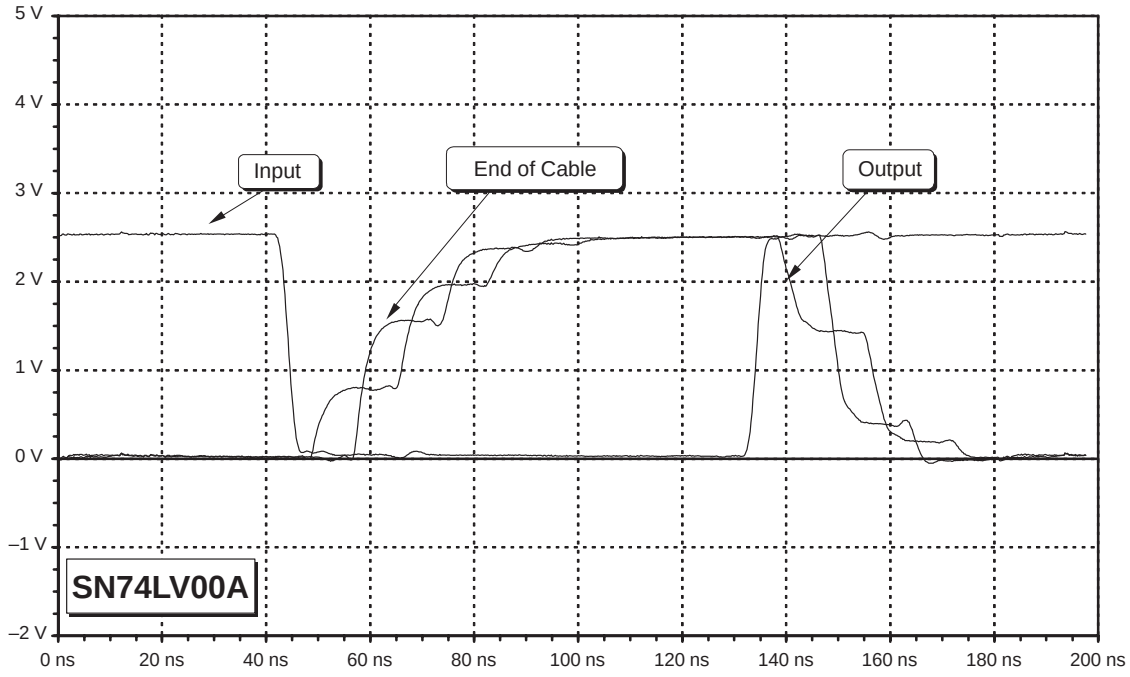


Figure 20. Output Waveforms of the SN74LV00A

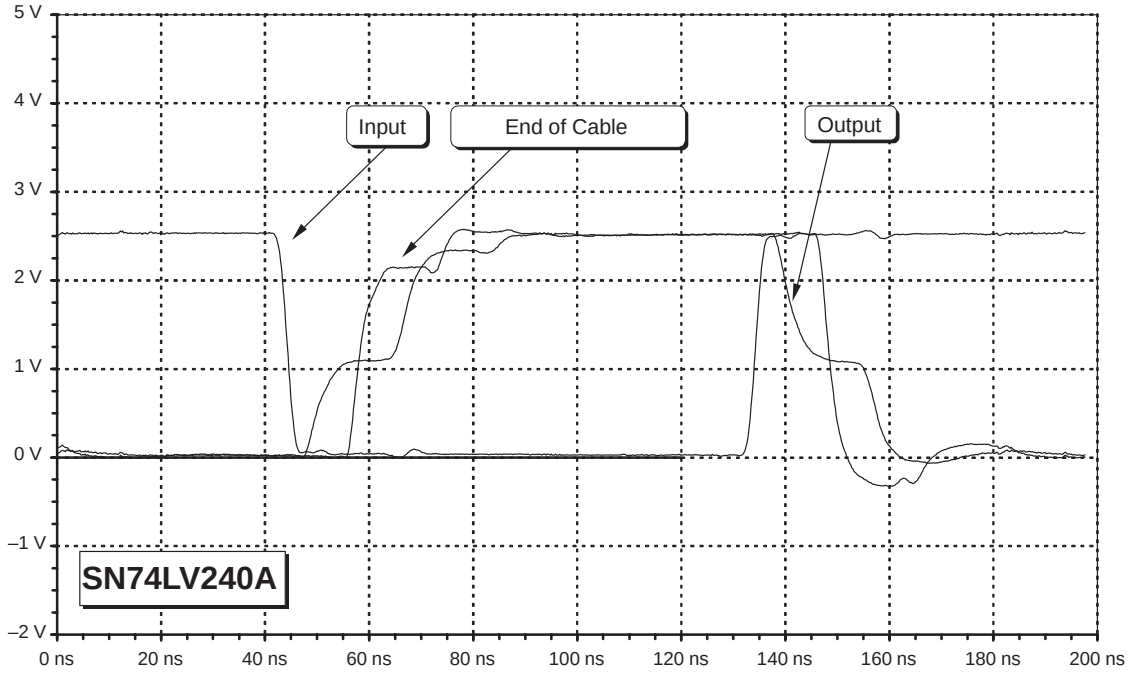


Figure 21. Output Waveforms of the SN74LV240A

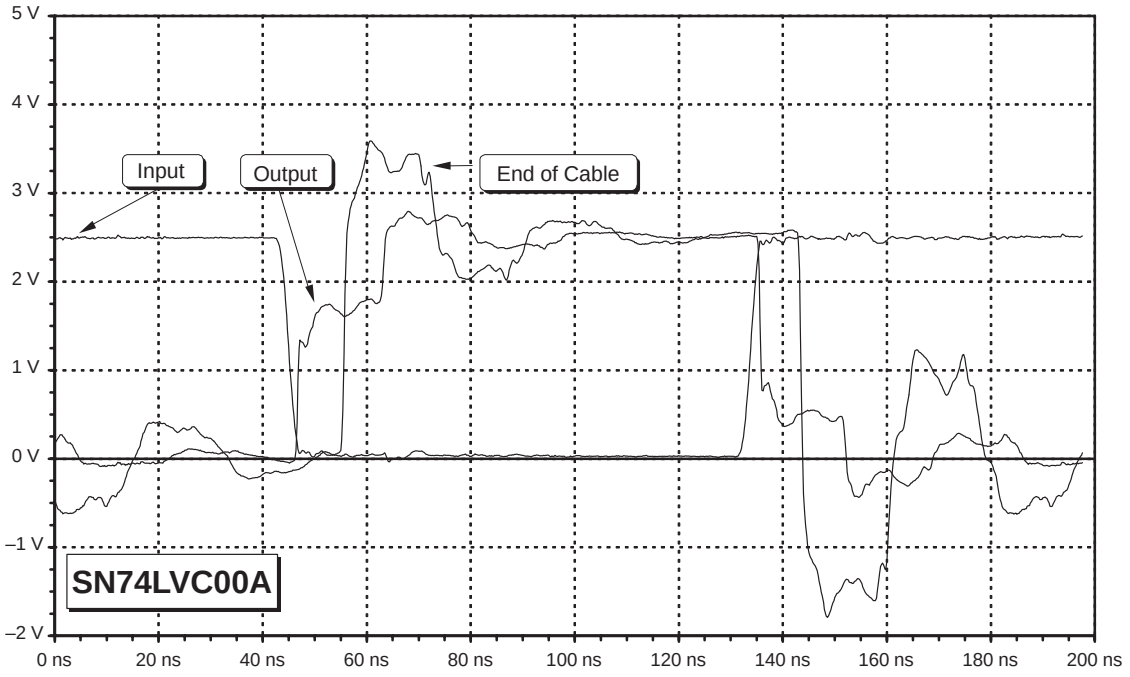


Figure 22. Output Waveforms of the SN74LVC00A

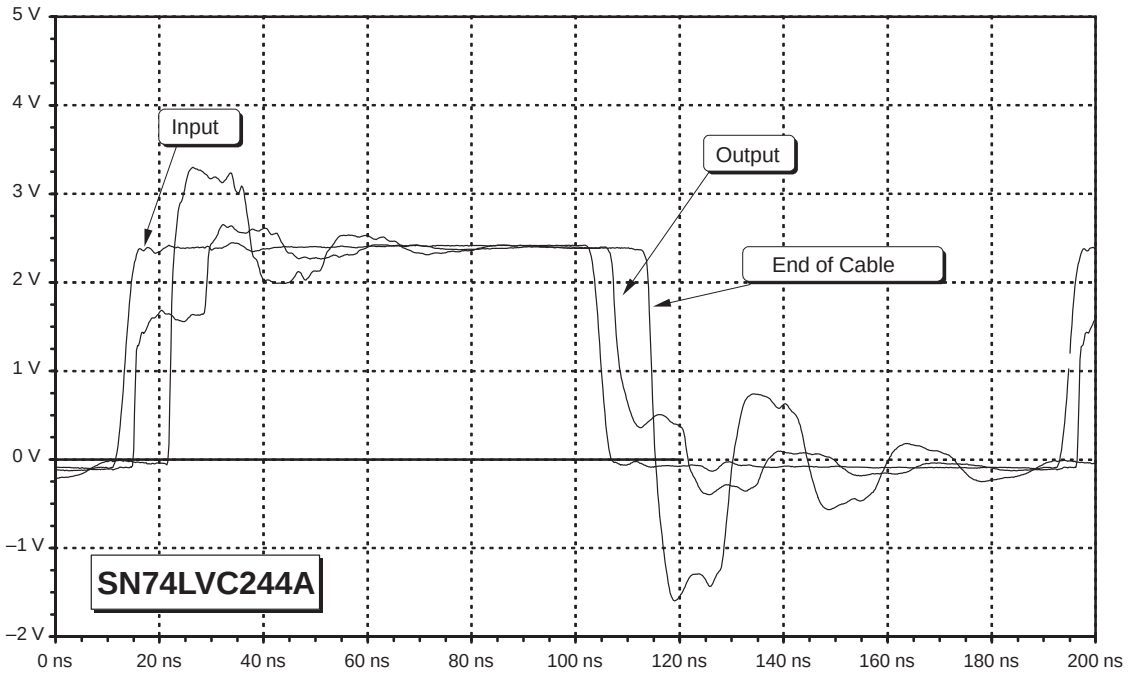


Figure 23. Output Waveforms of the SN74LVC244A

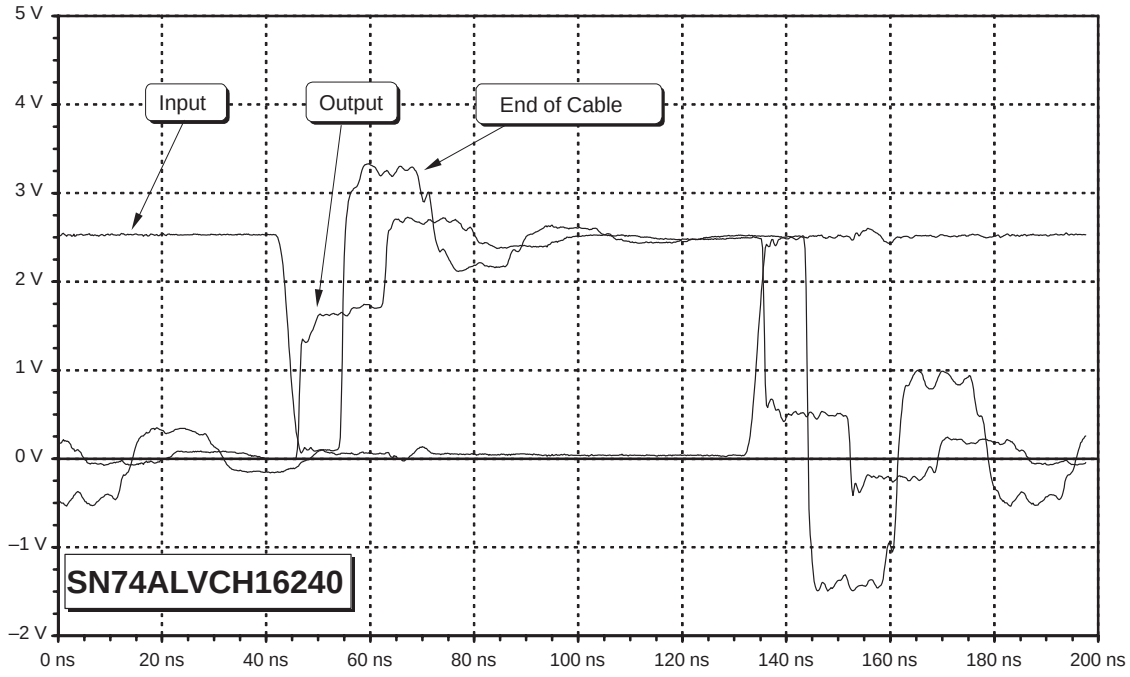


Figure 24. Output Waveforms of the SN74ALVCH16240

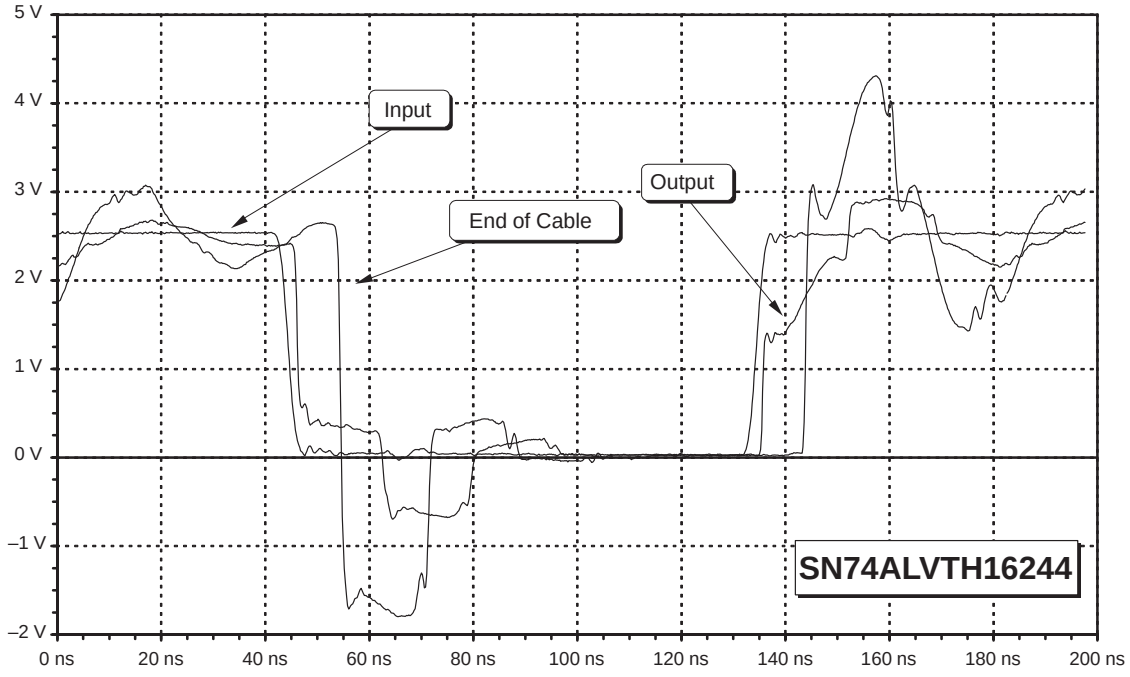


Figure 25. Output Waveforms of the SN74ALVTH16244

6 Abbreviations and Glossary

SN74ABT	Advanced BiCMOS Technology devices
SN74AC	Advanced CMOS devices
SN74AHC	Advanced High-speed CMOS devices
SN74ALS	Advanced Low-power Schottky devices
SN74AS	Advanced Schottky devices
SN74ALVC	Advanced Low-Voltage CMOS devices
SN74ALVT	Advance Low-Voltage Technology devices
SN74AVC	Advanced Very low-voltage CMOS devices
Auto3-state	During active-high state at the output, devices with auto3-state tolerate a higher voltage level at the outputs (also called overvoltage protection).
SN74BCT	BiCMOS Technology devices
BiCMOS	Combination of bipolar and CMOS process (CMOS input structure and bipolar output structure)
Bus hold	Input circuitry that holds the last valid logic state applied to it before entering a nondefined state on the bus, until a new valid logic state is driven actively.
3-/5-V tolerance	Logic devices with 5-V (3.3-V) tolerance tolerate 5-V (3.3-V) CMOS logic levels at their input and output in the high-impedance state while supplied with 2.5-V.
GND	Ground
I/O	Input/Output
SN74LS	Low-power Schottky devices
SN74LV	Low-Voltage CMOS devices, originally designed for V_{CC} = 3.3-V, also specified at 5 V
SN74LVC	Low-Voltage CMOS devices
SN74LVT	Low-Voltage Technology devices
Overvoltage protection	See auto3-state and 3-/5-V tolerance
R_L	Load resistor
SN74S	Schottky devices
Series resistor	A resistor in the output stage of a bus driver. With this resistor, the effective output impedance of the driver is shifted to about 50 Ω, making an optimum line adaptation.
SPICE	Simulation Program with Integrated Circuit Emphasis
TTL-level	Transistor-Transistor Logic level
V_{CC}	Supply voltage

7 References

7.1 Documents Published by TI

AVC Logic Technology and Application, 1998, literature number SCEA006A.

ABT Logic Advanced BiCMOS Technology, Data Book, 1998, literature number SCBD002C.

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7.2 Internet Information Sources

TI Semiconductor Home Page

http://www.ti.com/sc

TI Distributors

http://www.ti.com/sc/docs/distmenu.htm

TI Logic Home Page

http://www.ti.com/sc/docs/asl/home.htm

TI Logic Literature

http://www.ti.com/sc/docs/asl/lit/lit.htm

TI Product Information and Document Search

http://www.ti.com/sc/docs/msp/download.htm

8 Acknowledgment

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