

CCD ANALOG FRONT-END FOR DIGITAL CAMERAS

Check for Samples: [VSP2560](#), [VSP2562](#), [VSP2566](#)

FEATURES

- **CCD Signal Processing:**
 - 36-MHz Correlated Double Sampling (CDS)
- **Output Resolution:**
 - VSP2560 (10-Bit)
 - VSP2562 (12-Bit)
 - VSP2566 (16-Bit)
- **16-Bit Analog-to-Digital Conversion:**
 - 36-MHz Conversion Rate
 - No Missing Codes Ensured
- **80-dB Input-Referred SNR (at Gain = 12 dB)**
- **Programmable Black Level Clamping**
- **Programmable Gain Amp (PGA):**
 - -9 dB to +44 dB
 - -3 dB to +18 dB (Analog Front Gain)
 - -6 dB to +26 dB (Digital Gain)
- **Portable Operation:**
 - Low Voltage: 2.7 V to 3.6 V
 - Low Power: 86 mW at 3.0 V, 36 MHz
 - Low Power: 6 mW (Standby Mode)

- **Two-Channel, General-Purpose, 8-Bit DAC**

DESCRIPTION

The VSP2560/62/66 are a family of complete mixed-signal processing ICs for digital cameras that provide correlated double sampling (CDS) and analog-to-digital conversion for the output of CCD arrays. The CDS extracts the pixel video information from the CCD signal, and the analog-to-digital converter (ADC) converts the digital signal. For varying illumination conditions, a very stable gain control of -9 dB to 44 dB is provided. The gain control is linear in dB. Input signal clamping and offset correction of the input CDS are also provided.

Offset correction is performed by the optical black (OB) level calibration loop, and is held in calibrated black level clamping for an accurate black level reference. Additionally, the black level is quickly recovered after gain changes. The VSP2560/62/66 are available in LQFP-48 packages and operate from single +3 V supplies.

Table 1. FEATURE COMPARISON BY DEVICE

DEVICE	RESOLUTION (Bits)	TRANSFER CHARACTERISTICS (LSB)		OB CLAMP LOOP (LSB)		
		DNL	INL	PROGRAMMABLE RANGE	OBCLP LEVEL	OB LEVEL
VSP2560	10	±0.5	±1	16 to 78	32	2
VSP2562	12	±0.5	±2	64 to 312	128	8
VSP2566	16	±2	±32	1024 to 4992	2048	128



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
VSP2560PTR	OBSOLETE	LQFP	PT	48		TBD	Call TI	Call TI	-40 to 85	VSP2560	
VSP2562PT	OBSOLETE	LQFP	PT	48		TBD	Call TI	Call TI	-25 to 85	VSP2562	
VSP2566PT	OBSOLETE	LQFP	PT	48		TBD	Call TI	Call TI	-25 to 85	VSP2566	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

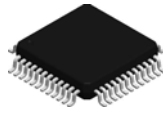
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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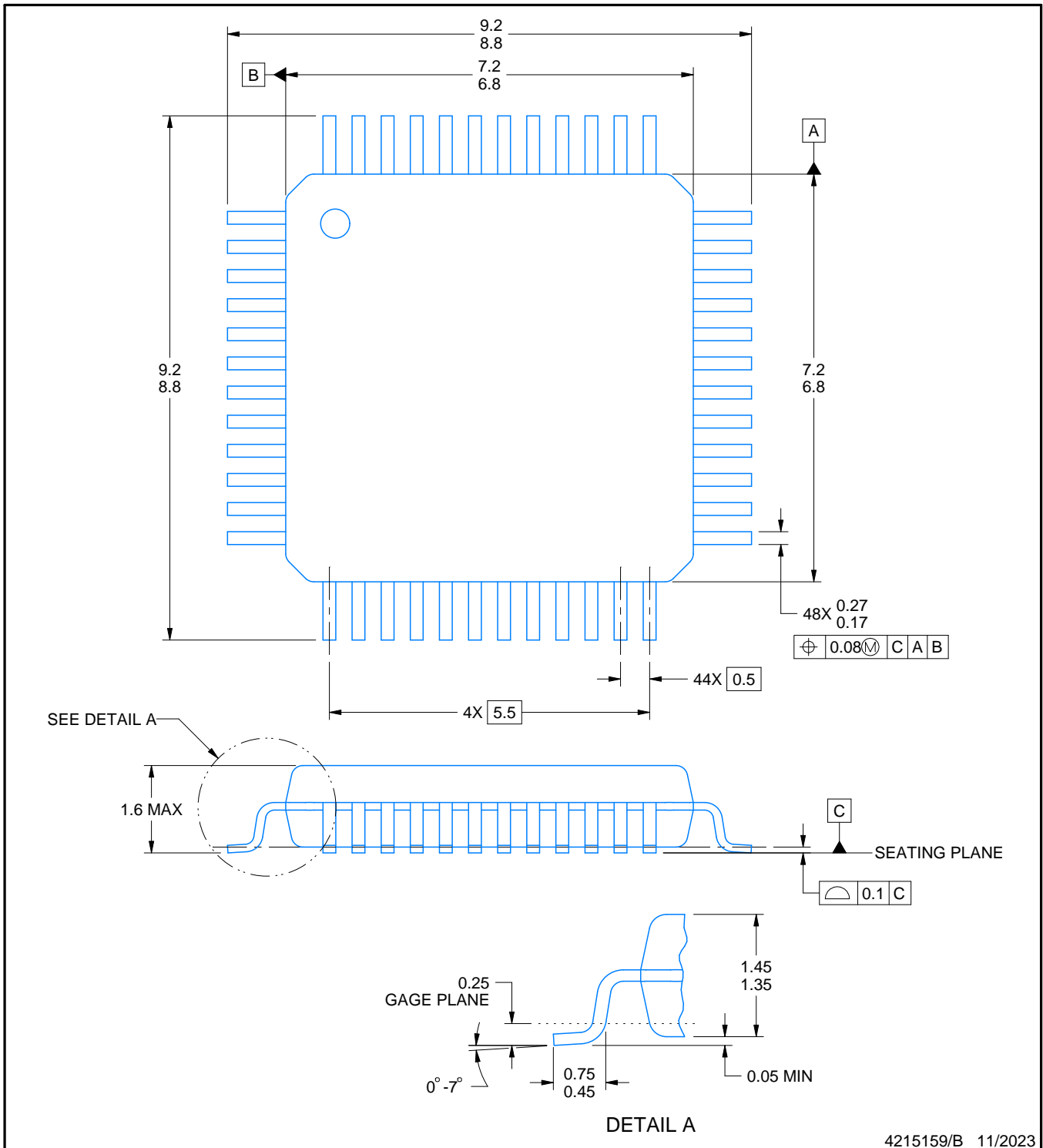
PT0048A



PACKAGE OUTLINE

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



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NOTES:

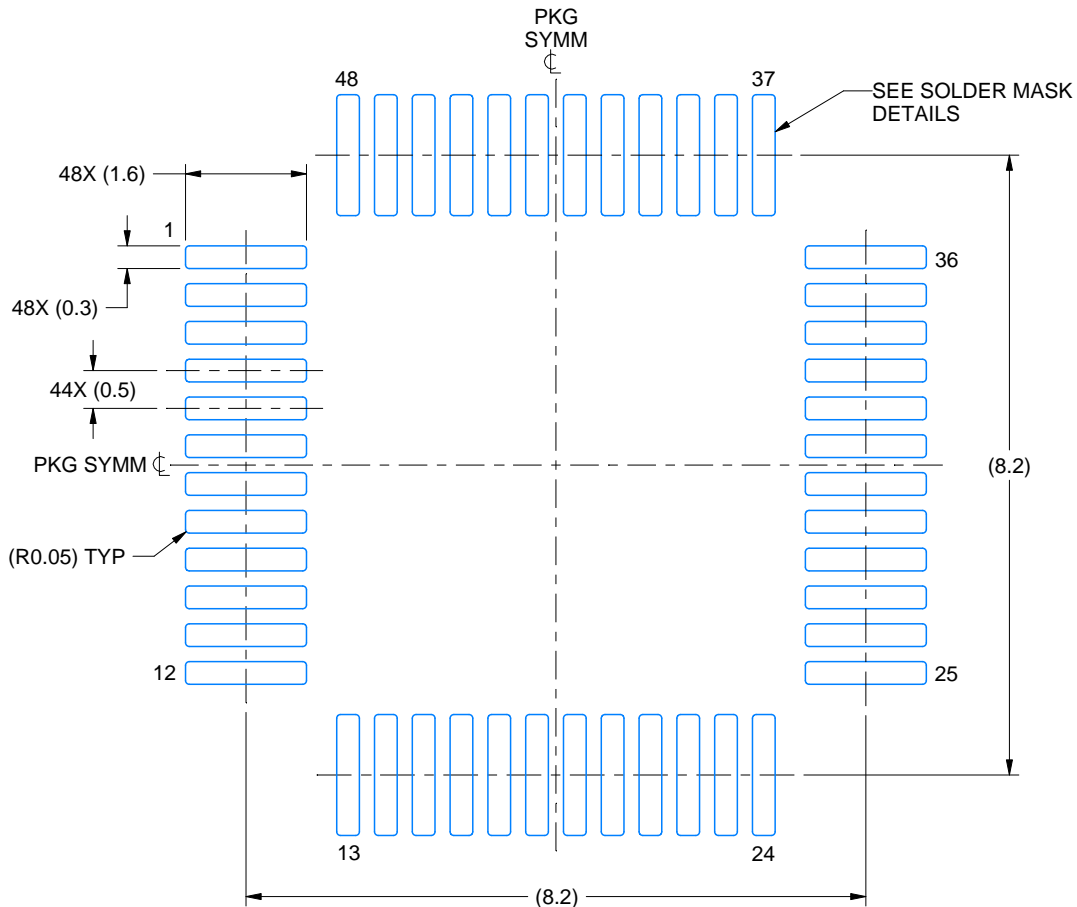
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads connected to the die pads.

EXAMPLE BOARD LAYOUT

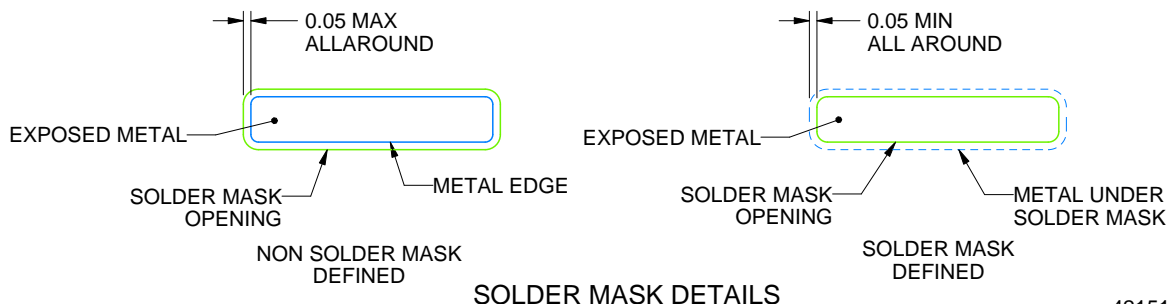
PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000



SOLDER MASK DETAILS

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NOTES: (continued)

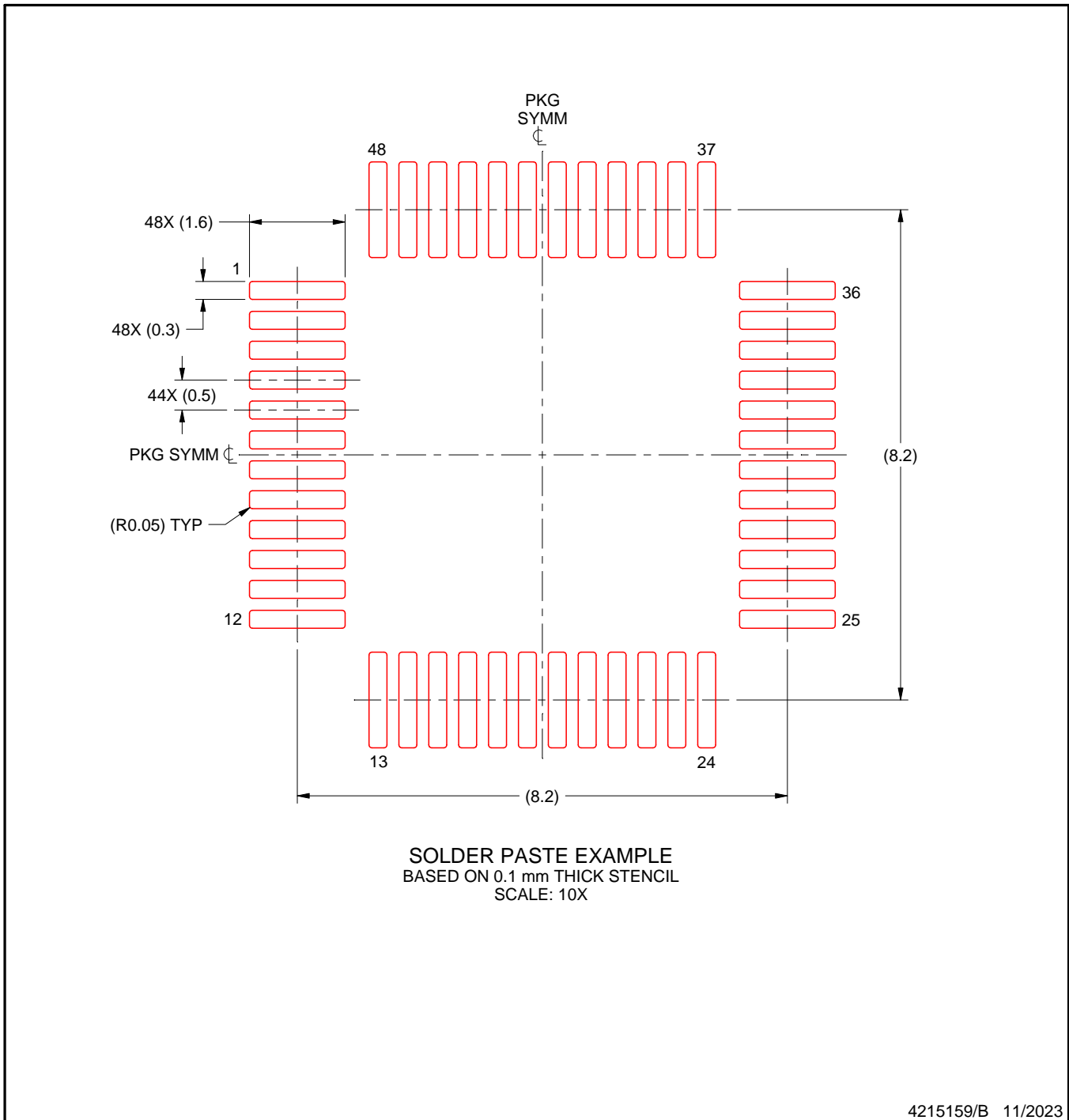
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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