



# Programmable Gamma-Voltage Generator and $V_{COM}$ Calibrator with Integrated Two-Bank Memory

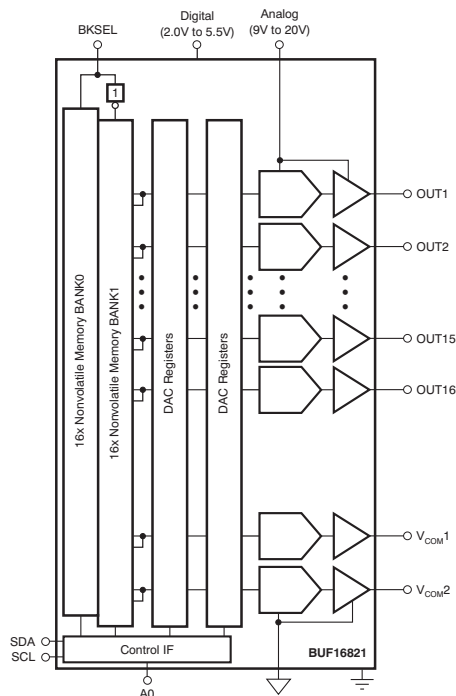
 Check for Samples: [BUF16821](#)

## FEATURES

- **10-BIT RESOLUTION**
- **16-CHANNEL P-GAMMA**
- **2-CHANNEL P- $V_{COM}$**
- **16x REWRITABLE NONVOLATILE MEMORY**
- **TWO INDEPENDENT PIN-SELECTABLE MEMORY BANKS**
- **RAIL-TO-RAIL OUTPUT**
  - 300mV Min Swing-to-Rail (10mA)
  - > 300mA Max  $I_{OUT}$
- **LOW SUPPLY CURRENT**
- **SUPPLY VOLTAGE: 9V to 20V**
- **DIGITAL SUPPLY: 2V to 5.5V**
- **I<sup>2</sup>C™ INTERFACE: Supports 400kHz and 3.4MHz**

## APPLICATIONS

- **TFT-LCD REFERENCE DRIVERS**



## DESCRIPTION

The BUF16821 offers 16 programmable gamma channels and two programmable  $V_{COM}$  channels.

The final gamma and  $V_{COM}$  values can be stored in the on-chip, nonvolatile memory. To allow for programming errors or liquid crystal display (LCD) panel rework, the BUF16821 supports up to 16 write operations to the on-chip memory.

The BUF16821 has two separate memory banks, allowing simultaneous storage of two different gamma curves to facilitate switching between gamma curves.

All gamma and  $V_{COM}$  channels offer a rail-to-rail output that typically swings to within 150mV of either supply rail with a 10mA load. All channels are programmed using an I<sup>2</sup>C interface that supports standard operations up to 400kHz and high-speed data transfers up to 3.4MHz.

The BUF16821 is manufactured using Texas Instruments' proprietary, state-of-the-art, high-voltage CMOS process. This process offers very dense logic and high supply voltage operation of up to 20V. The BUF16821 is offered in a HTSSOP-28 PowerPAD™ package, and is specified from –40°C to +85°C.

## RELATED PRODUCTS

FEATURES	PRODUCT
22-Channel Gamma Correction Buffer	<a href="#">BUF22821</a>
12-Channel Gamma Correction Buffer	<a href="#">BUF12800</a>
18-/20-Channel Programmable Buffer, 10-Bit, $V_{COM}$	<a href="#">BUF20800</a>
18-/20-Channel Programmable Buffer with Memory	<a href="#">BUF20820</a>
Programmable $V_{COM}$ Driver	<a href="#">BUF01900</a>
18V Supply, Traditional Gamma Buffers	<a href="#">BUF11704</a>
22V Supply, Traditional Gamma Buffers	<a href="#">BUF11705</a>



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**PACKAGE/ORDERING INFORMATION<sup>(1)</sup>**

PRODUCT	PACKAGE	PACKAGE DESIGNATOR	PACKAGE MARKING
BUF16821A	HTSSOP-28	PWP	BUF16821
BUF16821B	HTSSOP-28	PWP	BUF16821B

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		BUF16821	UNIT
Supply Voltage	$V_S$	+22	V
Supply Voltage	$V_{SD}$	+6	V
Digital Input Pins, SCL, SDA, AO, BKSEL: Voltage		–0.5 to +6	V
Digital Input Pins, SCL, SDA, AO, BKSEL: Current		±10	mA
Output Pins, OUT1 through OUT16, $V_{COM1}$ and $V_{COM2}$ <sup>(2)</sup>		(V–) – 0.5 to (V+) + 0.5	V
Output Short-Circuit <sup>(3)</sup>		Continuous	
Ambient Operating Temperature		–40 to +95	°C
Ambient Storage Temperature		–65 to +150	°C
Junction Temperature		$T_J$ +125	°C
ESD Rating	Human Body Model (HBM)	3000	V
	Charged Device Model (CDM)	1000	V
	Machine Model (MM)	200	V

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

(2) See the [Output Protection](#) section.

(3) Short-circuit to ground, one amplifier per package.

## ELECTRICAL CHARACTERISTICS

**Boldface** limits apply over the specified temperature range,  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .

At  $T_A = +25^{\circ}\text{C}$ ,  $V_S = +18\text{V}$ ,  $V_{SD} = +2\text{V}$ ,  $R_L = 1.5\text{k}\Omega$  connected to ground, and  $C_L = 200\text{pF}$ , unless otherwise noted.

PARAMETER	CONDITIONS	BUF16821			UNIT
		MIN	TYP	MAX	
<b>ANALOG GAMMA BUFFER CHANNELS</b>					
Reset Value	Code 512		9		V
OUT 1–16 Output Swing: High	Code = 1023, Sourcing 10mA	17.7	17.85		V
OUT 1–16 Output Swing: Low	Code = 0, Sinking 10mA		0.07	0.3	V
$V_{COM1, 2}$ Output Swing: High					
BUF16821A	Code = 1023, Sourcing 100mA	13	16.2		V
BUF16821B <sup>(1)</sup>	Code = 511, Sourcing 100mA		8.96		V
$V_{COM1, 2}$ Output Swing: Low					
BUF16821A	Code = 0, Sinking 100mA		0.6	2	V
BUF16821B <sup>(1)</sup>	Code = 384, Sinking 100mA		6.75		V
Continuous Output Current	Note <sup>(2)</sup>		30		mA
Output Accuracy			±20	±50	mV
<b>vs Temperature</b>	Code 512		±25		μV/°C
Integral Nonlinearity	INL		0.3		LSB
Differential Nonlinearity	DNL		0.3		LSB
Load Regulation, 10mA	REG	Code 512 or $V_{CC}/2$ , $I_{OUT} = +5\text{mA}$ to $-5\text{mA}$ Step	0.5	1.5	mV/mA
<b>OTP MEMORY</b>					
Number of OTP Write Cycles				16	Cycles
Memory Retention			100		Years
<b>ANALOG POWER SUPPLY</b>					
Operating Range		9		20	V
Total Analog Supply Current	$I_S$	Outputs at Reset Values, No Load	12	14	mA
<b>Over Temperature</b>				<b>18</b>	<b>mA</b>
<b>DIGITAL</b>					
Logic 1 Input Voltage	$V_{IH}$	$0.7 \times V_{SD}$			V
Logic 0 Input Voltage	$V_{IL}$			$0.3 \times V_{SD}$	V
Logic 0 Output Voltage	$V_{OL}$	$I_{SINK} = 3\text{mA}$	0.15	0.4	V
Input Leakage			±0.01	±10	μA
Clock Frequency	$f_{CLK}$	Standard/Fast Mode		400	kHz
		High-Speed Mode		3.4	MHz
<b>DIGITAL POWER SUPPLY</b>					
Operating Range	$V_{SD}$		2.0	5.5	V
Digital Supply Current <sup>(2)</sup>	$I_{SD}$	Outputs at Reset Values, No Load, Two-Wire Bus Inactive		115	μA
<b>Over Temperature</b>				<b>115</b>	<b>μA</b>
<b>TEMPERATURE RANGE</b>					
Specified Range			-40	+85	°C
Operating Range		Junction Temperature < +125°C	-40	+95	°C
Storage Range			-65	+150	°C
Thermal Resistance <sup>(2)</sup>	$\theta_{JA}$	See Note <sup>(3)</sup>			°C/W
HTSSOP-28			40		°C/W

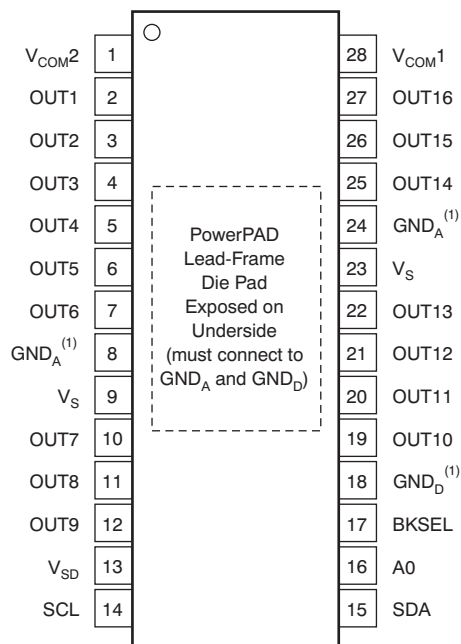
(1) BUF16821B output swing is limited internally. Bits 9, 8, and 7 are fixed at '011'.

(2) Observe maximum power dissipation.

(3) Thermal pad attached to printed circuit board (PCB), 0lfm airflow, and 76mm × 76mm copper area.

### PIN CONFIGURATION

**PWP PACKAGE  
HTSSOP-28  
(TOP VIEW)**



NOTE: (1) GND<sub>A</sub> and GND<sub>D</sub> must be connected together.

**PIN DESCRIPTIONS**

<b>PIN #</b>	<b>NAME</b>	<b>DESCRIPTION</b>
1	V <sub>COM2</sub>	V <sub>COM</sub> channel 2
2	OUT1	DAC output 1
3	OUT2	DAC output 2
4	OUT3	DAC output 3
5	OUT4	DAC output 4
6	OUT5	DAC output 5
7	OUT6	DAC output 6
8	GND <sub>A</sub>	Analog ground; must be connected to digital ground (GND <sub>D</sub> ).
9	V <sub>S</sub>	V <sub>S</sub> connected to analog supply
10	OUT7	DAC output 7
11	OUT8	DAC output 8
12	OUT9	DAC output 9
13	V <sub>SD</sub>	Digital supply; connect to logic supply
14	SCL	Serial clock input; open-drain, connect to pull-up resistor.
15	SDA	Serial data I/O; open-drain, connect to pull-up resistor.
16	A0	A0 address pin for I <sup>2</sup> C address; connect to either logic 1 or logic 0. See <a href="#">Table 1</a> .
17	BKSEL	Selects memory bank 0 or 1; connect to either logic 1 to select bank 1 or logic 0 to select bank 0.
18	GND <sub>D</sub>	Digital ground; must be connected to analog ground at the BUF16821.
19	OUT10	DAC output 10
20	OUT11	DAC output 11
21	OUT12	DAC output 12
22	OUT13	DAC output 13
23	V <sub>S</sub>	V <sub>S</sub> connected to analog supply
24	GND <sub>A</sub>	Analog ground; must be connected to digital ground (GND <sub>D</sub> ).
25	OUT14	DAC output 14
26	OUT15	DAC output 15
27	OUT16	DAC output 16
28	V <sub>COM1</sub>	V <sub>COM</sub> channel 1

### TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = +18\text{V}$ ,  $V_{SD} = +2\text{V}$ ,  $R_L = 1.5\text{k}\Omega$  connected to ground, and  $C_L = 200\text{pF}$ , unless otherwise noted.

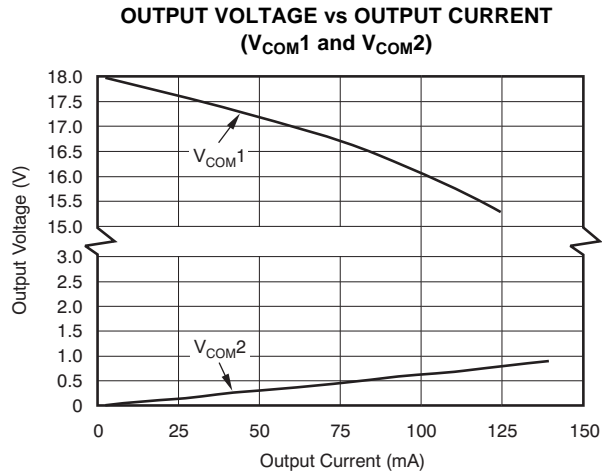


Figure 1.

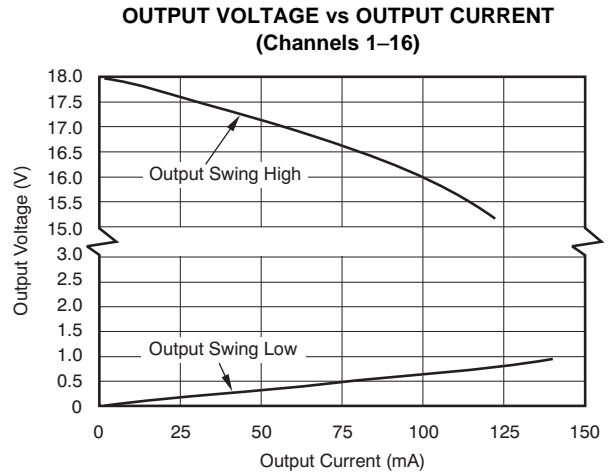


Figure 2.

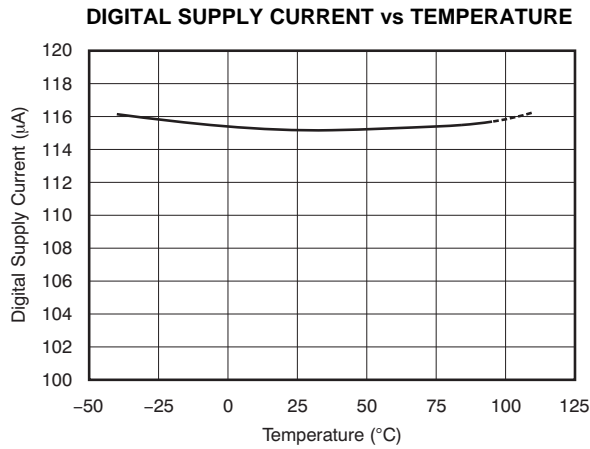


Figure 3.

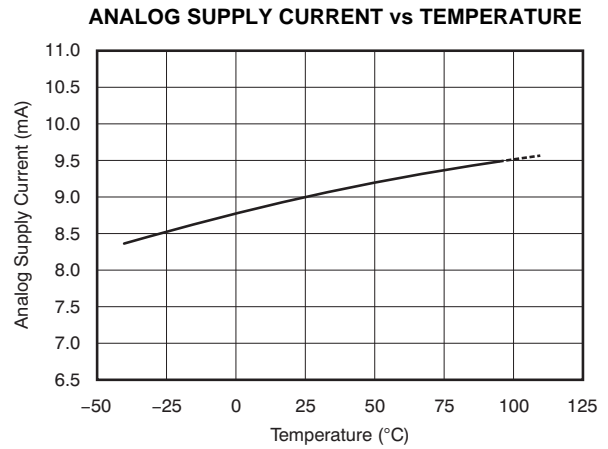


Figure 4.

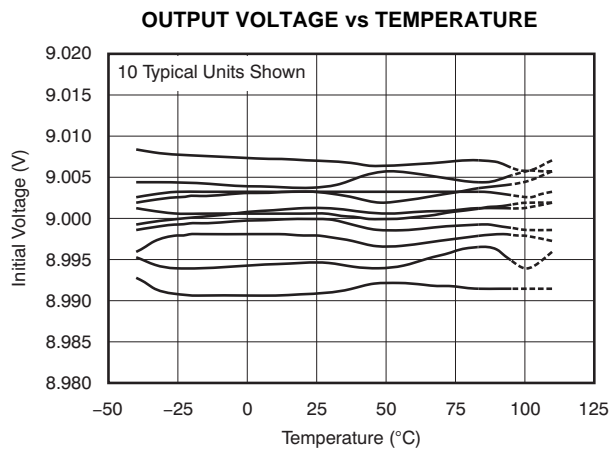


Figure 5.

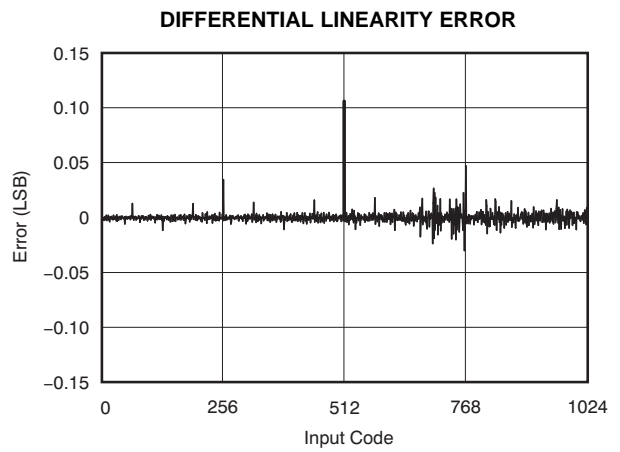
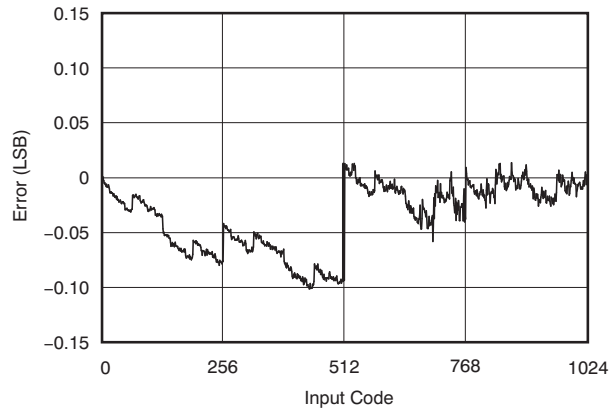


Figure 6.

**TYPICAL CHARACTERISTICS (continued)**

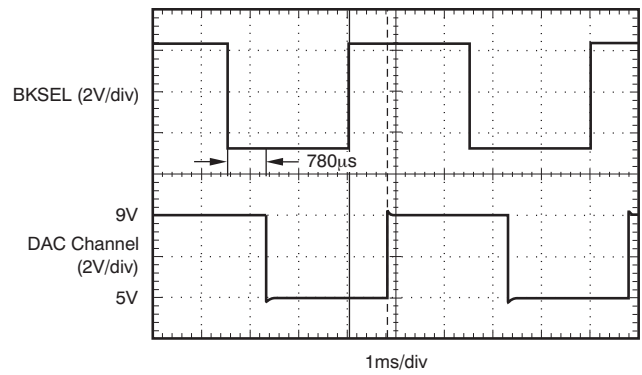
At  $T_A = +25^\circ\text{C}$ ,  $V_S = +18\text{V}$ ,  $V_{SD} = +2\text{V}$ ,  $R_L = 1.5\text{k}\Omega$  connected to ground, and  $C_L = 200\text{pF}$ , unless otherwise noted.

**INTEGRAL LINEARITY ERROR**



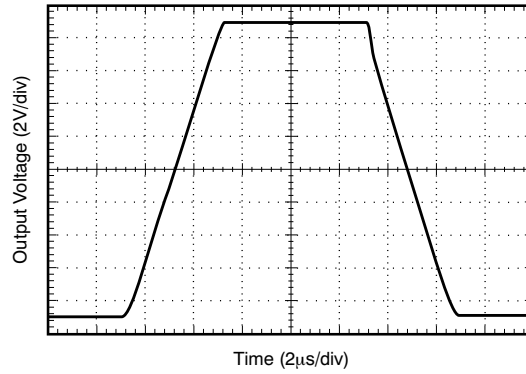
**Figure 7.**

**BKSEL SWITCHING TIME DELAY**



**Figure 8.**

**LARGE-SIGNAL STEP RESPONSE**



**Figure 9.**

## APPLICATION INFORMATION

### GENERAL

The BUF16821 programmable voltage reference allows fast and easy adjustment of 16 programmable gamma reference outputs and two  $V_{COM}$  outputs, each with 10-bit resolution. The BUF16821 is programmed through a high-speed, I<sup>2</sup>C interface. The final gamma and  $V_{COM}$  values can be stored in the onboard, nonvolatile memory. To allow for programming errors or liquid crystal display (LCD) panel rework, the BUF16821 supports up to 16 write operations to the onboard memory. The BUF16821 has two separate memory banks, allowing simultaneous storage of two different gamma curves to facilitate dynamic switching between gamma curves.

The BUF16821 can be powered using an analog supply voltage from 9V to 20V, and a digital supply from 2V to 5.5V. The digital supply must be applied before the analog supply to avoid excessive current and power consumption, or possibly even damage to the device if left connected only to the analog supply for extended periods of time. [Figure 10](#) illustrates a typical configuration of the BUF16821.

### TWO-WIRE BUS OVERVIEW

The BUF16821 communicates over an industry-standard, two-wire interface to receive data in slave mode. This standard uses a two-wire, open-drain interface that supports multiple devices on a single bus. Bus lines are driven to a logic low level only. The device that initiates the communication is called a *master*, and the devices controlled by the master are *slaves*. The master generates the serial clock on the clock signal line (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling the data signal line (SDA) from a HIGH to a LOW logic level while SCL is HIGH.

All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and eight bits of data are sent, followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH is interpreted as a START or STOP condition.

Once all data have been transferred, the master generates a STOP condition, indicated by pulling SDA from LOW to HIGH while SCL is HIGH. The BUF16821 can act only as a slave device; therefore, it never drives SCL. SCL is an input only for the BUF16821.

### ADDRESSING THE BUF16821

The address of the BUF16821 is 111010x, where x is the state of the A0 pin. When the A0 pin is LOW, the device acknowledges on address 74h (1110100). If the A0 pin is HIGH, the device acknowledges on address 75h (1110101). [Table 1](#) shows the A0 pin settings and BUF16821 address options.

Other valid addresses are possible through a simple mask change. Contact your TI representative for information.

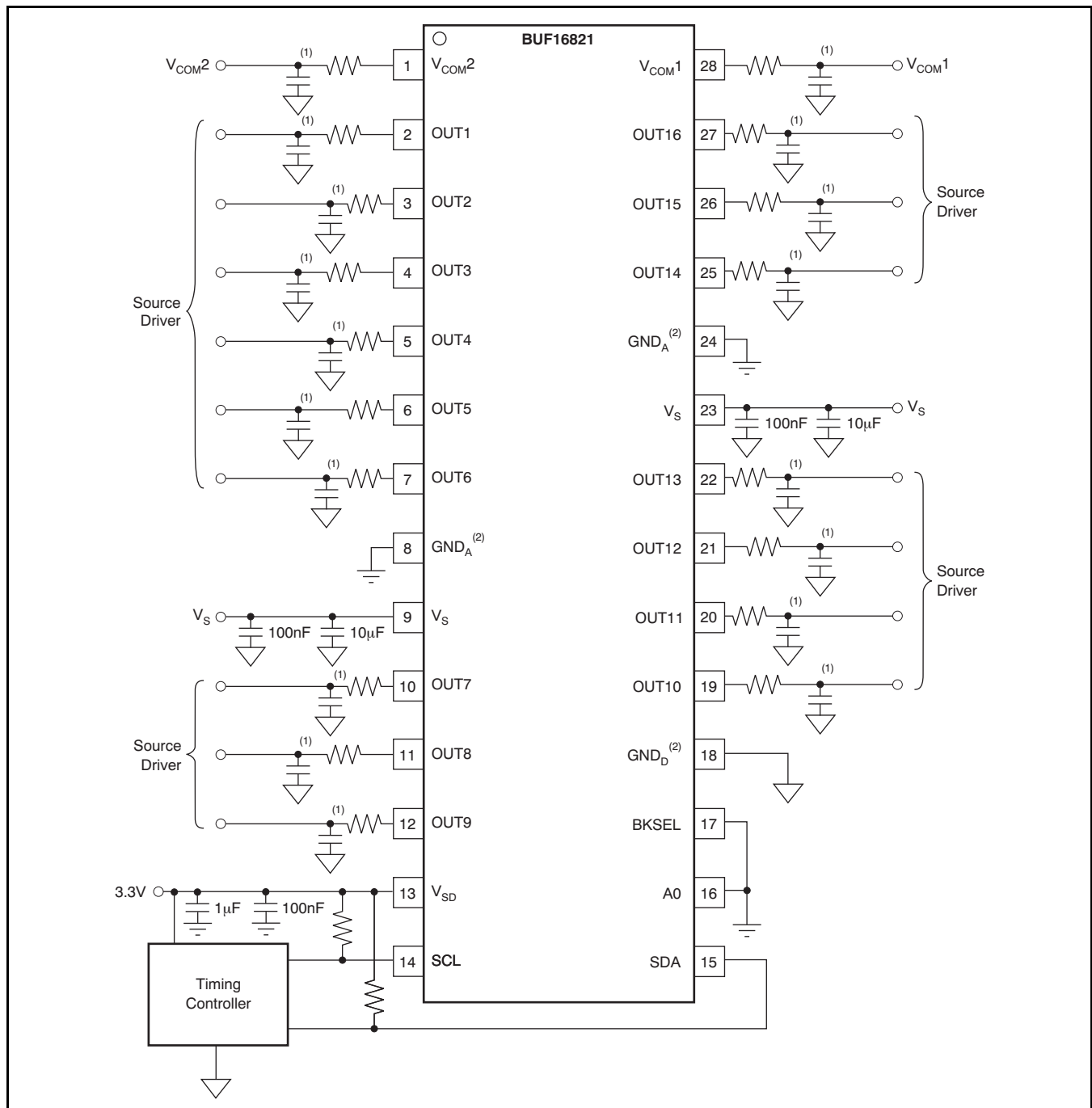
**Table 1. Quick-Reference of BUF16821 Addresses**

DEVICE/COMPONENT	ADDRESS
<b>BUF16821 Address</b>	
A0 pin is LOW (device acknowledges on address 74h)	1110100
A0 pin is HIGH (device acknowledges on address 75h)	1110101

**Table 2. Quick-Reference of Command Codes**

COMMAND	CODE
General-Call Reset	Address byte of 00h followed by a data byte of 06h.
High-Speed Mode	00001xxx, with SCL ≤ 400kHz; where xxx are bits unique to the Hs-capable master. This byte is called the Hs master code.





- (1) RC combination optional; see the [Output Protection](#) section.
- (2) GND<sub>A</sub> and GND<sub>D</sub> must be connected together.

**Figure 10. Typical Application Configuration**

## DATA RATES

The two-wire bus operates in one of three speed modes:

- Standard: allows a clock frequency of up to 100kHz;
- Fast: allows a clock frequency of up to 400kHz; and
- High-speed mode (also called Hs mode): allows a clock frequency of up to 3.4MHz.

The BUF16821 is fully compatible with all three modes. No special action is required to use the device in Standard or Fast modes, but High-speed mode must be activated. To activate High-speed mode, send a special address byte of 00001 xxx, with  $SCL \leq 400\text{kHz}$ , following the START condition; where xxx are bits unique to the Hs-capable master, which can be any value. This byte is called the Hs master code. [Table 2](#) provides a reference for the High-speed mode command code. (Note that this configuration is different from normal address bytes—the low bit does not indicate read/write status.) The BUF16821 responds to the High-speed command regardless of the value of these last three bits. The BUF16821 does not acknowledge this byte; the communication protocol prohibits acknowledgment of the Hs master code. Upon receiving a master code, the BUF16821 switches on its Hs mode filters, and communicates at up to 3.4MHz. Additional high-speed transfers may be initiated without resending the Hs mode byte by generating a repeat START without a STOP. The BUF16821 switches out of Hs mode with the next STOP condition.

## GENERAL-CALL RESET AND POWER-UP

The BUF16821 responds to a General-Call Reset, which is an address byte of 00h (0000 0000) followed by a data byte of 06h (0000 0110). The BUF16821 acknowledges both bytes. [Table 2](#) provides a reference for the General-Call Reset command code. Upon receiving a General-Call Reset, the BUF16821 performs a full internal reset, as though it had been powered off and then on. It always acknowledges the General-Call address byte of 00h (0000 0000), but does not acknowledge any General-Call data bytes other than 06h (0000 0110).

When the BUF16821 powers up, it automatically performs a reset. As part of the reset, the BUF16821 is configured for all outputs to change to the last programmed nonvolatile memory values, or 1000000000 if the nonvolatile memory values have not been programmed.

## OUTPUT VOLTAGE

Buffer output values are determined by the analog supply voltage ( $V_S$ ) and the decimal value of the binary input code used to program that buffer. The value is calculated using [Equation 1](#):

$$V_{OUT} = V_S \times \left( \frac{CODE_{10}}{1024} \right) \quad (1)$$

The BUF16821 outputs are capable of a full-scale voltage output change in typically 5 $\mu\text{s}$ ; no intermediate steps are required.

## UPDATING THE DAC OUTPUT VOLTAGES

Because the BUF16821 features a double-buffered register structure, updating the digital-to-analog converter (DAC) and/or the  $V_{COM}$  register is not the same as updating the DAC and/or  $V_{COM}$  output voltage. There are two methods for updating the DAC/ $V_{COM}$  output voltages.

**Method 1:** Method 1 is used when it is desirable to have the DAC/ $V_{COM}$  output voltage change immediately after writing to a DAC register. For each write transaction, the master sets data bit 15 to a '1'. The DAC/ $V_{COM}$  output voltage update occurs after receiving the 16th data bit for the currently-written register.

**Method 2:** Method 2 is used when it is desirable to have all DAC/ $V_{COM}$  output voltages change at the same time. First, the master writes to the desired DAC/ $V_{COM}$  channels with data bit 15 a '0'. Then, when writing the last desired DAC/ $V_{COM}$  channel, the master sets data bit 15 to a '1'. All DAC/ $V_{COM}$  channels are updated at the same time after receiving the 16th data bit.

## NONVOLATILE MEMORY

### BKSEL Pin

The BUF16821 has 16x rewrite capability of the nonvolatile memory. Additionally, the BUF16821 has the ability to store two distinct gamma curves in two different nonvolatile memory banks, each of which has 16x rewrite capability. One of the two available banks is selected using the external input pin, BKSEL. When this pin is low, BANK0 is selected; when this pin is high, BANK1 is selected.

When the BKSEL pin changes state, the BUF16821 acquires the last programmed DAC/ $V_{COM}$  values from the nonvolatile memory associated with this newly chosen bank. At power-up, the state of the BKSEL pin determines which memory bank is selected.

The I<sup>2</sup>C master also has the ability to update (acquire) the DAC registers with the last programmed nonvolatile memory values using software control. The bank to be acquired depends on the state of BKSEL.

### General Acquire Command

A general acquire command is used to update all registers and DAC/ $V_{COM}$  outputs to the last programmed values stored in nonvolatile memory. A single-channel acquire command updates only the register and DAC/ $V_{COM}$  output of the DAC/ $V_{COM}$  corresponding to the DAC/ $V_{COM}$  address used in the single-channel acquire command.

These are the steps of the sequence to initiate a general channel acquire:

1. Be sure BKSEL is in its desired state and has been stable for at least 1ms.
2. Send a START condition on the bus.
3. Send the appropriate device address (based on A0) and the read/write bit = LOW. The BUF16821 acknowledges this byte.
4. Send a DAC/ $V_{COM}$  pointer address byte. Set bit D7 = 1 and D6 = 0. Bits D5–D0 are any valid DAC/ $V_{COM}$  address. Although the BUF16821 acknowledges 000000 through 010111, it stores and returns data only from these addresses:
  - 000000 through 001111
  - 010010 and 010011
 It returns 0000 for reads from 010000 and 010001, and 010100 through 010111. See [Table 4](#) for valid DAC/ $V_{COM}$  addresses.
5. Send a STOP condition on the bus.

Approximately 750 $\mu$ s ( $\pm$ 80 $\mu$ s) after issuing this command, all DAC/ $V_{COM}$  registers and DAC/ $V_{COM}$  output voltages change to the respective, appropriate nonvolatile memory values.

### Single-Channel Acquire Command

These are the steps to initiate a single-channel acquire:

1. Be sure BKSEL is in its desired state and has been stable for at least 1ms.
2. Send a START condition on the bus.
3. Send the device address (based on A0) and read/write bit = LOW. The BUF16821 acknowledges this byte.
4. Send a DAC/ $V_{COM}$  pointer address byte using the DAC/ $V_{COM}$  address corresponding to the output and register to update with the OTP memory value. Set bit D7 = 0 and D6 = 1. Bits D5–D0 are the DAC/ $V_{COM}$  address. Although the BUF16821 acknowledges 000000 through 010111, it stores and returns data only from these addresses:
  - 000000 through 001111
  - 010010 and 010011
 It returns 0000 reads from 010000 and 010001, and 010100 through 010111. See [Table 4](#) for valid DAC/ $V_{COM}$  addresses.
5. Send a STOP condition on the bus.

Approximately 36 $\mu$ s ( $\pm$ 4 $\mu$ s) after issuing this command, the specified DAC/ $V_{COM}$  register and DAC/ $V_{COM}$  output voltage change to the appropriate OTP memory value.

### MaxBank

The BUF16821 can provide the user with the number of times the nonvolatile memory of a particular DAC/ $V_{COM}$  channel nonvolatile memory has been written to for the current memory bank. This information is provided by reading the register at pointer address 111111.

There are two ways to update the MaxBank register:

1. After initiating a single acquire command, the BUF16821 updates the MaxBank register with a code corresponding to how many times that particular channel memory has been written to.
2. Following a general acquire command, the BUF16821 updates the MaxBank register with a code corresponding to the maximum number of times the most used channel (OUT1–16 and  $V_{COM}$ S) has been written to.

MaxBank is a read-only register and is only updated by performing a general- or single-channel acquire.

Table 3 shows the relationship between the number of times the nonvolatile memory has been programmed and the corresponding state of the MaxBank Register.

**Table 3. MaxBank Details**

NUMBER OF TIMES WRITTEN TO	RETURNS CODE
0	0000
1	0000
2	0001
3	0010
4	0011
5	0100
6	0101
7	0110
8	0111
9	1000
10	1001
11	1010
12	1011
13	1100
14	1101
15	1110
16	1111

**Parity Error Correction**

The BUF16821 provides single-bit parity error correction for data stored in the nonvolatile memory to provide increased reliability of the nonvolatile memory. If a single bit of nonvolatile memory for a channel fails, the BUF16821 corrects for it and updates the appropriate DAC with the intended value when its memory is acquired.

If more than one bit of nonvolatile memory for a channel fails, the BUF16821 does not correct for it, and updates the appropriate DAC/V<sub>COM</sub> with the default value of 100000000.

**DIE\_ID AND DIE\_REV REGISTERS**

The user can verify the presence of the BUF16821 in the system by reading from address 11101. When read at this address, the BUF16821A returns 0101100100100111 and the BUF16821B returns 0101100100100100.

The user can also determine the die revision of the BUF16821 by reading from register 11100. BUF16821 returns 0000000000000000 when a RevA die is present. RevB would be designated by 0000000000000001 and so on.

**READ/WRITE OPERATIONS**

Read and write operations can be done for a single DAC/V<sub>COM</sub> or for multiple DACs/V<sub>COMS</sub>. Writing to a DAC/V<sub>COM</sub> register differs from writing to the nonvolatile memory. Bits D15–D14 of the most significant byte of data determines if data are written to the DAC/V<sub>COM</sub> register or the nonvolatile memory.

**Read/Write: DAC/V<sub>COM</sub> Register (volatile memory)**

The BUF16821 is able to read from a single DAC/V<sub>COM</sub>, or multiple DACs/V<sub>COMS</sub>, or write to the register of a single DAC/V<sub>COM</sub>, or multiple DACs/V<sub>COMS</sub> in a single communication transaction. DAC pointer addresses begin with 000000 (which corresponds to OUT1) through 001111 (which corresponds to OUT16). Addresses 010010 and 010011 are V<sub>COM1</sub> and V<sub>COM2</sub>, respectively.

Write commands are performed by setting the read/write bit LOW. Setting the read/write bit HIGH performs a read transaction.

**Writing: DAC/V<sub>COM</sub> Register (Volatile Memory)**

To write to a single DAC/V<sub>COM</sub> register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF16821 acknowledges this byte.
3. Send a DAC/V<sub>COM</sub> pointer address byte. Set bit D7 = 0 and D6 = 0. Bits D5–D0 are the DAC/V<sub>COM</sub> address. Although the BUF16821 acknowledges 000000 through 010111, it stores and returns data only from these addresses:
  - 000000 through 001111
  - 010010 through 010011
 It returns 0000 for reads from 010000 through 010001, and 010100 through 010111. See Table 4 for valid DAC/V<sub>COM</sub> addresses.
4. Send two bytes of data for the specified register. Begin by sending the most significant byte first (bits D15–D8, of which only bits D9 and D8 are used, and bits D15–D14 must not be 01), followed by the least significant byte (bits D7–D0). The register is updated after receiving the second byte.
5. Send a STOP or START condition on the bus.

The BUF16821 acknowledges each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified register is not updated. Updating the DAC/V<sub>COM</sub> register is not the same as updating the DAC/V<sub>COM</sub> output voltage; see the [Updating the DAC Outputs](#) section.

The process of updating multiple DAC/V<sub>COM</sub> registers begins the same as when updating a single register. However, instead of sending a STOP condition after writing the addressed register, the master continues to send data for the next register. The BUF16821 automatically and sequentially steps through subsequent registers as additional data are sent. The process continues until all desired registers have been updated or a STOP or START condition is sent.

To write to multiple DAC/V<sub>COM</sub> registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF16821 acknowledges this byte.
3. Send either the OUT1 pointer address byte to start at the first DAC, or send the pointer address byte for whichever DAC/V<sub>COM</sub> is the first in the sequence of DACs/V<sub>COM</sub>s to be updated. The BUF16821 begins with this DAC/V<sub>COM</sub> and steps through subsequent DACs/V<sub>COM</sub>s in sequential order.
4. Send the bytes of data; begin by sending the most significant byte (bits D15–D8, of which only bits D9 and D8 have meaning, and bits D15–D14 must not be 01), followed by the least significant byte (bits D7–D0). The first two bytes are for the DAC/V<sub>COM</sub> addressed in the previous step. The DAC/V<sub>COM</sub> register is automatically updated after receiving the second byte. The next two bytes are for the following DAC/V<sub>COM</sub>. That DAC/V<sub>COM</sub> register is updated after receiving the fourth byte. This process continues until the registers of all following DACs/V<sub>COM</sub>s have been updated. The BUF16821 continues to accept data for a total of 18 DACs; however, the two data sets following the 16th data set are meaningless. The 19th and 20th data sets apply to V<sub>COM</sub>1 and V<sub>COM</sub>2. The write disable bit cannot be accessed using this method. It must be written to using *the write to a single DAC register procedure*.

5. Send a STOP or START condition on the bus.

The BUF16821 acknowledges each byte. To terminate communication, send a STOP or START condition on the bus. Only DAC registers that have received both bytes of data are updated.

#### Reading: DAC/V<sub>COM</sub>/OTHER Register (Volatile Memory)

Reading a register returns the data stored in that DAC/V<sub>COM</sub>/OTHER register.

To read a single DAC/V<sub>COM</sub>/OTHER register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF16821 acknowledges this byte.
3. Send the DAC/V<sub>COM</sub>/OTHER pointer address byte. Set bit D7 = 0 and D6 = 0; bits D5–D0 are the DAC/V<sub>COM</sub>/OTHER address. NOTE: The BUF16821 stores and returns data only from these addresses:
  - 000000 through 001111
  - 010010
  - 010011
  - 111100 through 111111
 It returns 0000 for reads from 010000 and 010001, and 010100 through 010111. See [Table 4](#) for valid DAC/V<sub>COM</sub>/OTHER addresses.
4. Send a START or STOP/START condition.
5. Send the correct device address and read/write bit = HIGH. The BUF16821 acknowledges this byte.
6. Receive two bytes of data. They are for the specified register. The most significant byte (bits D15–D8) is received first; next is the least significant byte (bits D7–D0). In the case of DAC/V<sub>COM</sub> channels, bits D15–D10 have no meaning.
7. Acknowledge after receiving the first byte.
8. Send a STOP or START condition on the bus or do not acknowledge the second byte to end the read transaction.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not acknowledging.

To read multiple registers:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF16821 acknowledges this byte.
3. Send either the OUT1 pointer address byte to start at the first DAC, or send the pointer address byte for whichever register is the first in the sequence of DACs/ $V_{COM}$ s to be read. The BUF16821 begins with this DAC/ $V_{COM}$  and steps through subsequent DACs/ $V_{COM}$ s in sequential order.
4. Send a START or STOP/START condition on the bus.
5. Send the correct device address and read/write bit = HIGH. The BUF16821 acknowledges this byte.
6. Receive two bytes of data. They are for the specified DAC/ $V_{COM}$ . The first received byte is the most significant byte (bits D15–D8; only bits D9 and D8 have meaning), next is the least significant byte (bits D7–D0).
7. Acknowledge after receiving each byte of data.
8. When all desired DACs have been read, send a STOP or START condition on the bus.

Communication may be terminated by sending a premature STOP or START condition on the bus, or by not sending the acknowledge bit. The reading of registers DieID, DieRev, and MaxBank is not supported in this mode of operation (these values must be read using the single register read method).

#### Write: Nonvolatile Memory for the DAC Register

The BUF16821 is able to write to the nonvolatile memory of a single DAC/ $V_{COM}$  in a single communication transaction. In contrast to the BUF20820, writing to multiple nonvolatile memory words in a single transaction is not supported. Valid DAC/ $V_{COM}$  pointer addresses begin with 000000 (which corresponds to OUT1) through 001111 (which corresponds to OUT16). Addresses 010010 and 010011 are  $V_{COM1}$  and  $V_{COM2}$ , respectively.

When programming the nonvolatile memory, the analog supply voltage must be between 9V and 20V. Write commands are performed by setting the read/write bit LOW.

To write to a single nonvolatile register:

1. Send a START condition on the bus.
2. Send the device address and read/write bit = LOW. The BUF16821 acknowledges this byte. Although the BUF16821 acknowledges 000000 through 010111, it stores and returns data only from these addresses:
  - 000000 through 001111
  - 010010 and 010011
 It returns 0000 for reads from 010000 through 010001, and 010100 through 010111. See [Table 4](#) for DAC/ $V_{COM}$  addresses.
3. Send a DAC/ $V_{COM}$  pointer address byte. Set bit D7 = 0 and D6 = 0. Bits D5–D0 are the DAC/ $V_{COM}$  address.
4. Send two bytes of data for the nonvolatile register of the specified DAC/ $V_{COM}$ . Begin by sending the most significant byte first (bits D15–D8, of which only bits D9 and D8 are data bits, and bits D15–D14 must be 01), followed by the least significant byte (bits D7–D0). The register is updated after receiving the second byte.
5. Send a STOP condition on the bus.

The BUF16821 acknowledges each data byte. If the master terminates communication early by sending a STOP or START condition on the bus, the specified nonvolatile register is not updated. Writing a nonvolatile register also updates the DAC/ $V_{COM}$  register and output voltage.

The DAC/ $V_{COM}$  register and DAC/ $V_{COM}$  output voltage are updated immediately, while the programming of the nonvolatile memory takes up to 250 $\mu$ s. Once a nonvolatile register write command has been issued, no communication with the BUF16821 should take place for at least 250 $\mu$ s. Writing or reading over the serial interface while the nonvolatile memory is being written jeopardizes the integrity of the data being stored.

#### Read: Nonvolatile Memory for the DAC Register

To read the data present in nonvolatile register for a particular DAC/ $V_{COM}$  channel, the master must first issue a general acquire command, or a single acquire command with the appropriate DAC/ $V_{COM}$  channel chosen. This action updates both the DAC/ $V_{COM}$  register(s) and DAC/ $V_{COM}$  output voltage(s). The master may then read from the appropriate DAC/ $V_{COM}$  register as described earlier.

**Table 4. DAC Register Pointer Addresses**

<b>DAC REGISTER</b>	<b>POINTER ADDRESS</b>
OUT1	000000
OUT2	000001
OUT3	000010
OUT4	000011
OUT5	000100
OUT6	000101
OUT7	000110
OUT8	000111
OUT9	001000
OUT10	001001
OUT11	001010
OUT12	001011
OUT13	001100
OUT14	001101
OUT15	001110
OUT16	001111
V <sub>COM1</sub>	010010
V <sub>COM2</sub>	010011
<b>OTHER REGISTER</b>	<b>POINTER ADDRESS</b>
Die_Rev	111100
Die_ID	111101
MaxBank	111111

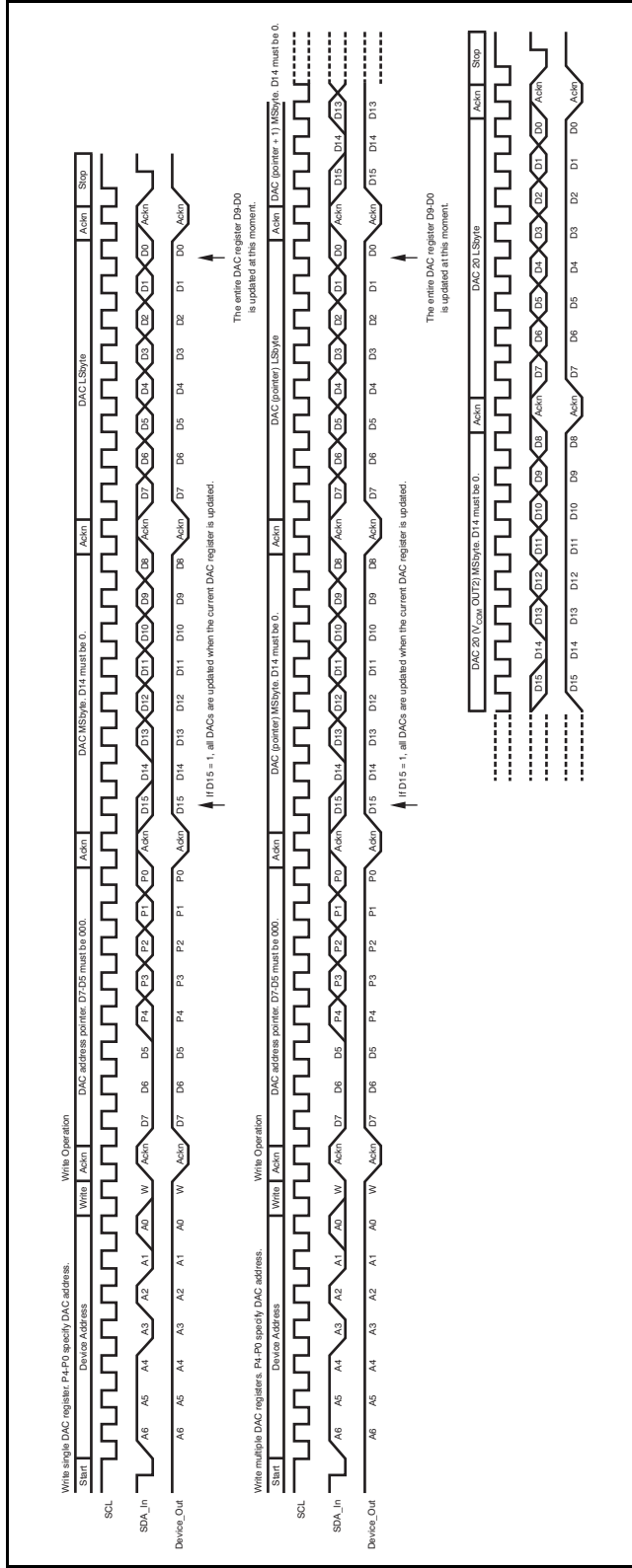


Figure 11. Write DAC Register Timing

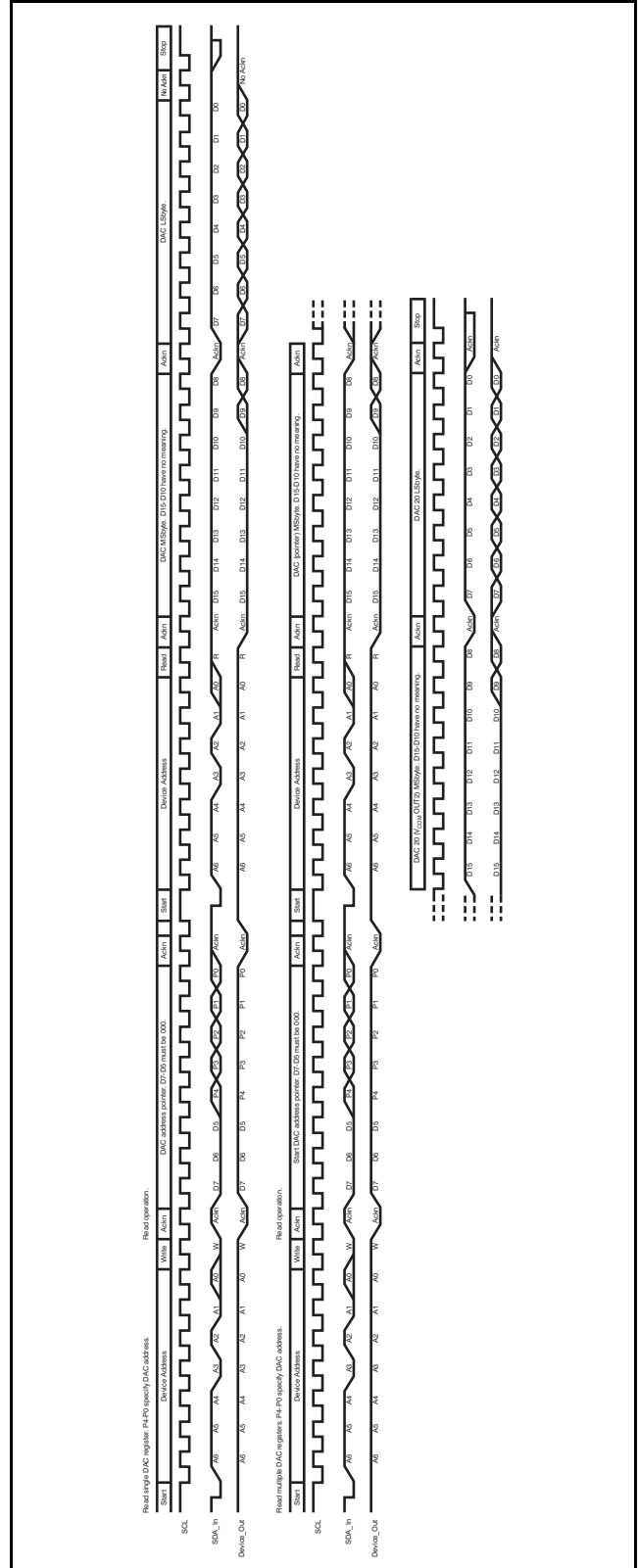
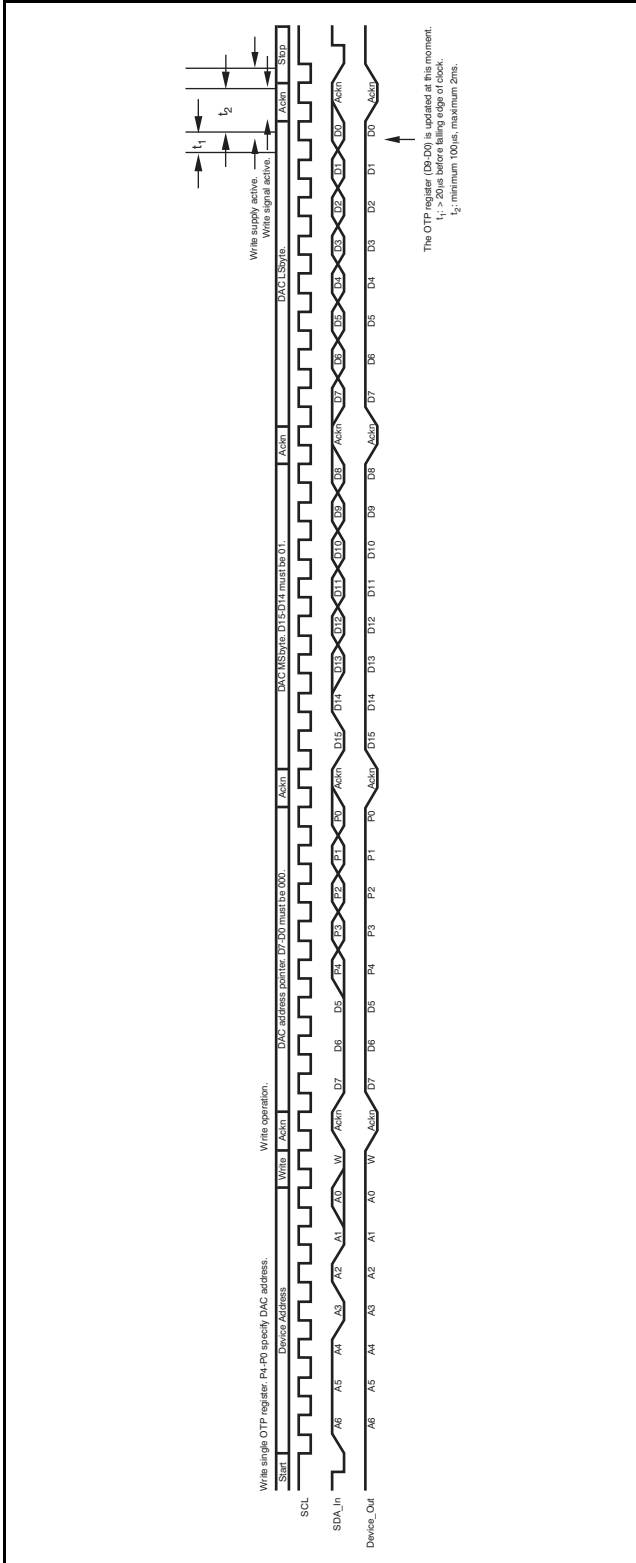
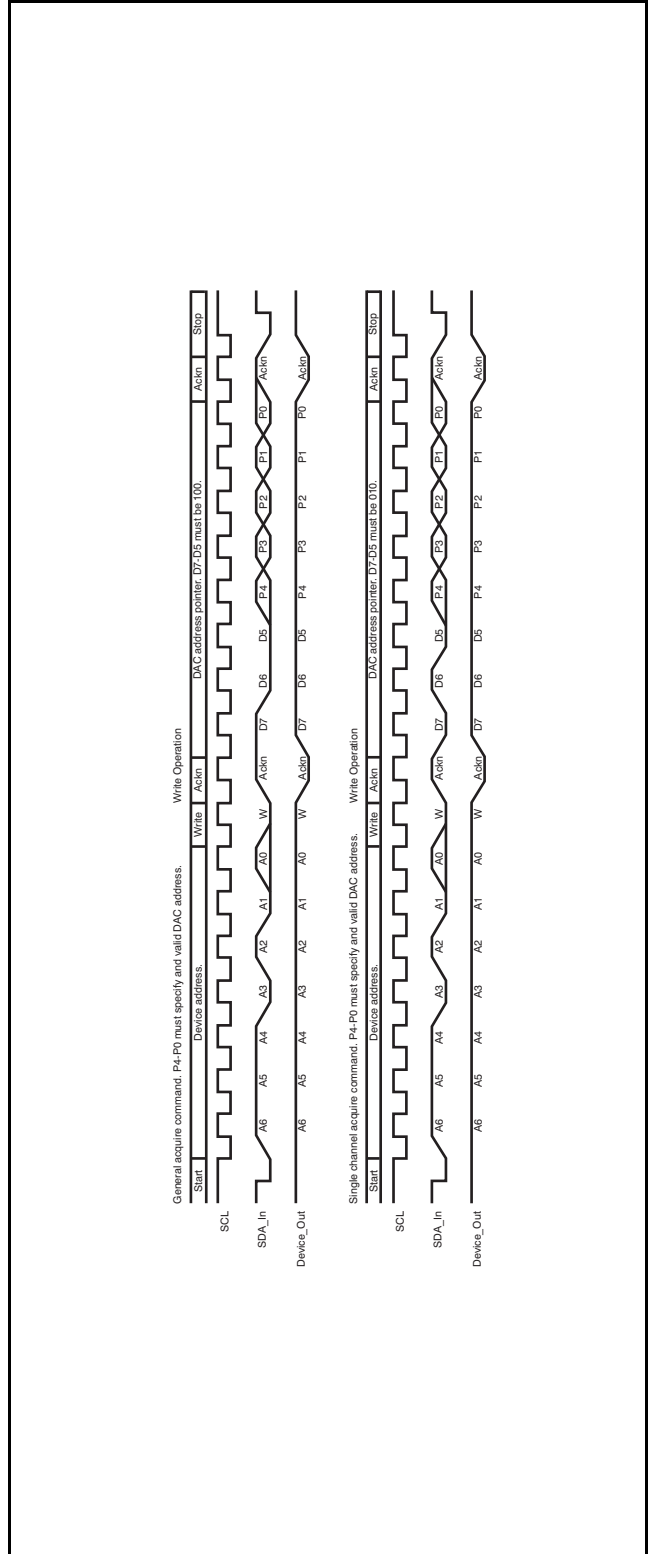


Figure 12. Read Register Timing





**Figure 13. Write Nonvolatile Register Timing**



**Figure 14. Acquire Operation Timing**

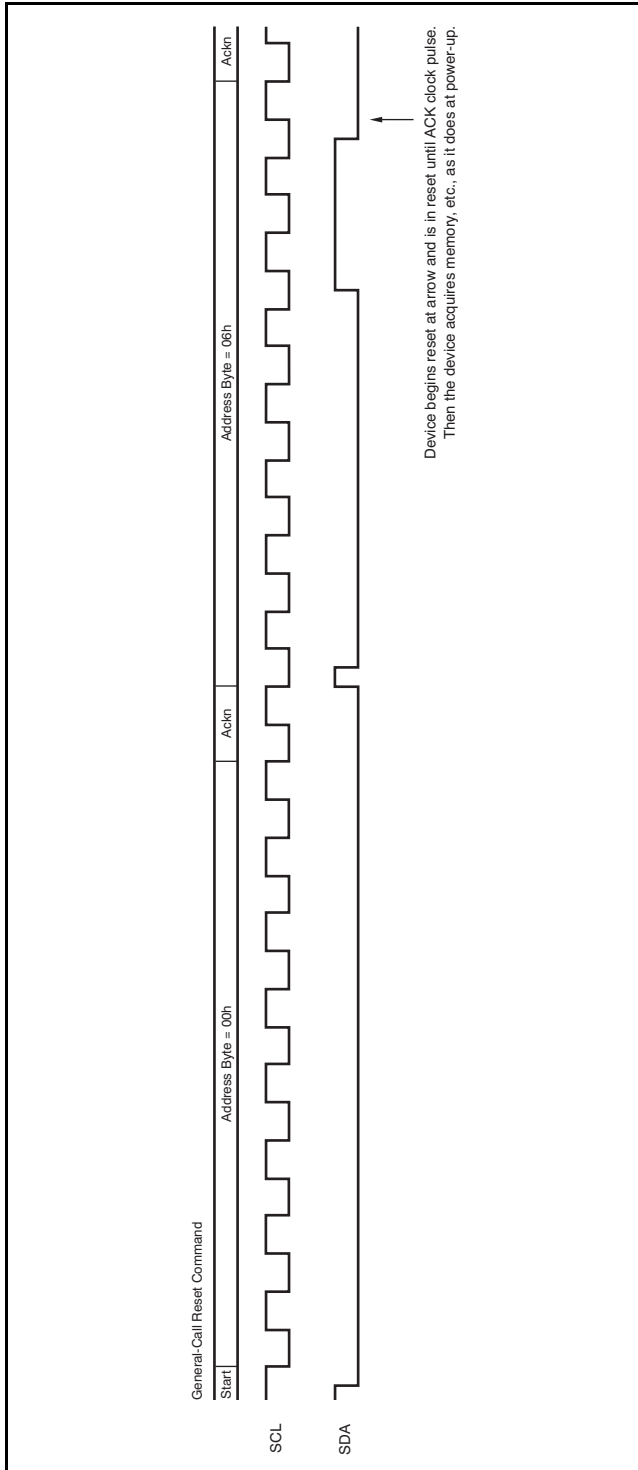


Figure 15. General-Call Reset Timing

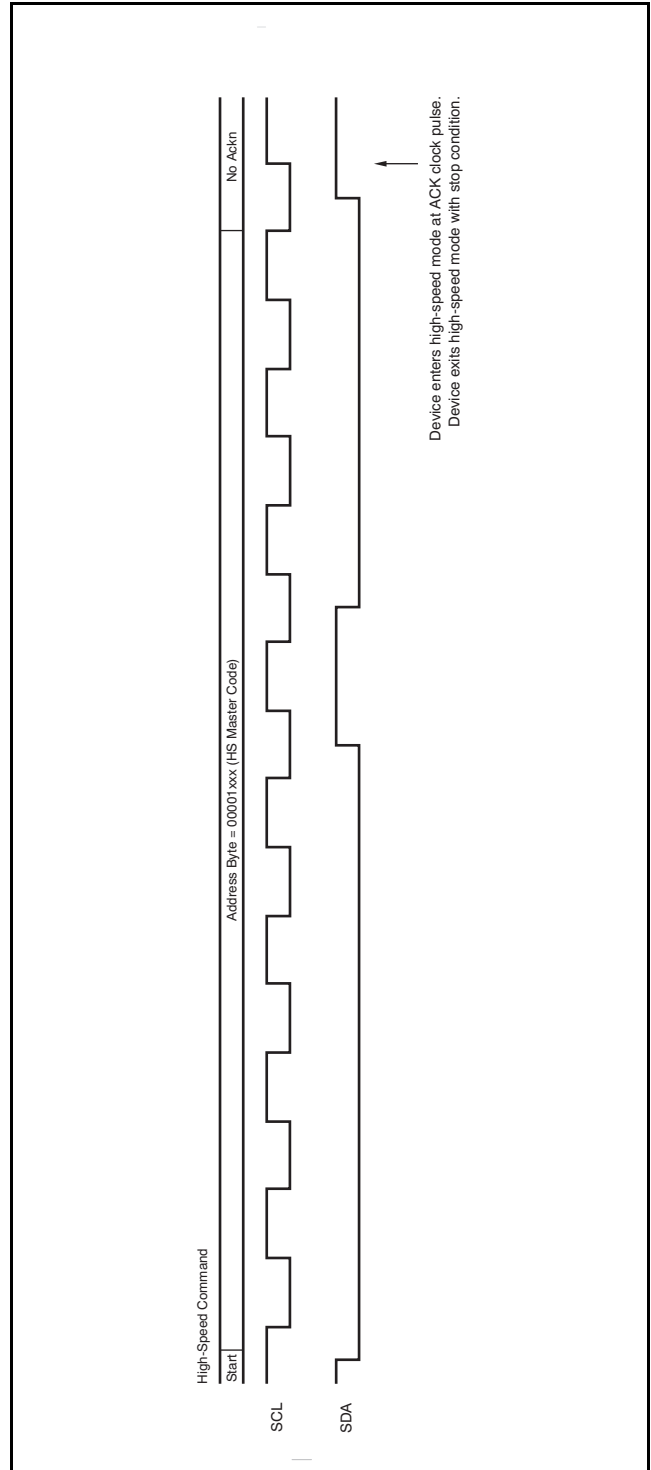


Figure 16. High-Speed Mode Timing

## END-USER SELECTED GAMMA CONTROL

Because the BUF16821 has two banks of nonvolatile memory, it is well-suited for providing two levels of gamma control by using the BKSEL pin, as shown in Figure 17. When the state of the BKSEL pin changes, the BUF16821 updates all 18 programmable buffer outputs simultaneously after 750µs (±80µs).

To update all 18 programmable output voltages simultaneously via hardware, toggle the BKSEL pin to switch between Gamma Curve 0 (stored in Bank0) and Gamma Curve 1 (stored in Bank1).

All DAC/V<sub>COM</sub> registers and output voltages are updated simultaneously after approximately 750µs.

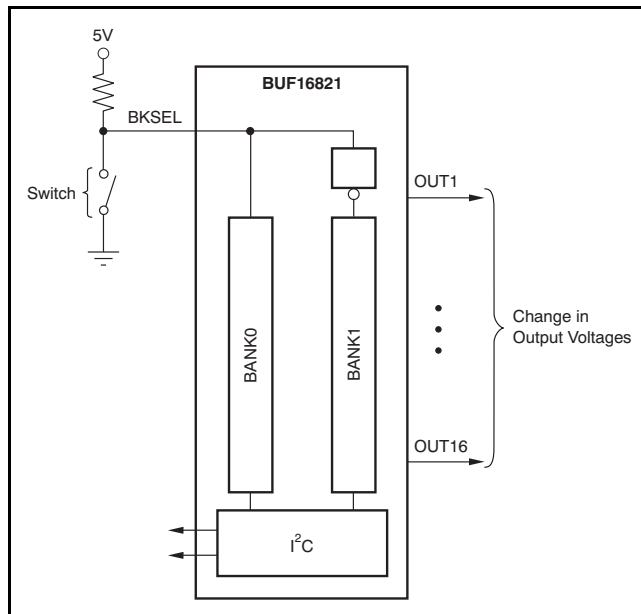


Figure 17. Gamma Control

## DYNAMIC GAMMA CONTROL

Dynamic gamma control is a technique used to improve the picture quality in LCD television applications. This technique typically requires switching gamma curves between frames. Using the BKSEL pin to switch between two gamma curves does not often provide good results because of the 750µs required to transfer the data from the nonvolatile memory to the DAC register. However, dynamic gamma control can still be accomplished by storing two gamma curves in an external EEPROM and writing directly to the DAC register (volatile).

The double register input structure saves programming time by allowing updated DAC values to be pre-stored into the first register bank. Storage of this data can occur while a picture is still being displayed. Because the data are only stored into the first register bank, the DAC/V<sub>COM</sub> output values remain unchanged—the display is unaffected. At the beginning or the end of a picture frame, the DAC/V<sub>COM</sub> outputs (and therefore, the gamma voltages) can be quickly updated by writing a '1' in bit 15 of any DAC/V<sub>COM</sub> register. For details on the operation of the double register input structure, see the [Updating the DAC Outputs](#) section.

To update all 18 programmable output voltages simultaneously via software, perform the following actions:

**STEP 1:** Write to registers 1–18 with bit 15 always '0'.

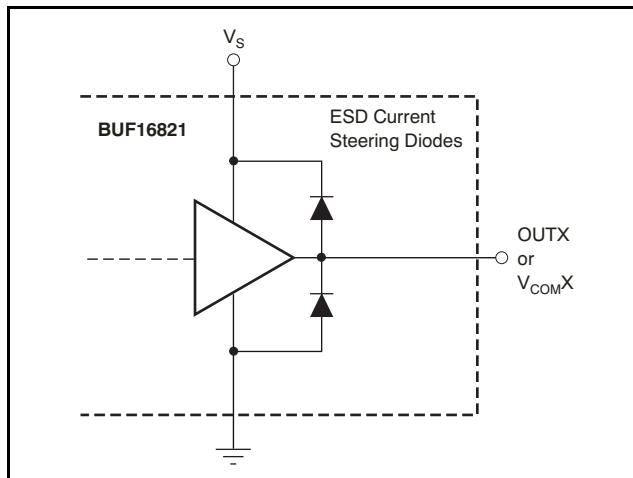
**STEP 2:** Write any DAC/V<sub>COM</sub> register a second time with identical data. Make sure that bit 15 is set to '1'. All DAC/V<sub>COM</sub> channels are updated simultaneously after receiving the last bit of data.

### OUTPUT PROTECTION

The BUF16821 output stages can safely source and sink the current levels indicated in Figure 1 and Figure 2. However, there are other modes where precautions must be taken to prevent to the output stages from being damaged by excessive current flow. The outputs (OUT1 through OUT16,  $V_{COM1}$  and  $V_{COM2}$ ) include ESD protection diodes, as shown in Figure 18. Normally, these diodes do not conduct and are passive during typical device operation. Unusual operating conditions can occur where the diodes may conduct, potentially subjecting them to high, even damaging current levels. These conditions are most likely to occur when a voltage applied to an output exceeds  $(V_S) + 0.5V$ , or drops below  $GND - 0.5V$ .

One common scenario where this condition can occur is when the output pin is connected to a sufficiently large capacitor, and the BUF16821 power-supply source ( $V_S$ ) is suddenly removed. Removing the power-supply source allows the capacitor to discharge through the current-steering diodes. The energy released during the high current flow period causes the power dissipation limits of the diode to be

exceeded. Protection against the high current flow may be provided by placing current-limiting resistors in series with the output, as shown in Figure 10. Select a resistor value that restricts the current level to the maximum rating for the particular pin.



**Figure 18. Output Pins ESD Protection Current-Steering Diodes**

## GENERAL POWERPAD DESIGN CONSIDERATIONS

The BUF16821 is available in a thermally-enhanced PowerPAD package. This package is constructed using a downset leadframe upon which the die is mounted; see [Figure 19\(a\)](#) and [Figure 19\(b\)](#). This arrangement results in the lead frame being exposed as a thermal pad on the underside of the package; see [Figure 19\(c\)](#). This thermal pad has direct thermal contact with the die; thus, excellent thermal performance is achieved by providing a good thermal path away from the thermal pad.

The PowerPAD package allows for both assembly and thermal management in one manufacturing operation. During the surface-mount solder operation (when the leads are being soldered), the thermal pad must be soldered to a copper area underneath the package. Through the use of thermal paths within this copper area, heat can be conducted away from the package into either a ground plane or other heat-dissipating device. Soldering the PowerPAD to the printed circuit board (PCB) is always required, even with applications that have low power dissipation. This technique provides the necessary thermal and mechanical connection between the lead frame die pad and the PCB.

The PowerPAD must be connected to the most negative supply voltage on the device,  $GND_A$  and  $GND_D$ .

1. Prepare the PCB with a top-side etch pattern. There should be etching for the leads as well as etch for the thermal pad.
2. Place recommended holes in the area of the thermal pad. Ideal thermal land size and thermal via patterns for the HTSSOP-28 PWP package can be seen in the technical brief, *PowerPAD Thermally-Enhanced Package (SLMA002)*, available for download at [www.ti.com](http://www.ti.com). These holes should be 13 mils (0,33mm) in diameter. Keep them small, so that solder wicking through the holes is not a problem during reflow. An

example thermal land pattern mechanical drawing is attached to the end of this data sheet.

3. Additional vias may be placed anywhere along the thermal plane outside of the thermal pad area to help dissipate the heat generated by the BUF16821 IC. These additional vias may be larger than the 13-mil diameter vias directly under the thermal pad. They can be larger because they are not in the thermal pad area to be soldered; thus, wicking is not a problem.
4. Connect all holes to the internal plane that is at the same voltage potential as the GND pins.
5. When connecting these holes to the internal plane, do not use the typical web or spoke via connection methodology. Web connections have a high thermal resistance connection that is useful for slowing the heat transfer during soldering operations. This configuration makes the soldering of vias that have plane connections easier. In this application, however, low thermal resistance is desired for the most efficient heat transfer. Therefore, the holes under the BUF16821 PowerPAD package should make their connection to the internal plane with a complete connection around the entire circumference of the plated-through hole.
6. The top-side solder mask should leave the terminals of the package and the thermal pad area with its twelve holes exposed. The bottom-side solder mask should cover the holes of the thermal pad area. This masking prevents solder from being pulled away from the thermal pad area during the reflow process.
7. Apply solder paste to the exposed thermal pad area and all of the IC terminals.
8. With these preparatory steps in place, simply place the BUF16821 IC in position and run the chip through the solder reflow operation as any standard surface-mount component. This preparation results in a properly installed part.

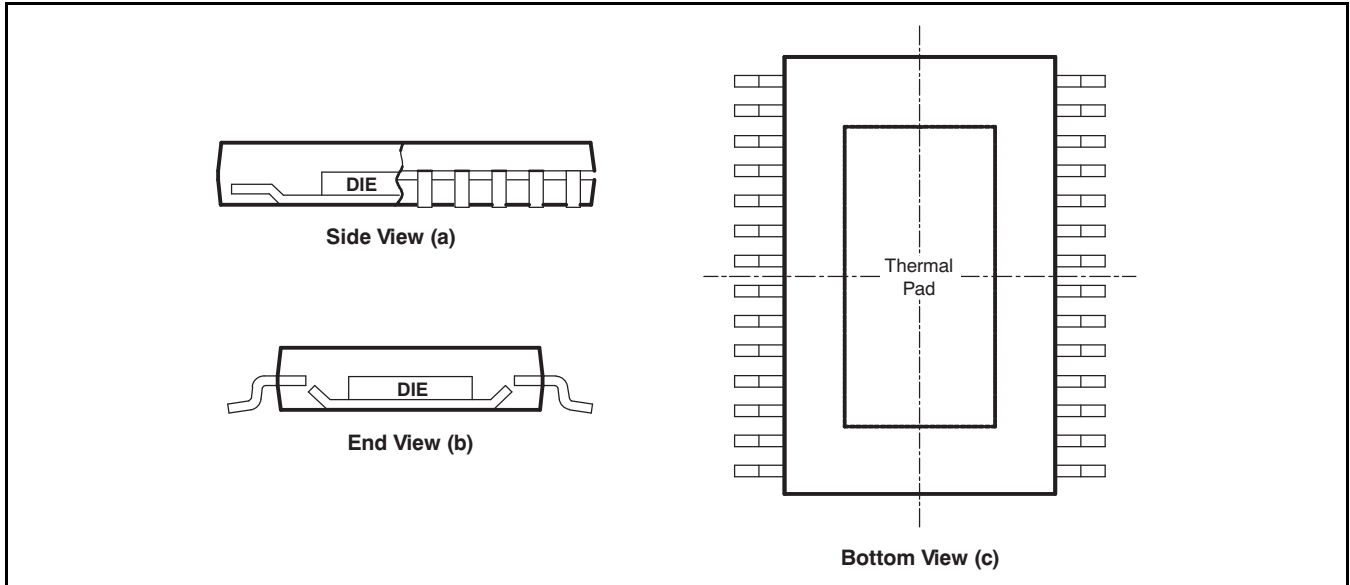


Figure 19. Views of Thermally-Enhanced PWP Package

For a given  $\theta_{JA}$  (listed in the [Electrical Characteristics](#)), the maximum power dissipation is shown in [Figure 20](#) and calculated by [Equation 2](#):

$$P_D = \left( \frac{T_{MAX} - T_A}{\theta_{JA}} \right) \tag{2}$$

Where:

$P_D$  = maximum power dissipation (W)

$T_{MAX}$  = absolute maximum junction temperature (+125°C)

$T_A$  = free-ambient air temperature (°C)

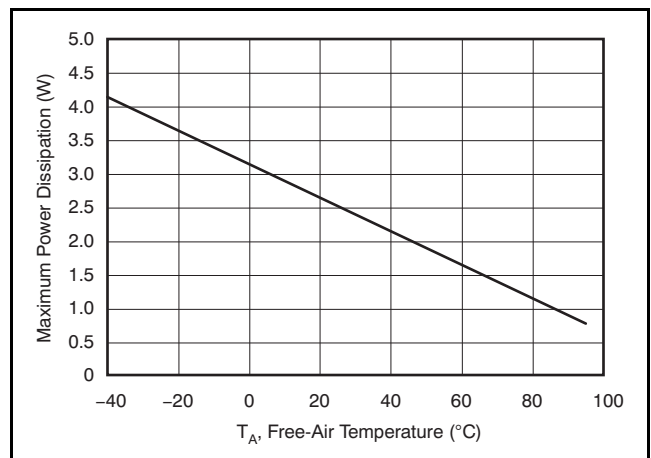


Figure 20. Maximum Power Dissipation vs Free-Air Temperature (with PowerPAD soldered down)

## REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

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### Changes from Revision B (May, 2009) to Revision C Page

- Corrected error in x-axis value for [Figure 9](#) ..... 7
- 

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### Changes from Revision A (February, 2009) to Revision B Page

- Changed title of [Figure 6](#) ..... 6
  - Changed title of [Figure 7](#) ..... 7
-

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BUF16821AIPWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BUF16821	<a href="#">Samples</a>
BUF16821BIPWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BUF16821B	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF BUF16821 :**

- Automotive: [BUF16821-Q1](#)

## NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BUF16821AIPWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
BUF16821BIPWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BUF16821AIPWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0
BUF16821BIPWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

## GENERIC PACKAGE VIEW

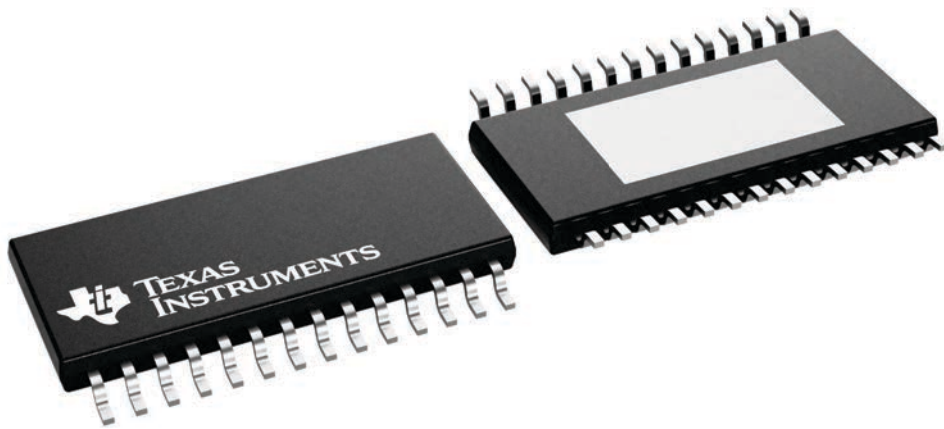
**PWP 28**

**PowerPAD™ TSSOP - 1.2 mm max height**

4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

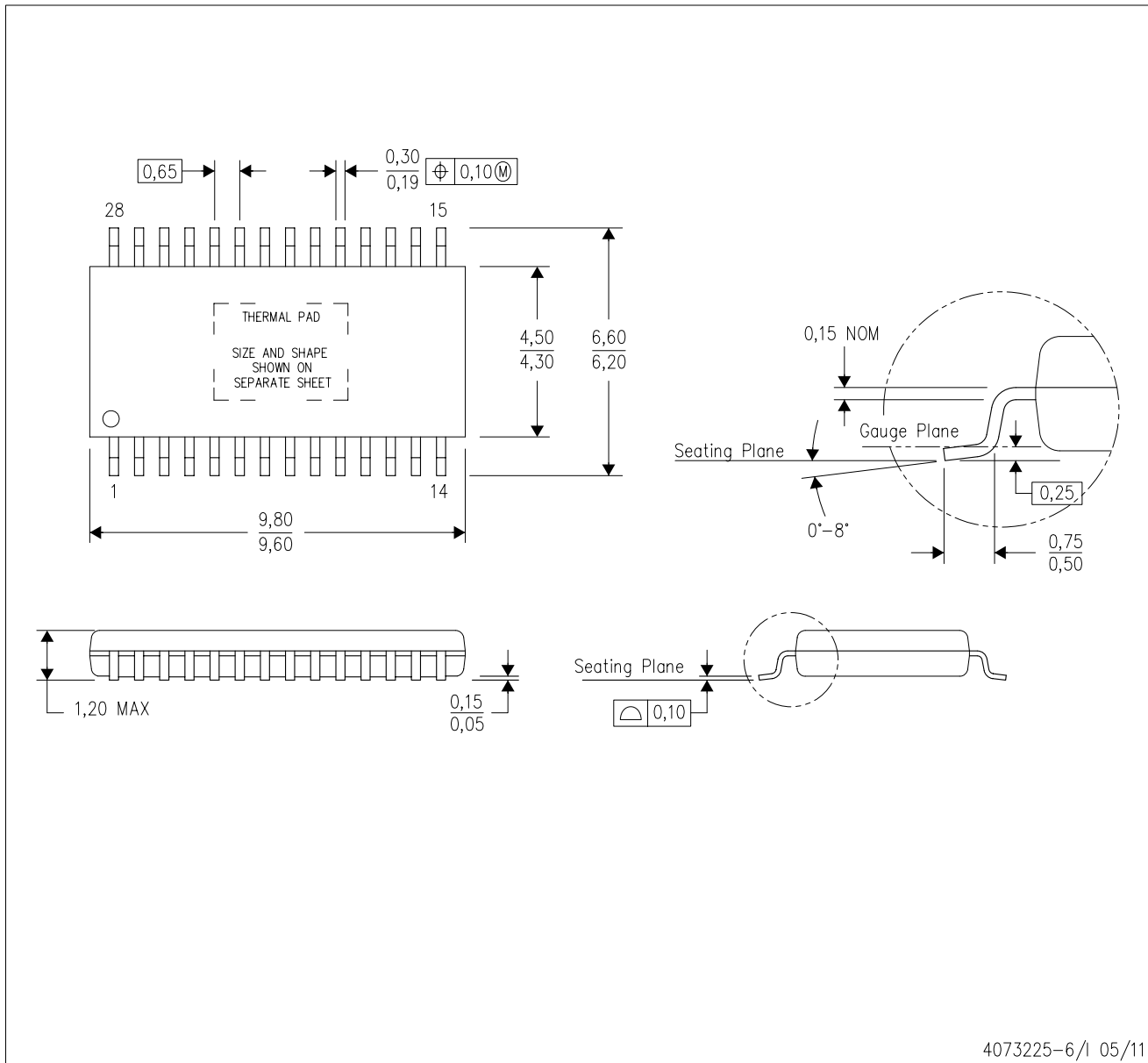


4224765/B

# MECHANICAL DATA

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



4073225-6/1 05/11

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

# THERMAL PAD MECHANICAL DATA

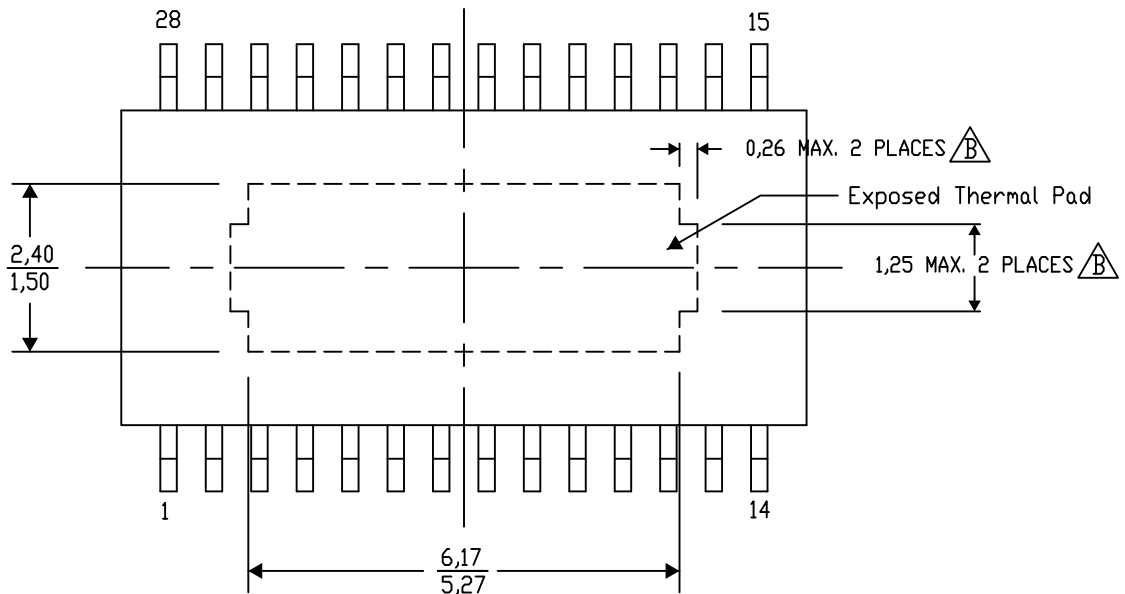
## PWP (R-PDSO-G28) PowerPAD™ SMALL PLASTIC OUTLINE

### THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-33/AO 01/16

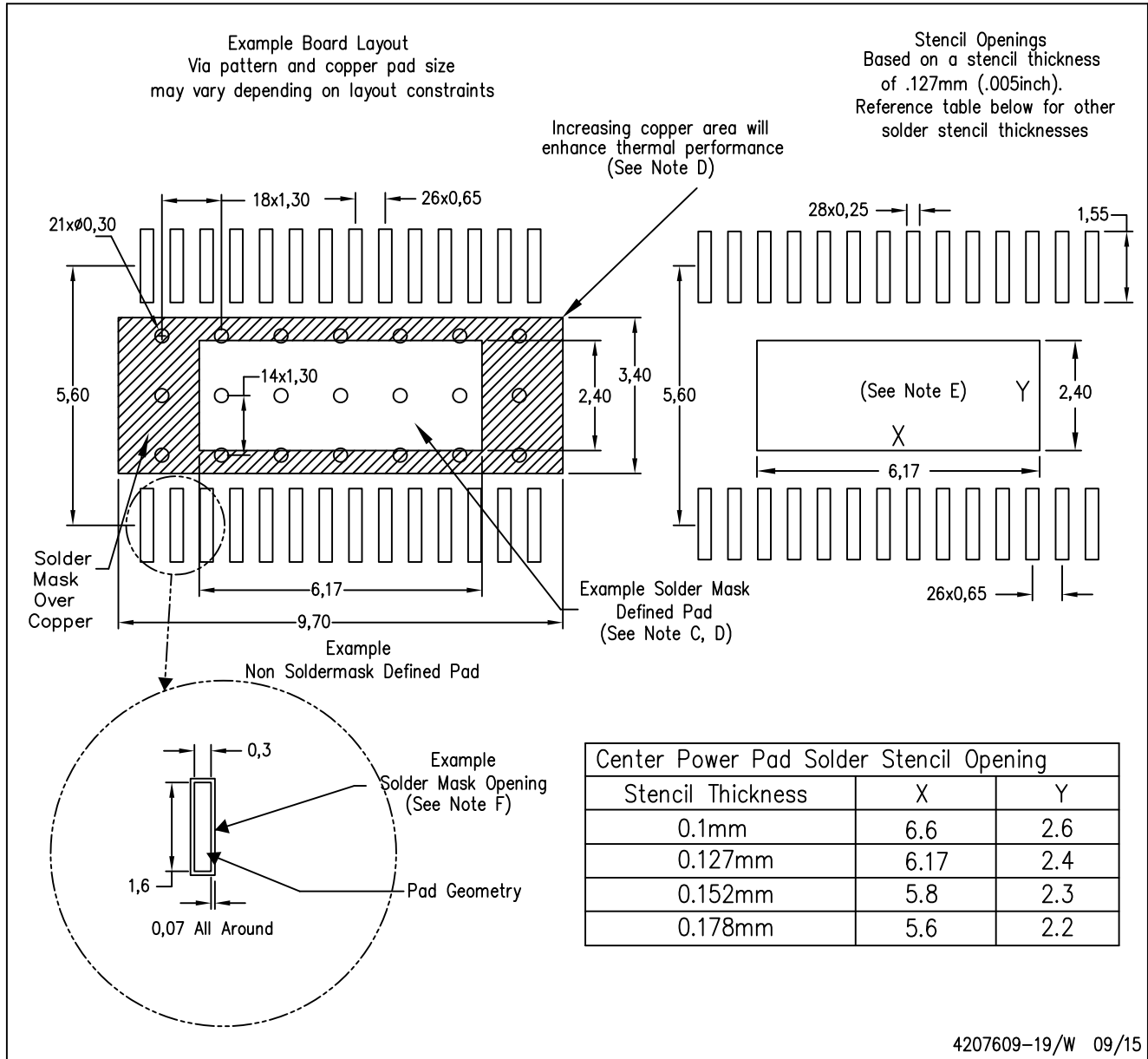
NOTE: A. All linear dimensions are in millimeters

$\triangle B$ . Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G28)

PowerPAD™ PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.
  - For specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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