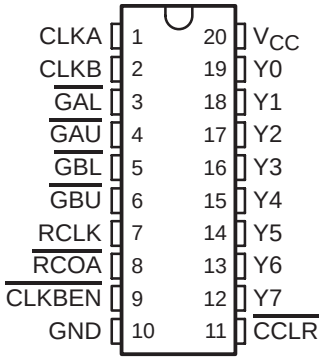
- **Controlled Baseline**
  - **One Assembly Site**
  - **One Test Site**
  - **One Fabrication Site**
- **Extended Temperature Performance of −55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree†**
- **Can Be Used as Two 16 Bit Counters or a Single 32 Bit Counter**
- **2-V to 5.5-V V_{CC} Operation**
- **Max t_{pd} of 25 ns at 5 V (RCLK to Y)**
- **Typical V_{OLP} (Output Ground Bounce) <0.7 V at V_{CC} = 5 V, T_A = 25°C**
- **Typical V_{OHV} (Output V_{OH} Undershoot) >4.4 V at V_{CC} = 5 V, T_A = 25°C**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

† Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

PW PACKAGE
(TOP VIEW)



description/ordering information

The SN74LV8154 is a dual 16 bit binary counter with 3-state output registers, designed for 2-V to 5.5-V V_{CC} operation.

This 16 bit counter (A or B) feeds a 16 bit storage register and each storage register is further divided into an upper byte and lower byte. The $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, and $\overline{GBU}$ inputs are used to select the byte that needs to be output at Y0−Y7. CLKA is the clock for A counter and CLKB is the clock for B counter. RCLK is the clock for the A and B storage registers. All three clock signals are positive-edge triggered.

A 32 bit counter can be realized by connecting CLKA and CLKB together and by connecting $\overline{RCOA}$ to $\overline{CLKBEN}$.

To ensure the high-impedance state during power up or power down, $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, and $\overline{GBU}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION†

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−55°C to 125°C	TSSOP − PW	Tape and reel	SN74LV8154MPWREP	LV8154ME

† For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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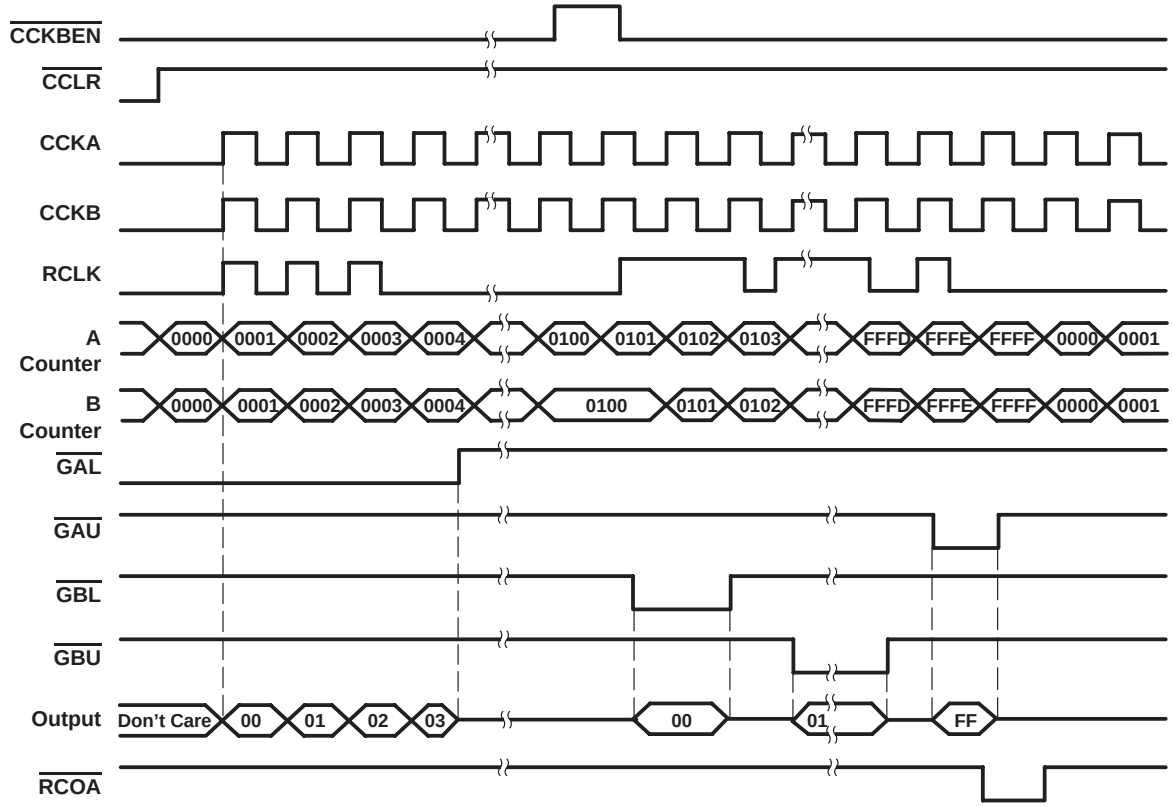
FUNCTION TABLE
(each buffer)

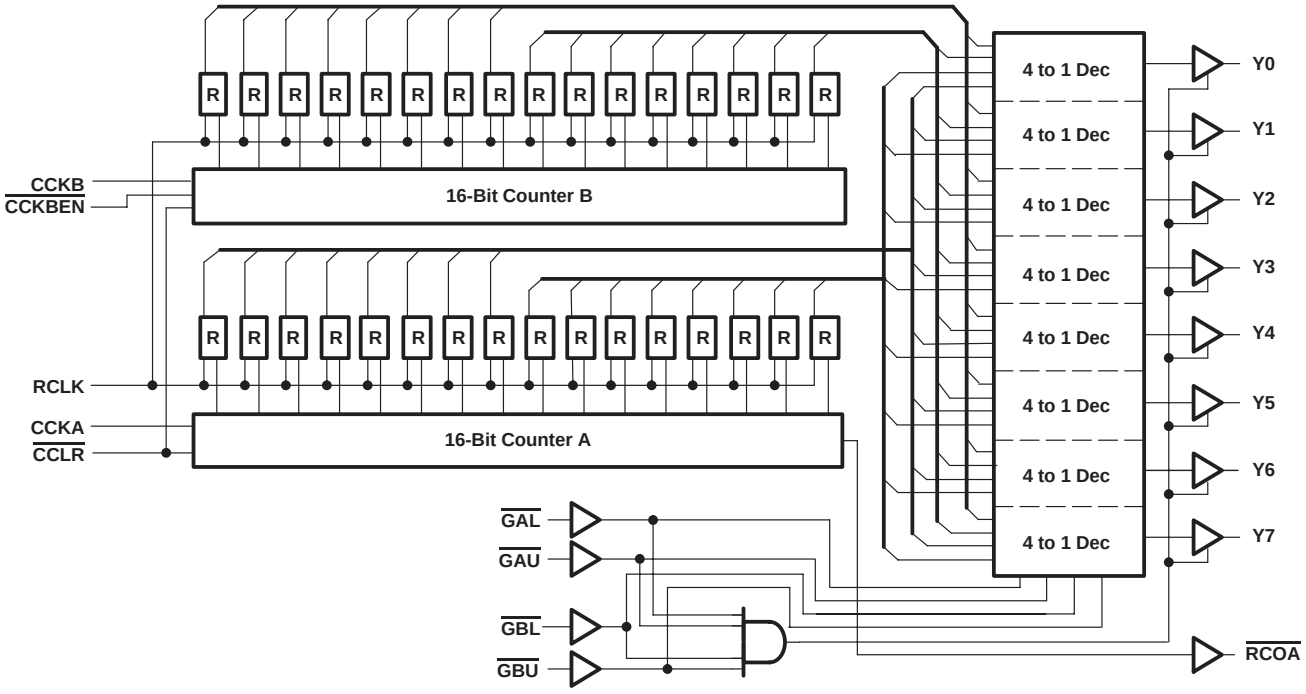
INPUTS				OUTPUT
$\overline{GAL}$	$\overline{GAU}$	$\overline{GBL}$	$\overline{GBU}$	Yn
L	H	H	H	Lower byte in A register
H	L	H	H	Upper byte in A register
H	H	L	H	Lower byte in B register
H	H	H	L	Upper byte in B register
H	H	H	H	Z

Combinations of $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, and $\overline{GBU}$, other than those shown above, are prohibited. If more than one input is L at the same time, the output data (Y0−Y7) may be invalid.

timing diagram



block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high-impedance
or power-off state, V_O (see Note 1) . . . . . −0.5 V to 7 V
Output voltage range, V_O (see Note 1 and Note 2) . . . . . −0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 V) . . . . . −20 mA
Output clamp current, I_{OK} (V_O < 0 V) . . . . . −50 mA
Continuous output current, I_O (V_O = 0 V to V_{CC}) . . . . . ±35 mA
Continuous current through V_{CC} or GND . . . . . ±70 mA
Package thermal impedance, θ_{JA} (see Note 3): . . . . . 83°C/W
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. This value is limited to 5.5 V maximum.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

			V_{CC}	MIN	MAX	UNIT
V_{CC}	Supply voltage			2	5.5	V
V_{IH}	High-level input voltage		2 V	1.5		V
			3 V to 3.6 V	$V_{CC} \times 0.7$		
			4.5 V to 5.5 V	$V_{CC} \times 0.7$		
V_{IL}	Low-level input voltage		2 V		0.5	V
			3 V to 3.6 V		$V_{CC} \times 0.3$	
			4.5 V to 5.5 V		$V_{CC} \times 0.3$	
V_I	Input voltage			0	5.5	V
V_O	Output voltage	High or low state		0	V_{CC}	V
		3-state		0	5.5	
I_{OH}	High-level output current	Yn outputs	2 V		−50	µA
			3 V to 3.6 V		−6	mA
			4.5 V to 5.5 V		−12	
		$\overline{RCOA}$	2 V		−50	µA
			3 V to 3.6 V		−6	mA
			4.5 V to 5.5 V		−12	
I_{OL}	Low-level output current	Yn outputs	2 V		50	µA
			3 V to 3.6 V		6	mA
			4.5 V to 5.5 V		12	
		$\overline{RCOA}$	2 V		50	µA
			3 V to 3.6 V		6	mA
			4.5 V to 5.5 V		12	
$\Delta t/\Delta v$	Input transition rise or fall rate		3 V to 3.6 V		100	ns/V
			4.5 V to 5.5 V		20	
T_A	Operating free-air temperature			−55	125	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. See the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	Yn	I_{OH} = −50 μA	2 V	1.9			V
		I_{OH} = −6 mA	3 V	2.48			
		I_{OH} = −12 mA	4.5 V	3.8			
	$\overline{RCOA}$	I_{OH} = −50 μA	2 V	1.9			
		I_{OH} = −6 mA	3 V	2.48			
		I_{OH} = −12 mA	4.5 V	3.8			
V_{OL}	Yn	I_{OL} = 50 μA	2 V			0.1	V
		I_{OL} = 6 mA	3 V			0.44	
		I_{OL} = 12 mA	4.5 V			0.55	
	$\overline{RCOA}$	I_{OL} = 50 μA	2 V			0.1	
		I_{OL} = 6 mA	3 V			0.44	
		I_{OL} = 12 mA	4.5 V			0.55	
I_I		V_I = 5.5 V or GND	0 V to 5.5 V			±1	μA
I_{OZ}		$V_O = V_{CC}$ or GND	5.5 V			±5	μA
I_{CC}		$V_I = V_{CC}$ or GND, I_O = 0	5.5 V			20	μA
I_{off}		V_I or V_O = 0 V to 5.5 V	0 V			5	μA
C_i		$V_I = V_{CC}$ or GND	5 V		3		pF
C_o		$V_O = V_{CC}$ or GND	5 V		5		pF

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			MIN	MAX	UNIT
t_w	Pulse duration	CLKA, CLKB, and RCLK high or low	10		ns
		$\overline{CCLR}$ low	22		
t_{su}	Setup time	$\overline{CLKBEN}$ low before CLKB↑	13		ns
		$\overline{CCLR}$ high (inactive) before CLKA↑ or CLKB↑	13		
		CLKA↑ or CLKB↑ before RCLK↑	13		
		RCLK↑ before $\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, or $\overline{GBU}$ low	13		
		$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, or $\overline{GBU}$ high (inactive) before RCLK↑	13		
t_h	Hold time	$\overline{CLKBEN}$ low after CLKB↑	0		ns
		CLKA or CLKB after RCLK	0		
t_z†	Z-period	$\overline{GAL}$, $\overline{GAU}$, $\overline{GBL}$, and $\overline{GBU}$ all high before one of them switches low	200		ns

† t_z condition: C_L = 50 pF, R_L = 1 kΩ

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			MIN	MAX	UNIT
t_w	Pulse duration	CLKA, CLKB, and RCLK high or low	10		ns
		$\overline{\text{CCLR}}$ low	20		
t_{su}	Setup time	$\overline{\text{CLKBEN}}$ low before CLKB↑	10		ns
		$\overline{\text{CCLR}}$ high (inactive) before CLKA↑ or CLKB↑	10		
		CLKA↑ or CLKB↑ before RCLK↑	10		
		RCLK↑ before $\overline{\text{GAL}}$, $\overline{\text{GAU}}$, $\overline{\text{GBL}}$, or $\overline{\text{GBU}}$ low	10		
		$\overline{\text{GAL}}$, $\overline{\text{GAU}}$, $\overline{\text{GBL}}$, or $\overline{\text{GBU}}$ high (inactive) before RCLK↑	10		
t_h	Hold time	$\overline{\text{CLKBEN}}$ low after CLKB↑	0		ns
		CLKA or CLKB after RCLK	0		
t_z†	Z period	$\overline{\text{GAL}}$, $\overline{\text{GAU}}$, $\overline{\text{GBL}}$, and $\overline{\text{GBU}}$ all high before one of them switches low	200		ns

† t_z condition: C_L = 50 pF, R_L = 1 kΩ

switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C TYP	MIN	MAX	UNIT
f_{MAX}			C_L = 50 pF		25		MHz
t_{pd}	RCLK	Y	C_L = 50 pF	25	1	42	ns
	CLKA	$\overline{\text{RCOA}}$		28	1	46	
t_{PLH}	$\overline{\text{CCLR}}$	$\overline{\text{RCOA}}$		20	1	35	ns
t_{en}	$\overline{\text{GAL}}$, $\overline{\text{GAU}}$, $\overline{\text{GBL}}$, $\overline{\text{GBU}}$	Y		30	1	50	ns
t_{dis}	$\overline{\text{GAL}}$, $\overline{\text{GAU}}$, $\overline{\text{GBL}}$, $\overline{\text{GBU}}$	Y		14	1	24	ns

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T_A = 25°C TYP	MIN	MAX	UNIT
f_{MAX}			C_L = 50 pF		25		MHz
t_{pd}	RCLK	Y	C_L = 50 pF	16	1	27	ns
	CLKA	$\overline{\text{RCOA}}$		17	1	28	
t_{PLH}	$\overline{\text{CCLR}}$	$\overline{\text{RCOA}}$		13	1	21	ns
t_{en}	$\overline{\text{GAL}}$, $\overline{\text{GAU}}$, $\overline{\text{GBL}}$, $\overline{\text{GBU}}$	Y		18	1	30	ns
t_{dis}	$\overline{\text{GAL}}$, $\overline{\text{GAU}}$, $\overline{\text{GBL}}$, $\overline{\text{GBU}}$	Y		9	1	16	ns

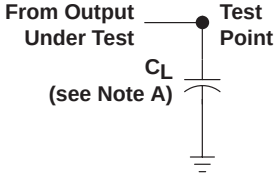
noise characteristics, V_{CC} = 5 V, C_L = 50 pF

PARAMETER		T_A = 25°C	UNIT
		TYP	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}	0.7	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	−0.75	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	4.4	V

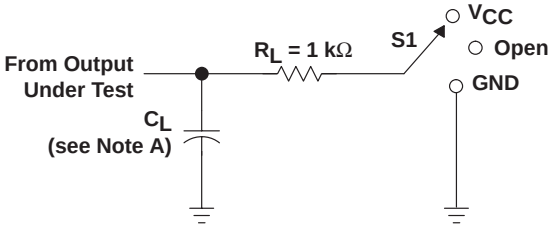
operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	TYP	UNIT
C_{pd}	Power dissipation capacitance	C_L = No load, CCLK = 10 MHz, RCLK = 1 MHz	56	pF

PARAMETER MEASUREMENT INFORMATION

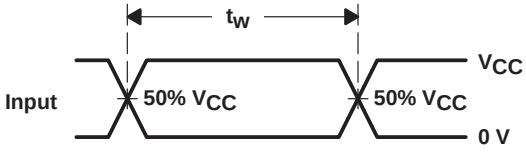


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

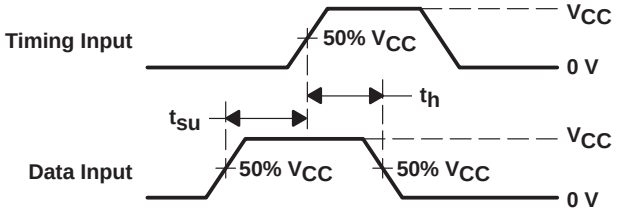


LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

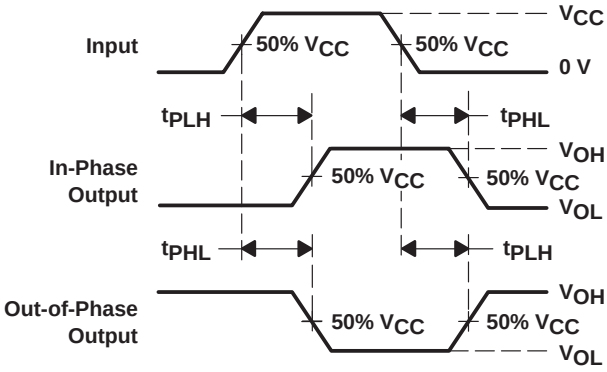
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}



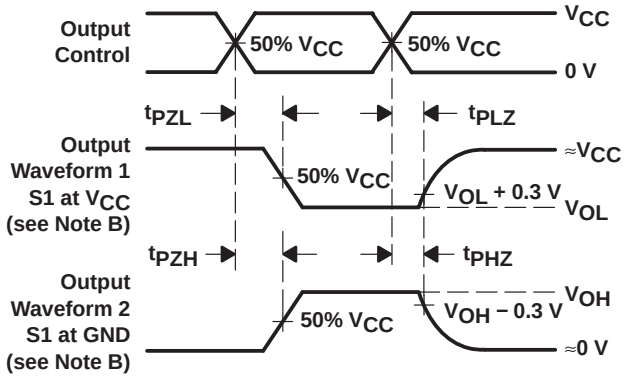
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r ≤ 3 ns, t_f ≤ 3 ns.
D. The outputs are measured one at a time, with one input transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PHL} and t_{PLH} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV8154MPWREP	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LV8154ME	Samples
V62/06662-01XE	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LV8154ME	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LV8154-EP :

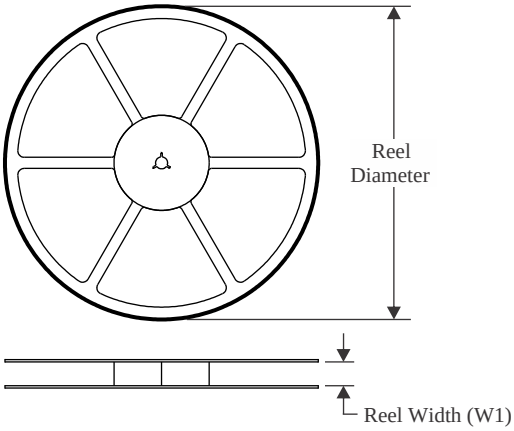
- Catalog: SN74LV8154

NOTE: Qualified Version Definitions:

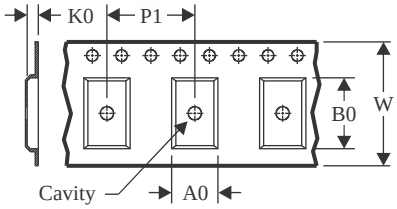
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

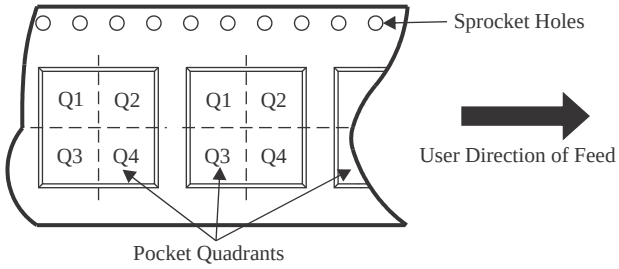


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

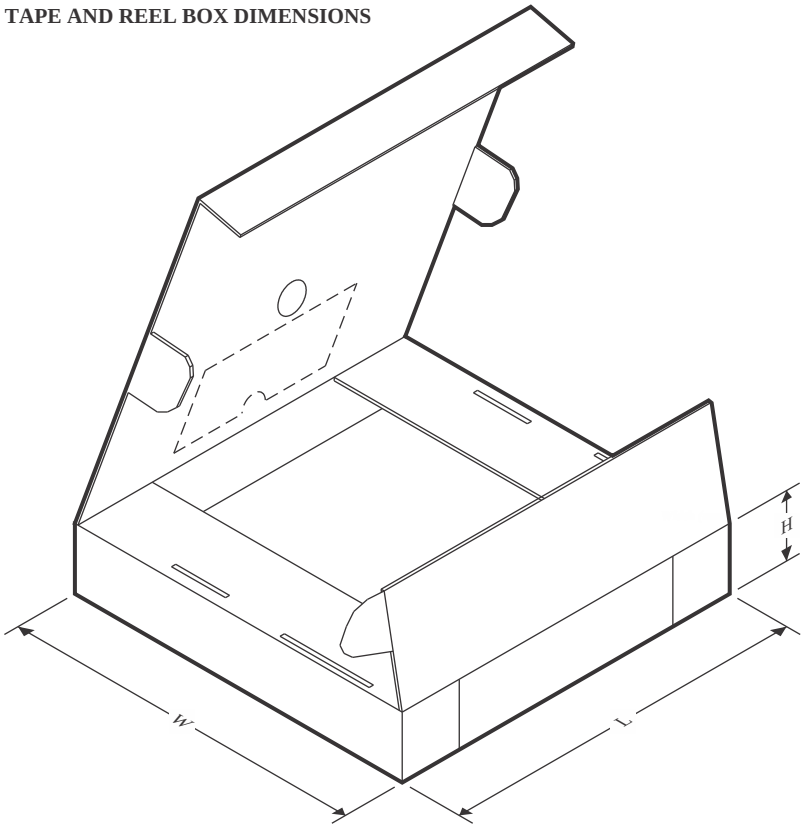
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV8154MPWREP	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

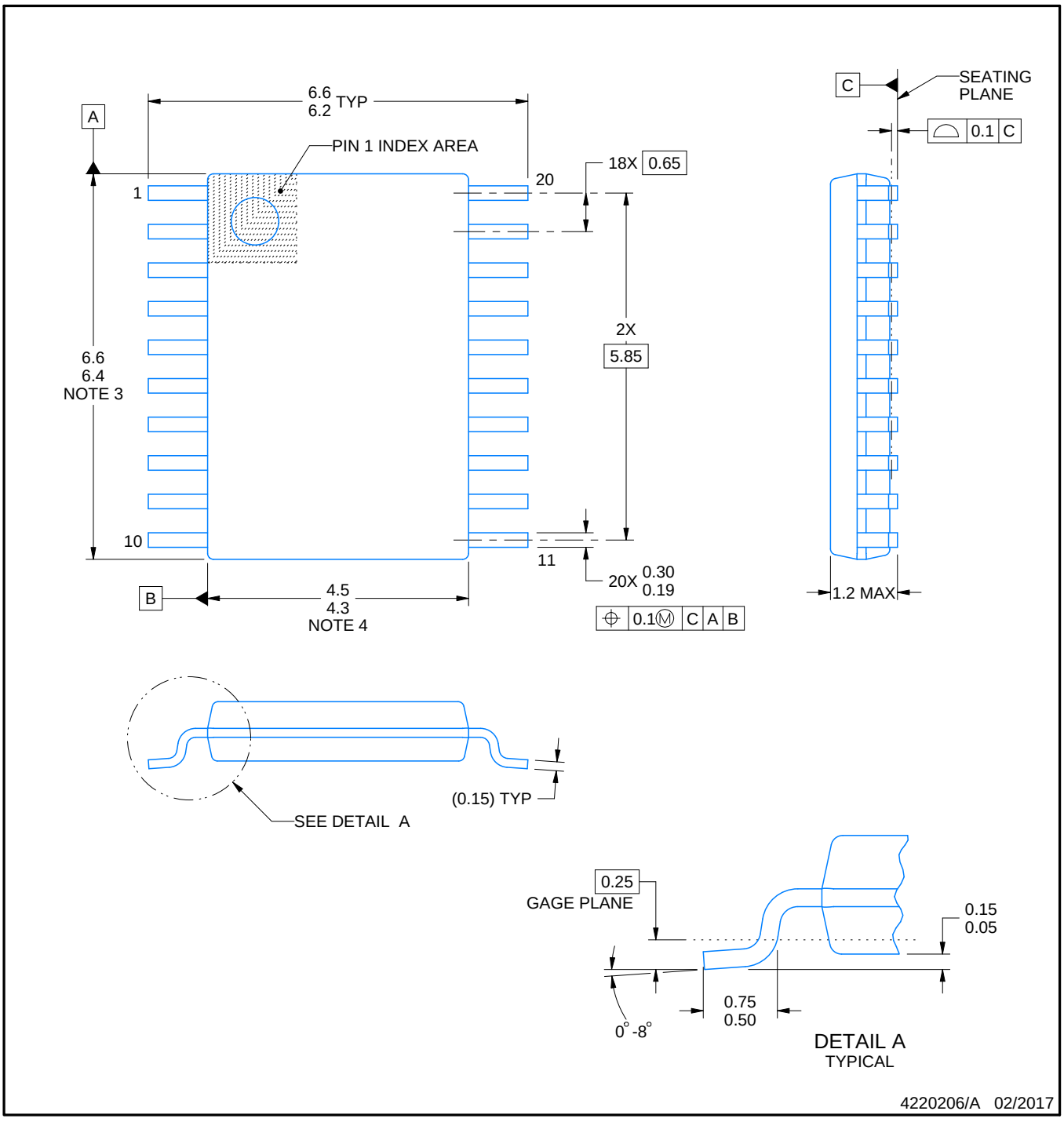
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV8154MPWREP	TSSOP	PW	20	2000	356.0	356.0	35.0

PACKAGE OUTLINE

PW0020A

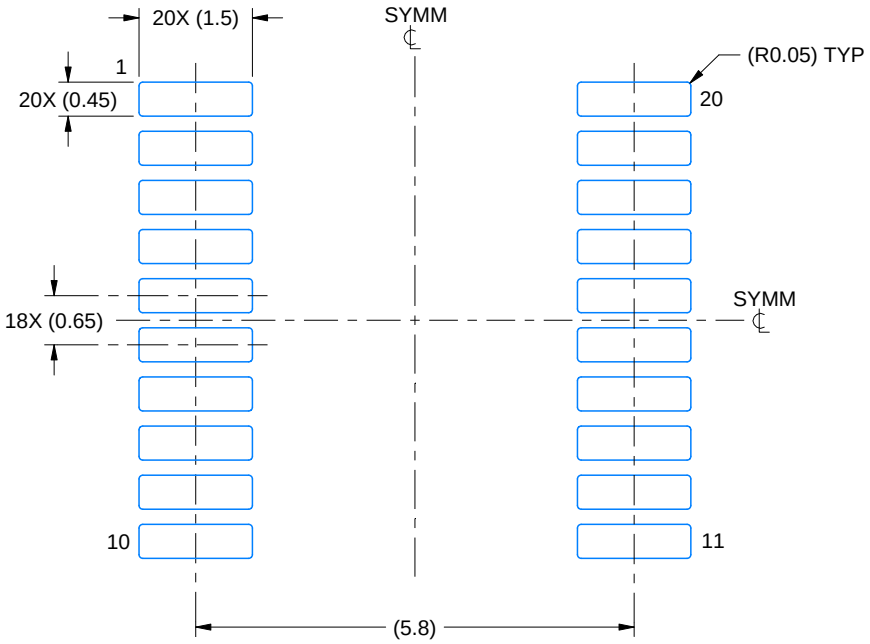
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK DEFINED (PREFERRED)

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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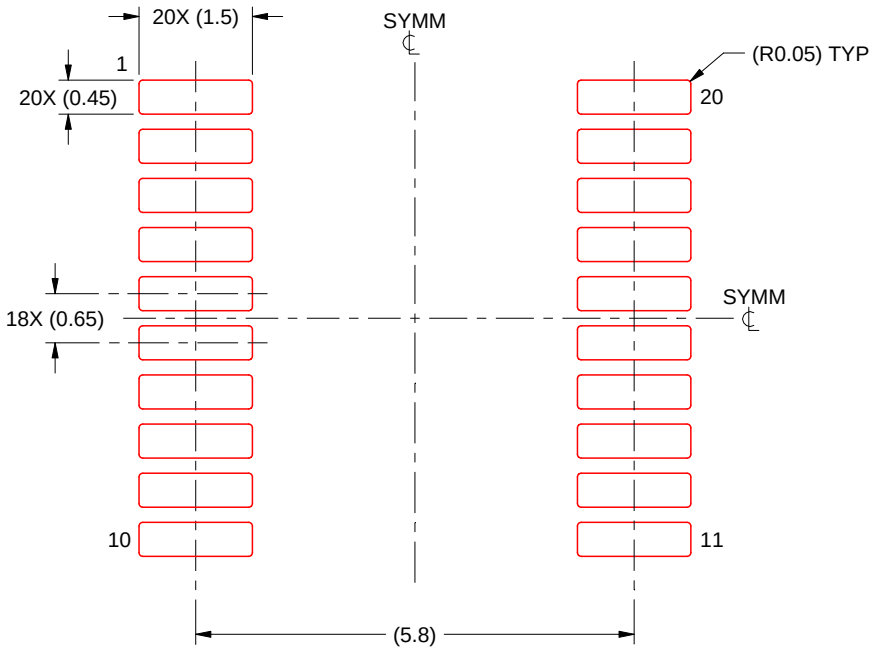
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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