# DUAL-CHANNEL, 16-BIT, 800 MSPS, 2x–8x INTERPOLATING DIGITAL-TO-ANALOG CONVERTER (DAC)

**Check for Samples: DAC5688**

## FEATURES

- **Dual, 16-Bit, 800 MSPS DACs**
- **Dual, 16-Bit, 250 MSPS CMOS Input Data**
  - **16 Sample Input FIFO**
  - **Flexible input data bus options**
- **High Performance**
  - **81 dBc ACLR WCDMA TM1 at 70 MHz**
- **2x-32x Clock Multiplying PLL/VCO**
- **Selectable 2x–8x Interpolation Filters**
  - **Stop-band Attenuation > 80 dB**
- **Complex Mixer with 32-Bit NCO**
- **Digital Quadrature Modulator Correction**
  - **Gain, Phase and Offset Correction**
- **Digital Inverse SINC Filter**
- **3- or 4-Wire Serial Control Interface**
- **On Chip 1.2-V Reference**
- **Differential Scalable Output: 2 to 20 mA**
- **Package: 64-pin 9×9mm QFN**

## APPLICATIONS

- **Cellular Base Stations**
- **Broadband Wireless Access (BWA)**
- **WiMAX 802.16**
- **Fixed Wireless Backhaul**
- **Cable Modem Termination System (CMTS)**

## DESCRIPTION

The DAC5688 is a dual-channel 16-bit 800 MSPS digital-to-analog converter (DAC) with dual CMOS digital data bus, integrated 2x-8x interpolation filters, a fine frequency mixer with 32-bit complex numerically controlled oscillator (NCO), on-board clock multiplier, IQ compensation, and internal voltage reference. Different modes of operation enable or bypass various signal processing blocks. The DAC5688 offers superior linearity, noise, crosstalk and PLL phase noise performance.

The DAC5688 dual CMOS data bus provides 250 MSPS input data transfer per DAC channel. Several input data options are available: dual-bus data, single-bus interleaved data, even and odd multiplexing at half-rate, and an input FIFO with either external or internal clock to ease interface timing. Input data can interpolated 2x, 4x or 8x by on-board digital interpolating FIR filters with over 80 dB of stop-band attenuation.

The DAC5688 allows both complex or real output. An optional 32-bit NCO/mixer in complex mode provides frequency upconversion and the dual DAC output produces a complex Hilbert Transform pair. A digital Inverse SINC filter compensates for natural DAC sin(x)/x frequency roll-off. The digital Quadrature Modulator Correction (QMC) feature allows IQ compensation of phase, gain and offset to maximize sideband rejection and minimize LO feed-through of an external quadrature modulator performing the final single sideband RF up-conversion.

The DAC5688 is pin compatible with the DAC5689 which does not include a clock-multiplying PLL. The DAC5688 is characterized for operation over the industrial temperature range of –40°C to 85°C and is available in a 64-pin 9x9mm QFN package.

### ORDERING INFORMATION[1]

| Order Code T_A = –40°C to 85°C | Package Qty Tape and Reel Format | Package Drawing/Type[2] [3] |
|---|---|---|
| DAC5688IRGCT | 250 | RGC / 64QFN Quad Flatpack No-Lead |
| DAC5688IRGCR | 2000 | |

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) Thermal Pad Size: 7,4 mm × 7,4 mm
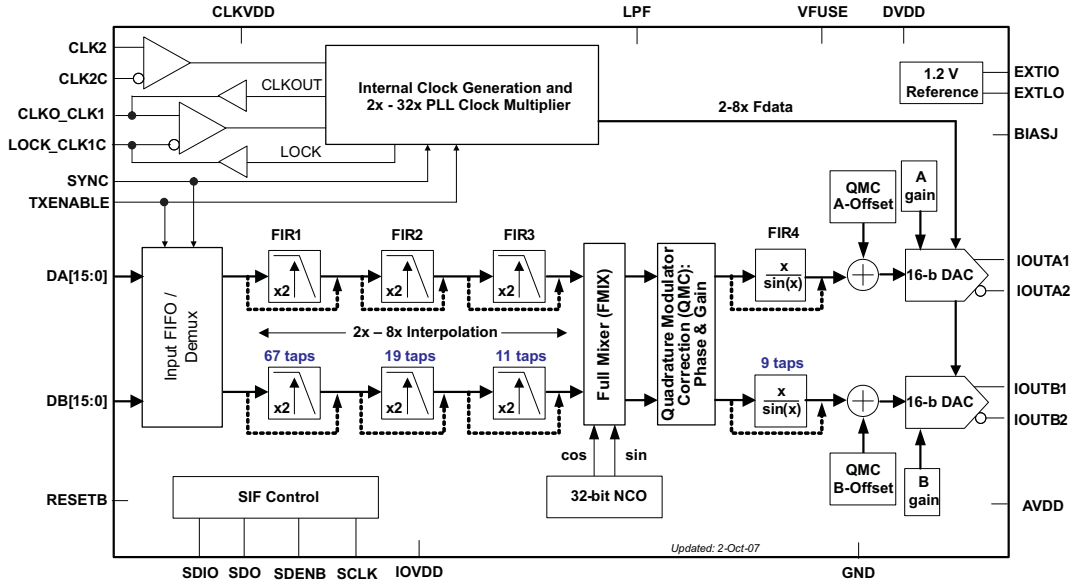(3) MSL Peak Temperature: Level-3-260C-168 HR

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
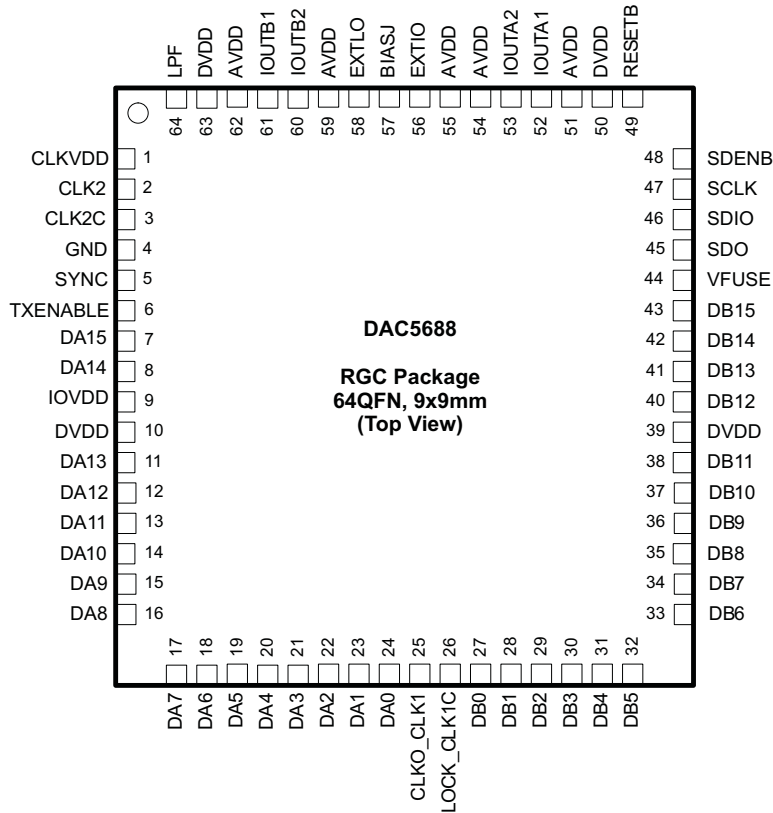
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## FUNCTIONAL BLOCK DIAGRAM



## PINOUT

## PIN FUNCTIONS

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| AVDD | 51, 54, 55, 59, 62 | I | Analog supply voltage. (3.3V) |
| BIASJ | 57 | O | Full-scale output current bias. For 20mA full-scale output current, connect a 960 Ω resistor to GND. |
| CLK2 | 2 | I | With the clock multiplier PLL enabled, CLK2 provides lower frequency reference clock. If the PLL is disabled, CLK2 directly provides clock for DAC up to 800 MHz. |
| CLK2C | 3 | I | Complementary CLK2 input. |
| CLKO_CLK1 | 25 | I/O | In Dual Clock Modes, provides lower frequency input clock (CLK1). Optionally provides clock (CLKO) output for data bus. Internal pull-down. |
| LOCK_ CLK1C | 26 | I/O | Complementary CLK1 signal if configured as a differential input. In PLL mode, optionally outputs PLL lock status. Internal pull-down. |
| CLKVDD | 1 | I | Internal clock buffer supply voltage. (1.8V) It is recommended to isolate this supply from DVDD. |
| DA[15..0] | 7, 8, 11–24 | I | A-Channel Data Bits 0 through 15. DA15 is most significant data bit (MSB) – pin 7 DA0 is least significant data bit (LSB) – pin 24 Internal pull-down. The order of bus can be reversed via CONFIG4 **reva** bit. |
| DB[15..0] | 40–43, 27–38 | I | B-Channel Data Bits 0 through 15. DB15 is most significant data bit (MSB) – pin 43 DB0 is least significant data bit (LSB) – pin 27 Internal pull-down. The order of bus can be reversed via CONFIG4 **revb** bit. |
| DVDD | 10, 39, 50, 63 | I | Digital supply voltage. (1.8V) For best performance it is recommended to isolate pins 10 and 39 from all other 1.8V supplies. |
| EXTIO | 56 | I/O | Used as external reference input when internal reference is disabled (i.e., EXTLO connected to AVDD). Used as internal reference output when EXTLO = GND, requires a 0.1μF decoupling capacitor to GND when used as reference output |
| EXTLO | 58 | O | Connect to GND for internal reference, or AVDD for external reference. |
| GND | 4, Thermal Pad | I | Pin 4 and the Thermal Pad located on the bottom of the QFN package is ground for AVDD, DVDD and IOVDD supplies. |
| IOUTA1 | 52 | O | A-Channel DAC current output. An offset binary data pattern of 0x0000 at the DAC input results in a full scale current sink and the least positive voltage on the IOUTA1 pin. Similarly, a 0xFFFF data input results in a 0 mA current sink and the most positive voltage on the IOUTA1 pin. In single DAC mode, outputs appear on the IOUTA1/A2 pair only. |
| IOUTA2 | 53 | O | A-Channel DAC complementary current output. The IOUTA2 has the opposite behavior of the IOUTA1 described above. An input data value of 0x0000 results in a 0mA sink and the most positive voltage on the IOUTA2 pin. |
| IOUTB1 | 61 | O | B-Channel DAC current output. Refer to IOUTA1 description above. |
| IOUTB2 | 60 | O | B-Channel DAC complementary current output. Refer to IOUTA2 description above. |
| IOVDD | 9 | I | 3.3V supply voltage for all digital I/O. Note: This supply input should remain at 3.3V regardless of the 1.8V or 3.3V selectable digital input switching thresholds via CONFIG26 **io_1p8_3p3**. |
| LPF | 64 | I | PLL loop filter connection. If not using the clock multiplying PLL, leave the LPF pin open. Set **PLL_sleep** and clear **PLL_ena** control bits for reduced power dissipation. |
| SYNC | 5 | I | Optional SYNC input for internal clock dividers, FIFO, NCO and QMC blocks. Internal pull-down. |
| RESETB | 49 | I | Resets the chip when low. Internal pull-up. |
| SCLK | 47 | I | Serial interface clock. Internal pull-down. |
| SDENB | 48 | I | Active low serial data enable, always an input to the DAC5688. Internal pull-up. |
| SDIO | 46 | I/O | Bi-directional serial data in 3-pin mode (default). In 4-pin interface mode (CONFIG5 **sif4**), the SDIO pin is an input only. Internal pull-down. |
| SDO | 45 | O | Uni-directional serial interface data in 4-pin mode (CONFIG5 **sif4**). The SDO pin is tri-stated in 3-pin interface mode (default). Internal pull-down. |
| TXENABLE | 6 | I | Transmit enable input. Internal pull-down. TXENABLE has two purposes. In all modes, TXENABLE must be high for the DATA to the DAC to be enabled. When TXENABLE is low, the digital logic section is forced to all 0, and any input data is ignored. In interleaved data mode, TXENABLE can be used to synchronize the data to channels A and B. The first A-channels sample should be aligned with the rising edge of TXENABLE. |
| VFUSE | 44 | I | Digital supply voltage. (1.8V) This supply pin is also used for factory fuse programming. **Connect to DVDD pins for normal operation.** |

# DAC5688

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

| | | VALUE | UNIT |
|---|---|---|---|
| Supply Voltage Range | DVDD[2] | −0.5 to 2.3 | V |
| | VFUSE[2] | −0.5 to 2.3 | V |
| | CLKVDD[2] | −0.5 to 2.3 | V |
| | AVDD[2] | −0.5 to 4 | V |
| | IOVDD[2] | −0.5 to 4 | V |
| Supply Voltage Range | AVDD to DVDD | −2 to 2.6 | V |
| | CLKVDD to DVDD | −0.5 to 0.5 | V |
| | IOVDD to AVDD | −0.5 to 0.5 | V |
| | CLK2, CLK2C[2] | −0.5 to CLKVDD + 0.5 | V |
| | CLKO_CLK1, LOCK_CLK1C, SLEEP, TXENABLE[2] | −0.5 to IOVDD + 0.5 | V |
| | DA[15..0] ,DB[15..0] [2] | −0.5 to IOVDD + 0.5 | V |
| | SDO, SDIO, SCLK, SDENB, RESETB [2] | −0.5 to IOVDD + 0.5 | V |
| | IOUTA1/B1, IOUTA2/B2 [2] | −0.5 to AVDD + 0.5 | V |
| | LPF, EXTIO, EXTLO, BIASJ [2] | −0.5 to AVDD + 0.5 | V |
| Peak input current (any input) | | 20 mA | mA |
| Peak total input current (all inputs) | | −30 mA | mA |
| Operating free-air temperature range, $T_A$: DAC5688I | | −40 to 85 | °C |
| Storage temperature range | | −65 to 150 | °C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured with respect to GND.

## THERMAL INFORMATION

| THERMAL CONDUCTIVITY | | DAC5688 | UNITS |
|---|---|---|---|
| | | 64ld QFN | |
| $T_J$ | Maximum junction temperature [1][2] | 125 | °C |
| $\theta_{JA}$ | Theta junction-to-ambient thermal resistance (still air) | 22 | °C/W |
| | Theta junction-to-ambient thermal resistance (200 lfm) | 15 | |
| $\psi_{JT}$ | Psi junction-to-top of package characterization parameter | 0.2 | |
| $\theta_{JB}$ | Theta junction-to-board characterization parameter | 3.5 | |

(1) Air flow or heat sinking reduces $\theta_{JA}$ and may be required for sustained operation at 85°C under maximum operating conditions.
(2) It is strongly recommended to solder the device thermal pad to the board ground plane.

Product Folder Link(s): *DAC5688*

## ELECTRICAL CHARACTERISTICS (DC SPECIFICATIONS)

over recommended operating free-air temperature range, AVDD, IOVDD = 3.3 V, DVDD, CLKVDD = 1.8 V, $IOUT_{FS}$ = 20 mA

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **RESOLUTION** | | | 16 | | | Bits |
| **DC ACCURACY** | | | | | | |
| INL | Integral nonlinearity | 1 LSB = $IOUT_{FS}/2^{16}$ | | ±4 | | LSB |
| DNL | Differential nonlinearity | | | ±2 | | LSB |
| **ANALOG OUTPUT** | | | | | | |
| | Coarse gain linearity | | | ± 0.04 | | LSB |
| | Offset error mid code offset | | | 0.01 | | %FSR |
| | Gain error | With external reference | | 1 | | %FSR |
| | | With internal reference | | 0.7 | | %FSR |
| | Gain mismatch | With internal reference, dual DAC mode | −2 | | 2 | %FSR |
| | Minimum full scale output current | Nominal full-scale current, $IOUT_{FS}$ = 16 × IBIAS current. | | 2 | | mA |
| | Maximum full scale output current | | | 20 | | |
| | Output compliance range[1] | $IOUT_{FS}$ = 20 mA | AVDD − 0.5V | | AVDD + 0.5V | V |
| | Output resistance | | | 300 | | kΩ |
| | Output capacitance | | | 5 | | pF |
| **REFERENCE OUTPUT** | | | | | | |
| $V_{REF}$ | Reference output voltage | Internal Reference Mode | 1.14 | 1.2 | 1.26 | V |
| | Reference output current[2] | | | 100 | | nA |
| **REFERENCE INPUT** | | | | | | |
| $V_{EXTIO}$ | Input voltage range | External Reference Mode | 0.1 | | 1.25 | V |
| | Input resistance | | | 1 | | MΩ |
| | Small signal bandwidth | CONFIG26: isbiaslpf_a and isbiaslpf_b = 0 | | 95 | | kHz |
| | | CONFIG26: isbiaslpf_a and isbiaslpf_b = 1 | | 472 | | |
| | Input capacitance | | | 100 | | pF |
| **TEMPERATURE COEFFICIENTS** | | | | | | |
| | Offset drift | | | ±1 | | ppm of FSR/°C |
| | Gain drift | With external reference | | ±15 | | |
| | | With internal reference | | ±30 | | |
| | Reference voltage drift | | | ±8 | | ppm/°C |
| **POWER SUPPLY** | | | | | | |
| | AVDD, IOVDD | | 3.0 | 3.3 | 3.6 | V |
| | DVDD, CLKVDD | | 1.7 | 1.8 | 1.9 | V |
| PSRR | Power supply rejection ratio | | | ±0.2 | | %FSR/V |
| P | AVDD + IOVDD current, 3.3V | **Mode 1:** ×8 Interp, PLL on, QMC = off, ISINC = off, DAC A+B on, $F_{IN}$ = 5 MHz Tone, NCO = 145 MHz, $F_{OUT}$ = 150 MHz, $F_{DAC}$ = 500 MHz | | 150 | | mA |
| | DVDD + CLKVDD current, 1.8V | | | 450 | | mA |
| | Power Dissipation | | | 1300 | | mW |
| | AVDD + IOVDD current, 3.3V | **Mode 2:** ×8 Interp, PLL off, QMC = on, ISINC = on, DAC A+B on, $F_{IN}$ = 5 MHz Tone, NCO = 91 MHz $F_{OUT}$ = 96 MHz, $F_{DAC}$ = 614.4 MHz | | 140 | | mA |
| | DVDD + CLKVDD current, 1.8V | | | 520 | | mA |
| | Power Dissipation | | | 1400 | | mW |
| | AVDD + IOVDD current, 3.3V | **Mode 3 (Max):** ×4 Interp, PLL on, QMC = on, ISINC = on, DAC A+B on, $F_{IN}$ = 5 MHz Tone, NCO = 135 MHz, $F_{OUT}$ = 140 MHz, $F_{DAC}$ = 800 MHz | | 150 | | mA |
| | DVDD + CLKVDD current, 1.8V | | | 700 | | mA |
| | Power Dissipation | | | 1750 | 1950 | mW |
| | AVDD + IOVDD current, 3.3V | **Mode 4 (Sleep):** ×8 Interp, PLL off, QMC = off, ISINC = off, DAC A+B off, $F_{IN}$ = 5 MHz Tone, NCO = off, $F_{OUT}$ = off, $F_{DAC}$ = 800 MHz, | | 12 | | mA |
| | DVDD + CLKVDD current, 1.8V | | | 15 | | mA |
| | Power Dissipation | | | 65 | 100 | mW |

(1)  The upper limit of the output compliance is determined by the CMOS process. Exceeding this limit may result in transistor breakdown, resulting in reduced reliability of the DAC5688 device. The lower limit of the output compliance is determined by the load resistors and full-scale output current. Exceeding the upper limit adversely affects distortion performance and integral nonlinearity.

(2)  Use an external buffer amplifier with high impedance input to drive any external load.

## ELECTRICAL CHARACTERISTICS (AC SPECIFICATIONS)

Over recommended operating free-air temperature range, AVDD, IOVDD = 3.3 V, DVDD, CLKVDD = 1.8 V, $IOUT_{FS}$ = 20 mA

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **ANALOG OUTPUT**[1] | | | | | | | |
| $f_{DAC}$ | Maximum output update rate | | | 800 | | | MSPS |
| $t_{s(DAC)}$ | Output settling time to 0.1% | Transition: Code 0x0000 to 0xFFFF | | | 10.4 | | ns |
| $t_{pd}$ | Output propagation delay | DAC outputs are updated on falling edge of DAC clock. Does not include Digital Latency (see below). | | | 2 | | ns |
| $t_{r(IOUT)}$ | Output rise time | 10% to 90% | | | 220 | | ps |
| $t_{f(IOUT)}$ | Output fall time | 90% to 10% | | | 220 | | ps |
| Digital Latency | | No Interp, NCO off, QMC off, ISINC = off | | | 109 | | DAC clock cycles |
| | | **x2** Interpolation, NCO off, QMC off, ISINC = off | | | 172 | | |
| | | **x4** Interpolation, NCO off, QMC off, ISINC = off | | | 276 | | |
| | | **x8** Interpolation, NCO off, QMC off, ISINC = off | | | 488 | | |
| | | x8 Interpolation, NCO **on**, QMC off, ISINC = off | | | 512 | | |
| | | x8 Interpolation, NCO on, QMC **on**, ISINC = off | | | 528 | | |
| | | x8 Interpolation, NCO on, QMC on, ISINC = **on** | | | 548 | | |
| **AC PERFORMANCE** [2] | | | | | | | |
| SFDR | Spurious free dynamic range | ×4 Interp, PLL off, CLK2 = 800 MHz, DAC A+B on, 0 dBFS Single tone, $F_{OUT}$ = $F_{IN}$ First Nyquist Zone < $f_{DATA}$/2 | $F_{OUT}$= 10.1 MHz | | 83 | | dBc |
| | | | $F_{OUT}$= 20.1 MHz | | 79 | | |
| SNR | Signal-to-Noise Ratio | ×4 Interp, PLL off, CLK2 = 800 MHz, DAC A+B on, 0 dBFS Single tone, $F_{IN}$ = 10.1 MHz, $F_{OUT}$ = $F_{IN}$ + NCO | NCO= 10 MHz, $F_{OUT}$= 20.1 MHz | | 72 | | dBc |
| | | | NCO= 60 MHz, $F_{OUT}$= 70.1 MHz | | 68 | | |
| | | | NCO= 140 MHz, $F_{OUT}$= 150.1 MHz | | 64 | | |
| | | | NCO= 290 MHz, $F_{OUT}$= 300.1 MHz | | 57 | | |
| IMD3 | Third-order Two-Tone intermodulation (Each tone at –6 dBFS) | ×4 Interp, PLL off, CLK2 = 800 MHz, DAC A+B on, $F_{IN}$ = 10.5 and 11. 5 MHz, $F_{OUT}$ = $F_{IN}$ + NCO | NCO= 40 MHz, $F_{OUT}$= 51±0.5 MHz | | 85 | | dBc |
| | | | NCO= 60 MHz, $F_{OUT}$= 71±0.5 MHz | | 83 | | |
| | | | NCO= 130 MHz, $F_{OUT}$= 141±0.5 MHz | | 74 | | |
| IMD | Four-tone Intermodulation to Nyquist (Each tone at –12 dBFS) | ×4 Interp, PLL off, CLK2 = 800 MHz, DAC A+B on, $F_{IN}$ = 9.8, 10.4, 11.6 and 12.2 MHz (600kHz spacing), NCO = 129 MHz, $F_{OUT}$ = $F_{IN}$ + NCO = 140±1.2 MHz | | | 73 | | dBc |
| ACLR [3] | Adjacent Channel Leakage Ratio | ×8 Interp, PLL off, CLK2 = 737.28 MHz, DAC A+B on, $F_{IN}$ = 23 .04 MHz, NCO = off | Single Carrier, $F_{OUT}$ = 23.04 MHz | | 81 | | dBc |
| | | ×8 Interp, PLL off, CLK2 = 737.28 MHz, DAC A+B on, $F_{IN}$ = Baseband I/Q, $F_{OUT}$ = NCO | Single Carrier, $F_{OUT}$ = 70MHz | | 81 | | |
| | | | Single Carrier, $F_{OUT}$ = 140MHz | | 78 | | |
| | | | Four Carrier, $F_{OUT}$ = 140MHz | | 70 | | |
| | Noise Floor, Noise Spectral Density (NSD) [3] | ×8 Interp, PLL off, CLK2 = 737.28 MHz, DAC A+B on, $F_{IN}$ = $F_{OUT}$ = Baseband I/Q, 50 MHz offset, 1 MHz BW | Single Carrier Noise Floor | | 101 | | dBm |
| | | | Single Carrier NSD in 1 MHz BW | | 161 | | dBm/Hz |
| | | | Four Carrier Noise Floor | | 101 | | dBm |
| | | | Four Carrier NSD in 1 MHz BW | | 161 | | dBm/Hz |

(1)  Measured differential across IOUTA1 and IOUTA2 or IOUTB1 and IOUTB2 with 25 Ω each to AVDD.
(2)  4:1 transformer output termination, 50Ω doubly terminated load
(3)  W-CDMA with 3.84 MHz BW, 5-MHz spacing, centered at IF. TESTMODEL 1, 10 ms

Product Folder Link(s): DAC5688

## ELECTRICAL CHARACTERISTICS (DIGITAL SPECIFICATIONS)

Over recommended operating free-air temperature range, AVDD, IOVDD = 3.3V, DVDD, CLKVDD = 1.8V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **CMOS INTERFACE: SDO, SDIO, SCLK, SDENB, RESETB, DA[15:0], DB[15:0], SYNC, TXENABLE, CLKO_CLK1, LOCK_CLK1C** | | | | | | |
| $V_{IH}$ | High-level input voltage | CONFIG26 **io_1p8_3p3** = 0 (3.3V levels) | 2.30 | | | V |
| | | CONFIG26 **io_1p8_3p3** = 1 (1.8V levels) | 1.25 | | | |
| $V_{IL}$ | Low-level input voltage | CONFIG26 **io_1p8_3p3** = 0 (3.3V levels) | | | 1.00 | V |
| | | CONFIG26 **io_1p8_3p3** = 1 (1.8V levels) | | | 0.54 | |
| $I_{IH}$ | High-level input current | | | ±20 | | µA |
| $I_{IL}$ | Low-level input current | | | ±20 | | µA |
| $C_I$ | CMOS Input capacitance | | | 2 | | pF |
| $V_{OH}$ | SDO, SDIO | $I_{LOAD}$ = −100 µA | IOVDD − 0.2 | | | V |
| | SDO, SDIO | $I_{LOAD}$ = −2 mA | 0.8 × IOVDD | | | |
| $V_{OL}$ | SDO, SDIO | $I_{LOAD}$ = 100 µA | | | 0.2 | V |
| | SDO, SDIO | $I_{LOAD}$ = 2 mA | | | 0.5 | |
| | Input data rate | | 0 | | 250 | MSPS |
| $t_{s(SDENB)}$ | Setup time, SDENB to rising edge of SCLK | | 20 | | | ns |
| $t_{s(SDIO)}$ | Setup time, SDIO valid to rising edge of SCLK | | 10 | | | ns |
| $t_{h(SDIO)}$ | Hold time, SDIO valid to rising edge of SCLK | | 5 | | | ns |
| $t_{SCLK}$ | Period of SCLK | | 100 | | | ns |
| $t_{SCLKH}$ | High time of SCLK | | 40 | | | ns |
| $t_{SCLK}$ | Low time of SCLK | | 40 | | | ns |
| $t_{d(Data)}$ | Data output delay after falling edge of SCLK | | | 10 | | ns |
| $t_{RESET}$ | Minimum RESETB pulse width | | | 25 | | ns |
| **TIMING PARALLEL DATA INPUT: (DUAL CLOCK and DUAL SYNCHRONOUS CLOCK MODES: Figure 32)** | | | | | | |
| $t_s$ | Setup time | CLK1/C = input | 1 | | | ns |
| $t_h$ | Hold time | | 1 | | | ns |
| t_align | Max timing offset between CLK1 and CLK2 rising edges | DUAL SYNCHRONOUS BUS MODE only (Typical characteristic) | $\dfrac{1}{2f_{CLK2}} - 0.55$ | | | ns |
| **TIMING PARALLEL DATA INPUT (EXTERNAL CLOCK MODE: Figure 33 and PLL CLOCK MODE: Figure 34)** | | | | | | |
| $t_s$ | Setup time | CLKO_CLK1 = input or output. Note: Delay time increases with higher capacitive loads. | 1 | | | ns |
| $t_h$ | Hold time | | 1 | | | ns |
| $t_{d(CLKO)}$ | Delay time | | | 4.5 | | ns |
| **CLOCK INPUT (CLK2/CLK2C)** | | | | | | |
| | CLK2/C Duty cycle | | 40% | | 60% | |
| | CLK2/C Differential voltage[1] | | 0.4 | 1 | | V |
| | CLK2/C Input common mode | | | 2/3 × CLKVDD | | V |
| | CLK2C Input Frequency | | | | 800 | MHz |
| **CLOCK INPUT (CLK1/CLK1C)** | | | | | | |
| | CLK1/C Duty cycle | | 40% | | 60% | |
| | CLK1/C Differential voltage | | 0.4 | 1.0 | | V |
| | CLK1/C Input common mode | | | IOVDD /2 | | V |
| | CLK1/C Input Frequency | | | | 250 | MHz |
| **CLOCK OUTPUT (CLKO)** | | | | | | |
| | CLKO Output Frequency[2] | with 3pF load | | | 160 | MHz |

(1)   Driving the clock input with a differential voltage lower than 1V will result in degraded performance.
(2)   Specified by design and simulation. Not production tested. It is recommended to buffer CLKO.

## ELECTRICAL CHARACTERISTICS (DIGITAL SPECIFICATIONS)

Over recommended operating free-air temperature range, AVDD, IOVDD = 3.3V, DVDD, CLKVDD = 1.8V.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| **PHASE LOCKED LOOP** | | | | | |
| Phase noise at 600 kHz offset | 100 MHz, 0-dBFS tone, $f_{DATA}$ = 200 MSPS, CLK2/C = 200 MHz, **PLL_m** = '00111', **PLL_n** = '001', (M/N=4) **PLL_gain** = '11', **PLL_range** = '1000' (8) x4 Interpolation | | −125 | | dBc/ Hz |
| Phase noise at 6 MHz offset | | | −146 | | |
| PLL/VCO Operating Frequency, Typical VCO Gain | **PLL_gain** = '00', **PLL_range** = '0000' (0) | 140 | | 270 | MHz |
| | | | 215 | | MHz/V |
| | **PLL_gain** = '01', **PLL_range** = '0001' (1) | 270 | | 440 | MHz |
| | | | 290 | | MHz/V |
| | **PLL_gain** = '01', **PLL_range** = '0010' (2) | 370 | | 490 | MHz |
| | | | 255 | | MHz/V |
| | **PLL_gain** = '01', **PLL_range** = '0011' (3) | 450 | | 530 | MHz |
| | | | 230 | | MHz/V |
| | **PLL_gain** = '10', **PLL_range** = '0100' (4) | 530 | | 650 | MHz |
| | | | 285 | | MHz/V |
| | **PLL_gain** = '10', **PLL_range** = '0101' (5) | 600 | | 680 | MHz |
| | | | 260 | | MHz/V |
| | **PLL_gain** = '10', **PLL_range** = '0110' (6) | 660 | | 720 | MHz |
| | | | 245 | | MHz/V |
| | **PLL_gain** = '10', **PLL_range** = '0111' (7) | 710 | | 750 | MHz |
| | | | 230 | | MHz/V |
| | **PLL_gain** = '11', **PLL_range** = '1000' (8) | 750 | | 830 | MHz |
| | | | 275 | | MHz/V |
| | **PLL_gain** = '11', **PLL_range** = '1001' (9) | 800 | | 860 | MHz |
| | | | 260 | | MHz/V |
| | **PLL_gain** = '11', **PLL_range** = '1010' (A) | 840 | | 890 | MHz |
| | | | 245 | | MHz/V |
| | **PLL_gain** = '11', **PLL_range** = '1011' (B) | 880 | | 910 | MHz |
| | | | 235 | | MHz/V |
| PFD Maximum Frequency | | | 160 | | MHz |

## TYPICAL CHARACTERISTICS
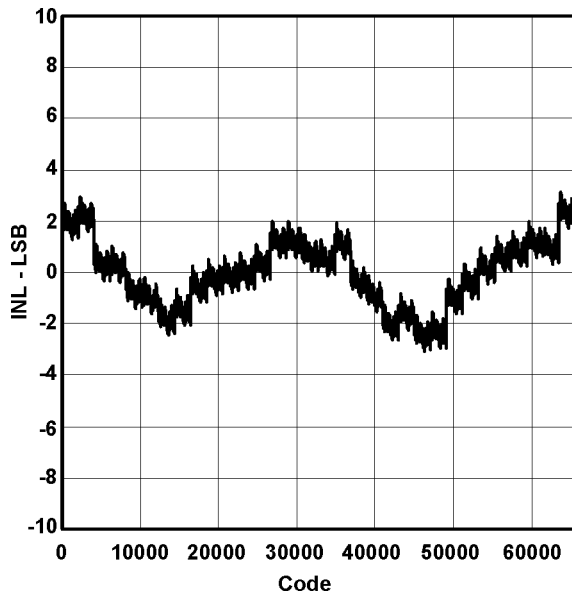


Figure 1. Integral Nonlinearity
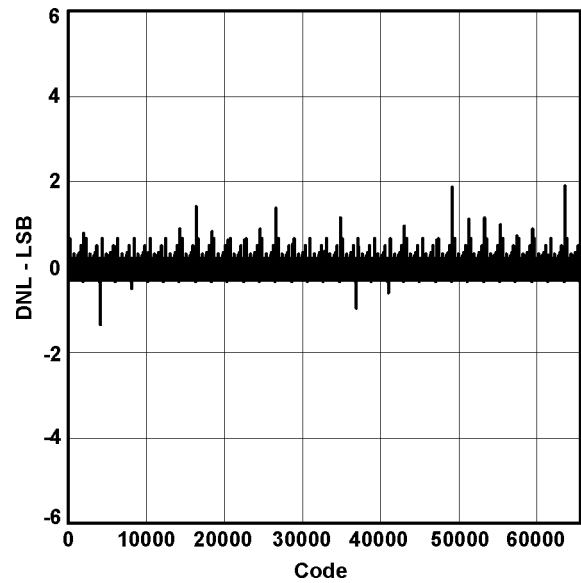


Figure 2. Differential Nonlinearity



Fdata = 200 MSPS, IQ
$F_{IN}$ = 20 MHz Complex
IF = 20 MHz
x4 Interpolation
PLL off
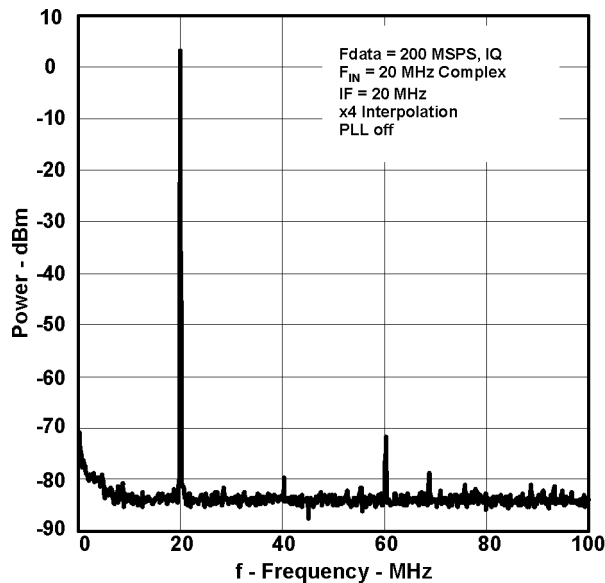
Figure 3. Single Tone Spectral Plot



Fdata = 200 MSPS, IQ
$F_{IN}$ = 0 MHz Complex
IF = 140 MHz
x4 Interpolation, FMIX
PLL off
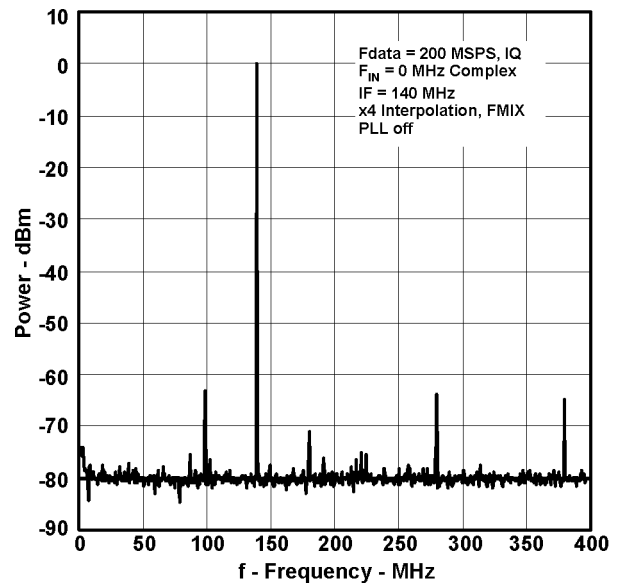
Figure 4. Single Tone Spectral Plot

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**TEXAS INSTRUMENTS**

## TYPICAL CHARACTERISTICS (continued)
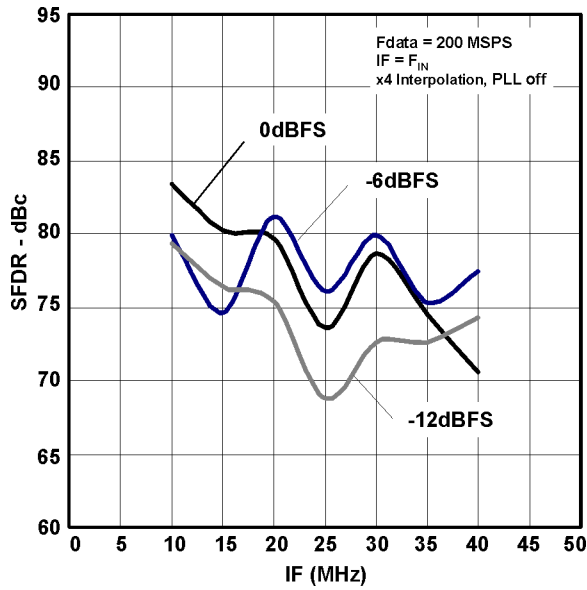


Figure 5. In-Band SFDR vs. Intermediate Frequency
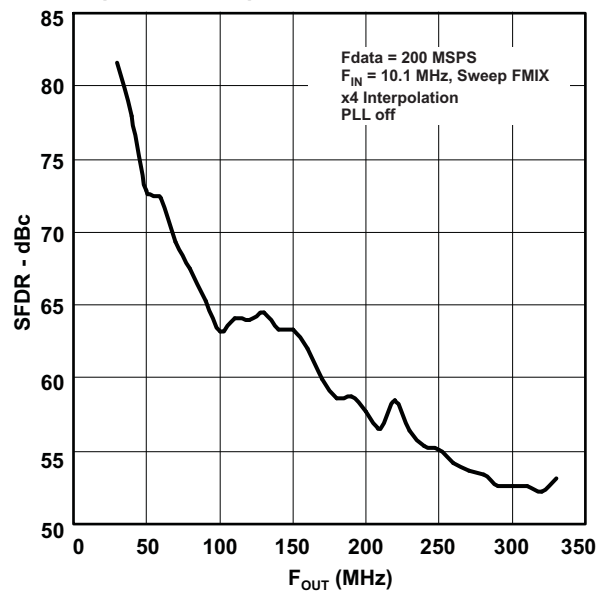


Figure 6. Out-Of-Band SFDR vs Intermediate Frequency
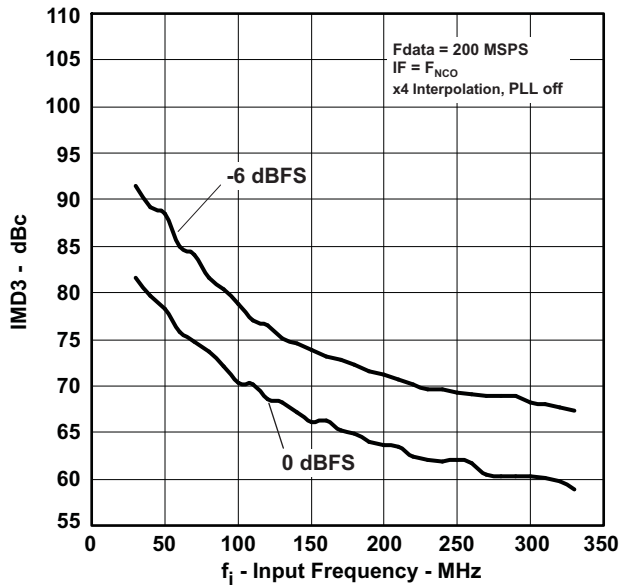


Figure 7. Two Tone IMD vs Intermediate Frequency
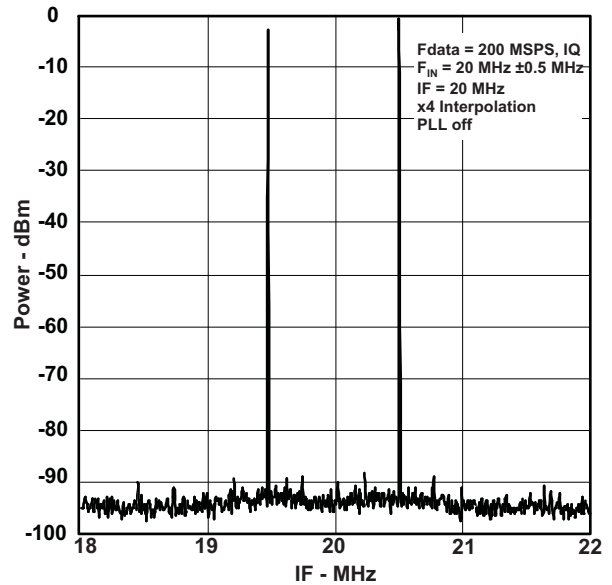


Figure 8. Two Tone IMD Spectral Plot

Product Folder Link(s): DAC5688

## TYPICAL CHARACTERISTICS (continued)
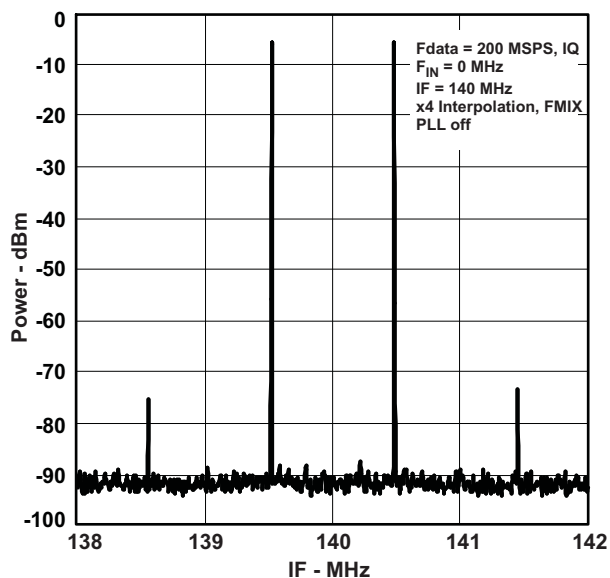


Figure 9. Two Tone IMD Spectral Plot
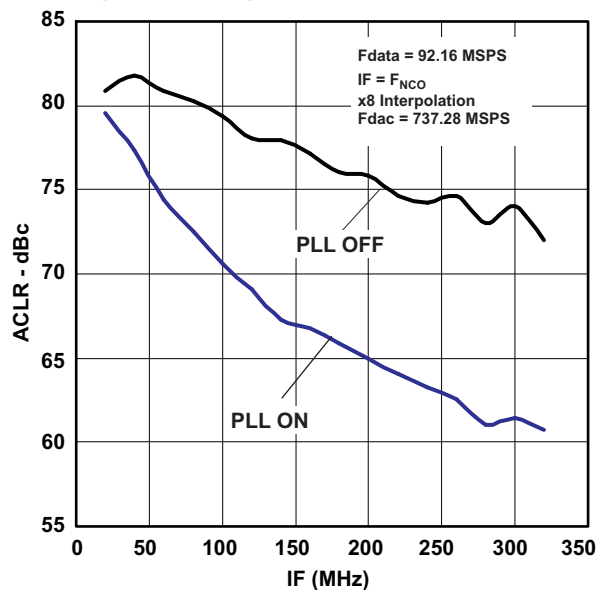


Figure 10. WCDMA ACLR vs Intermediate Frequency
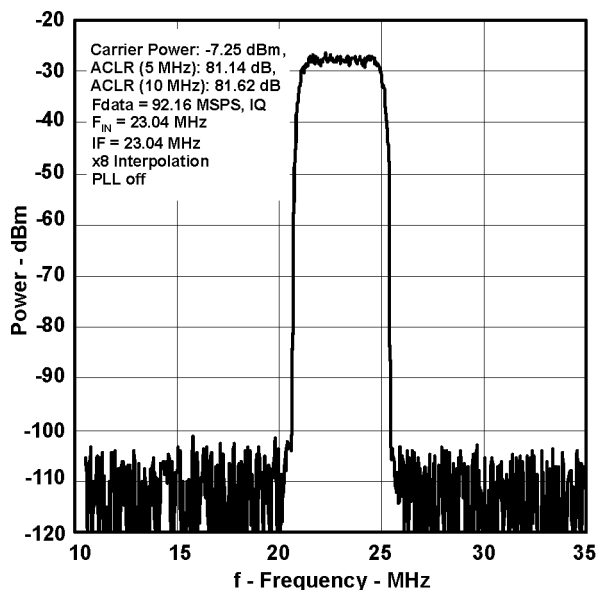


Figure 11. WCDMA TM1:Single Carrier, PLL Off
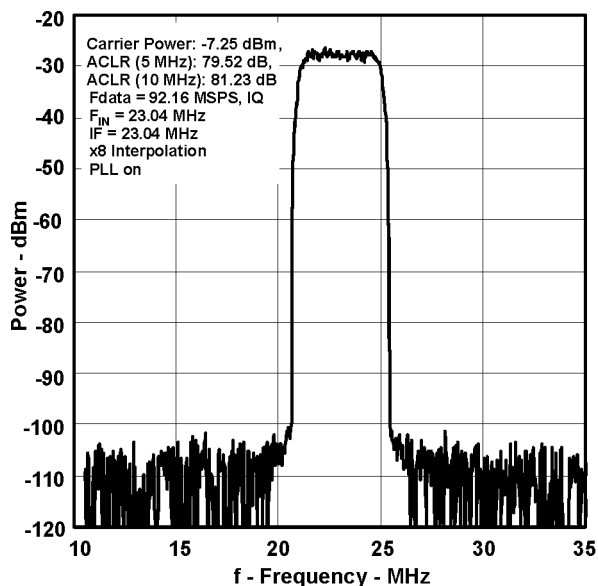


Figure 12. WCDMA TM1:Single Carrier, PLL On

Product Folder Link(s): DAC5688

# TYPICAL CHARACTERISTICS (continued)

Carrier Power: -11.05 dBm,
ACLR (5 MHz): 77.75 dB,
ACLR (10 MHz): 80.09 dB
Fdata = 92.16 MSPS, IQ
$F_{IN}$ = 0 MHz
IF = 140 MHz
x8 Interpolation, FMIX
PLL Off
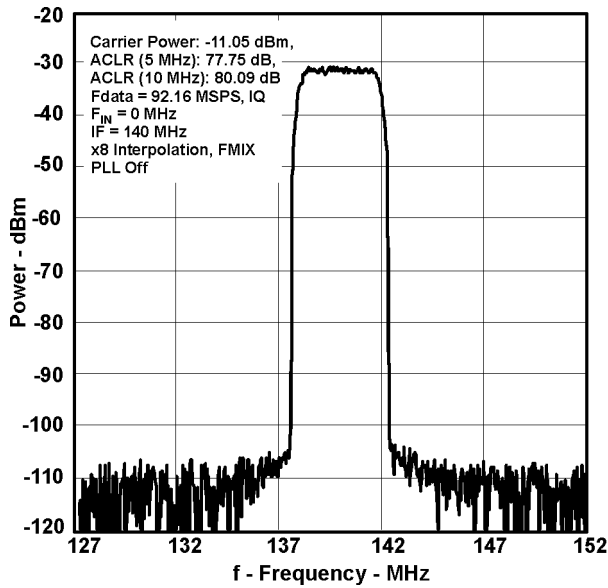
Figure 13. WCDMA TM1:Single Carrier, PLL Off

Carrier Power: -11.07 dBm,
ACLR (5 MHz): 66.79 dB,
ACLR (10 MHz): 74.59 dB
Fdata = 92.16 MSPS, IQ
$F_{IN}$ = 0 MHz
IF = 140 MHz
x8 Interpolation, FMIX
PLL on
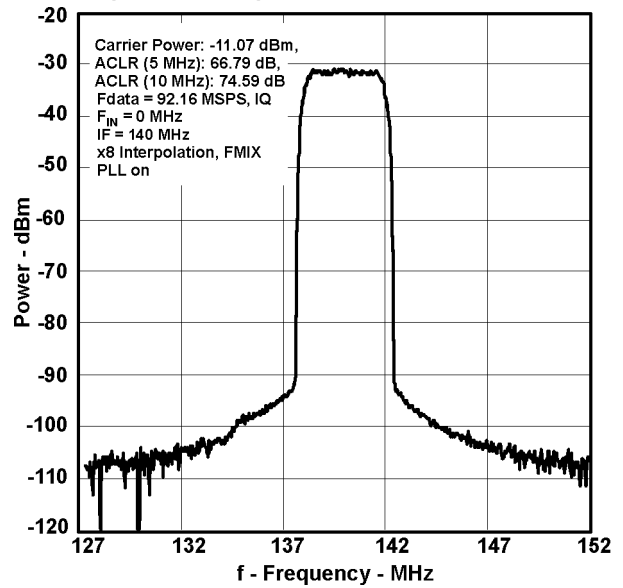
Figure 14. WCDMA TM1:Single Carrier, PLL On

Carrier Power: -11.85 dBm,
ACLR (5 MHz): 74.22 dB,
ACLR (10 MHz): 75.42 dB

Fdata = 92.16 MSPS, IQ
$F_{IN}$ = 0 MHz
IF = 140 MHz
x8 Interpolation, FMIX
PLL Off
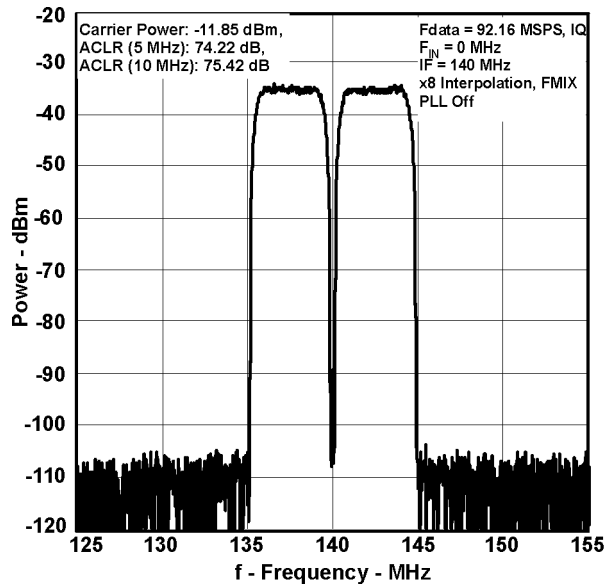
Figure 15. WCDMA TM1:Two Carriers, PLL Off

Carrier Power: -11.86 dBm
ACLR (5 MHz): 66.26 dBm
ACLR (10 MHz): 72.06 dBm

Fdata = 92.16 MSPS, IQ
$F_{IN}$ = 0 MHz
IF = 140 MHz
x8 Interpolation, FMIX
PLL on
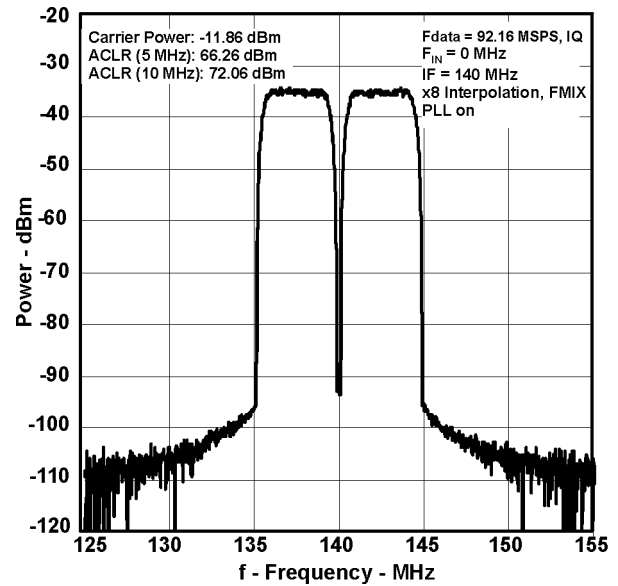
Figure 16. WCDMA TM1:Two Carriers, PLL On

Product Folder Link(s): DAC5688

## TYPICAL CHARACTERISTICS (continued)
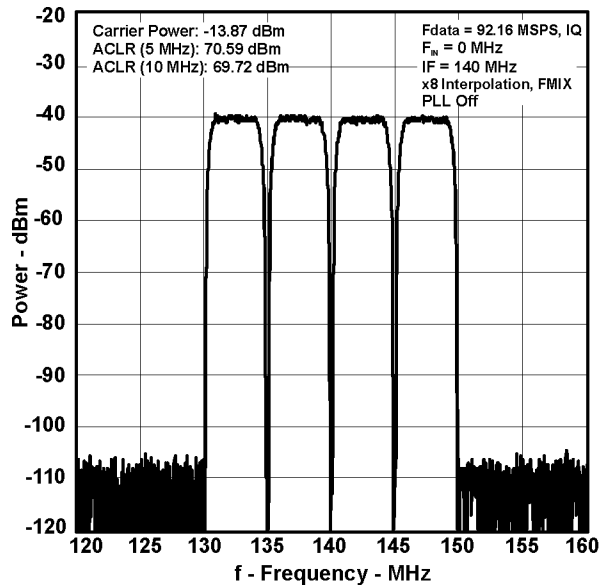


Figure 17. WCDMA TM1:Four Carriers, PLL Off
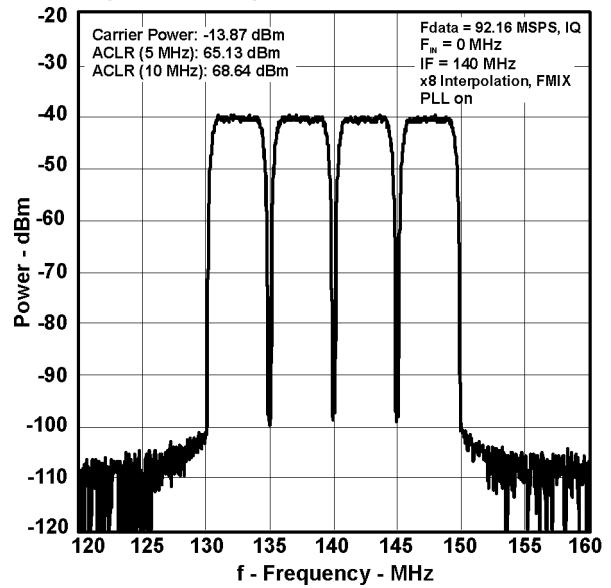


Figure 18. WCDMA TM1:Four Carriers, PLL On

Product Folder Link(s): DAC5688

## TEST METHODOLOGY

Typical AC specifications were characterized with the DAC5688EVM. A sinusoidal master clock frequency is generated by an HP8665B signal generator which drives an Agilent 8133A pulse generator to generate a square wave output clock for the TSW3100 Pattern Generator and EVM input clock. On the EVM, the input clock is driven by an CDCM7005 clock distribution chip that is configured to simply buffer the external clock or divide it down for necessary test configurations.

The DAC5688 output is characterized with a Rohde and Schwarz FSU spectrum analyzer. For WCDMA signal characterization, it is important to use a spectrum analyzer with high IP3 and noise subtraction capability so that the spectrum analyzer does not limit the ACPR measurement.

## DEFINITION OF SPECIFICATIONS

**Adjacent Carrier Leakage Ratio (ACLR):** Defined for a 3.84Mcps 3GPP W-CDMA input signal measured in a 3.84MHz bandwidth at a 5MHz offset from the carrier with a 12dB peak-to-average ratio.

**Analog and Digital Power Supply Rejection Ratio (APSRR, DPSRR):** Defined as the percentage error in the ratio of the delta IOUT and delta supply voltage normalized with respect to the ideal IOUT current.

**Differential Nonlinearity (DNL):** Defined as the variation in analog output associated with an ideal 1 LSB change in the digital input code.

**Gain Drift:** Defined as the maximum change in gain, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

**Gain Error:** Defined as the percentage error (in FSR%) for the ratio between the measured full-scale output current and the ideal full-scale output current.

**Integral Nonlinearity (INL):** Defined as the maximum deviation of the actual analog output from the ideal output, determined by a straight line drawn from zero scale to full scale.

**Intermodulation Distortion (IMD3, IMD):** The two-tone IMD3 or four-tone IMD is defined as the ratio (in dBc) of the worst 3rd-order (or higher) intermodulation distortion product to either fundamental output tone.

**Offset Drift:** Defined as the maximum change in DC offset, in terms of ppm of full-scale range (FSR) per °C, from the value at ambient (25°C) to values over the full operating temperature range.

**Offset Error:** Defined as the percentage error (in FSR%) for the ratio between the measured mid-scale output current and the ideal mid-scale output current.

**Output Compliance Range:** Defined as the minimum and maximum allowable voltage at the output of the current-output DAC. Exceeding this limit may result reduced reliability of the device or adversely affecting distortion performance.

**Reference Voltage Drift:** Defined as the maximum change of the reference voltage in ppm per degree Celsius from value at ambient (25°C) to values over the full operating temperature range.

**Spurious Free Dynamic Range (SFDR):** Defined as the difference (in dBc) between the peak amplitude of the output signal and the peak spurious signal.

**Signal to Noise Ratio (SNR):** Defined as the ratio of the RMS value of the fundamental output signal to the RMS sum of all other spectral components below the Nyquist frequency, including noise, but excluding the first six harmonics and dc.

# REGISTER DESCRIPTIONS

## Table 1. Register Map

| Name | Address | Default | (MSB) Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | (LSB) Bit 0 |
|------|---------|---------|-------------|-------|-------|-------|-------|-------|-------|-------------|
| STATUS0 | 0x00 | 0x01 | PLL_lock | unused | unused | device_ID(2:0) | | | version(1:0) | |
| CONFIG1 | 0x01 | 0x0B | insel_mode(1:0) | | unused | synchr_clkin | twos | inv_inclk | interp_value(1:0) | |
| CONFIG2 | 0x02 | 0xE1 | diffclk_ena | clk1_in_ena | clk1c_in_ena | clko_SE_hold | fir4_ena | qmc_offset_ena | qmc_corr_ena | mixer_ena |
| CONFIG3 | 0x03 | 0x00 | diffclk_dly(1:0) | | clko_dly(1:0) | | reserved | | | |
| CONFIG4 | 0x04 | 0x00 | ser_dac_data_ena | output_delay(1:0) | | B_equals_A | A_equals_B | unused | reva | revb |
| CONFIG5 | 0x05 | 0x22 | sif4 | sif_sync_sig | clkdiv_sync_ena | clkdiv_sync_sel | reserved | clkdiv_shift | mixer_gain | unused |
| CONFIG6 | 0x06 | 0x00 | phaseoffset(7:0) | | | | | | | |
| CONFIG7 | 0x07 | 0x00 | phaseoffset(15:8) | | | | | | | |
| CONFIG8 | 0x08 | 0x00 | phaseadd(7:0) | | | | | | | |
| CONFIG9 | 0x09 | 0x00 | phaseadd(15:8) | | | | | | | |
| CONFIG10 | 0x0A | 0x00 | phaseadd(23:16) | | | | | | | |
| CONFIG11 | 0x0B | 0x00 | phaseadd(31:24) | | | | | | | |
| CONFIG12 | 0x0C | 0x00 | qmc_gaina(7:0) | | | | | | | |
| CONFIG13 | 0x0D | 0x00 | qmc_gainb(7:0) | | | | | | | |
| CONFIG14 | 0x0E | 0x00 | qmc_phase(7:0) | | | | | | | |
| CONFIG15 | 0x0F | 0x24 | qmc_phase(9:8) | | qmc_gaina(10:8) | | | qmc_gainb(10:8) | | |
| CONFIG16 | 0x10 | 0x00 | qmc_offseta(7:0) | | | | | | | |
| CONFIG17 | 0x11 | 0x00 | qmc_offsetb(7:0) | | | | | | | |
| CONFIG18 | 0x12 | 0x00 | qmc_offseta(12:8) | | | | | unused | unused | unused |
| CONFIG19 | 0x13 | 0x00 | qmc_offsetb(12:8) | | | | | unused | unused | unused |
| CONFIG20 | 0x14 | 0x00 | ser_dac_data(7:0) | | | | | | | |
| CONFIG21 | 0x15 | 0x00 | ser_dac_data(15:8) | | | | | | | |
| CONFIG22 | 0x16 | 0x15 | nco_sel(1:0) | | nco_reg_sel(1:0) | | qmcorr_reg_sel(1:0) | | qmoffset_reg_sel(1:0) | |
| CONFIG23 | 0x17 | 0x15 | unused | unused | fifo_sel(2:0) | | | aflag_sel | unused | unused |
| CONFIG24 | 0x18 | 0x80 | fifo_sync_strt(3:0) | | | | unused | unused | unused | unused |
| CONFIG25 | 0x19 | 0x00 | unused | unused | unused | unused | unused | unused | unused | unused |
| CONFIG26 | 0x1A | 0x0D | io_1p8_3p3 | unused | sleepb | sleepa | isbiaslpf_a | isbiaslpf_b | PLL_sleep | PLL_ena |
| CONFIG27 | 0x1B | 0xFF | coarse_daca(3:0) | | | | coarse_dacb(3:0) | | | |
| CONFIG28 | 0x1C | 0x00 | reserved | | | | | | | |
| CONFIG29 | 0x1D | 0x00 | PLL_m(4:0) | | | | | PLL_n(2:0) | | |
| CONFIG30 | 0x1E | 0x00 | PLL_LPF_reset | VCO_div2 | PLL_gain(1:0) | | PLL_range(3:0) | | | |

Product Folder Link(s): DAC5688

### Register name: STATUS0 - Address: 0x00, Default 0x01

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PLL_lock | unused | unused | device_ID (2:0) | | | version(1:0) | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

| | | |
|---|---|---|
| PLL_lock | : | Asserted when the internal PLL is locked. (Read Only) |
| device_ID(2:0) | : | Returns '000' for DAC5688. (Read Only) |
| version(1:0) | : | A hardwired register that contains the version of the chip. (Read Only) |

### Register name: CONFIG1 Address: 0x01, Default 0x0B

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| insel_mode (1:0) | | unused | synchr_clkin | twos | inv_inclk | interp_valule(1:0) | |
| 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |

**insel_mode(1:0)** : Controls the expected format of the input data. For the interleaved modes, TXENABLE or the MSB of the port that does not have data can be used to tell the chip which sample is the A sample. For TXENABLE the sample aligned with the rising edge is A. For the MSB, it is presumed that this signal will toggle with A and B. The MSB should be '1' for A and '0' for B. (*** See CONFIG23 ***)

| insel_mode | Function |
|------------|----------|
| 00 | Normal input on A and B. |
| 01 | Interleaved input on A, which is de-interleaved and placed on both A and B data paths. (*** See CONFIG23 ***) |
| 10 | Interleaved input on B, which is de-interleaved and placed on both A and B data paths. (*** See CONFIG23 ***) |
| 11 | Half rate data on A and B inputs. This data is merge together to form a single stream of data on the A data path. |

**synchr_clkin** : This turns on the synchronous mode of the dual-clock in mode. In this mode, the CLK2/C and CLK1/C must be synchronous in phase since the slower clock is used to synchronize dividers in the clock distribution circuit.

**twos** : When set (default), the input data format is expected to be 2's complement. When cleared, the input is expected to be offset-binary.

**inv_inclk** : This allows the input clock, the clock driving the input side of the FIFO to be inverted. This allows easier registering of the data (more setup/hold time) in the single-clock mode of the device

**interp_value(1:0)** : These bits define the interpolation factor:

| interp_value | Interpolation Factor |
|--------------|---------------------|
| 00 | 1X |
| 01 | 2X |
| 10 | 4X |
| 11 | 8X |

## Register name: CONFIG2 Address: 0x02, Default 0xE1

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| diffclk_ena | clk1_in_ena | clk1c_ in_ena | clko_SE_hold | fir4_ ena | qmc_ offset_ena | qmc_ corr_ena | mixer_ena |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

| | | |
|---|---|---|
| **diffclk_ena** | : | When set (default), CLK1 and CLK1C pins are used as a differential clock input. Otherwise, CLK1 pin is used as a single ended input. |
| **clk1_in_ena** | : | When set (default), the CLKO_CLK1 pin is configured as the CLK1 input. If cleared, the pin is configured to output an internally generated CLKO as a clock signal for the input data. |
| **clk1c_in_ena** | : | When set (default), the LOCK_CLK1C pin is configured as the CLK1C input. If cleared, the pin is configured to output the PLL_LOCK status. |
| **clko_SE_hold** | : | When set, the single ended (SE) clock is held to a value of '1' so that the signal doesn't toggle when using the differential clock input. |
| **fir4_ena** | : | When set, the FIR4 Inverse SINC filter is enabled. Otherwise it is bypassed |
| **qmc_offset_ena** | : | When set, the digital Quadrature Modulator Correction (QMC) offset correction circuitry is enabled. |
| **qmc_corr_ena** | : | When set, the QMC phase and gain correction circuitry is enabled. |
| **mixer_ena** | : | When set, the Full Mixer (FMIX) is enabled. Otherwise it is bypassed. |

## Register name: CONFIG3 Address: 0x03, Default 0x00

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| diffclk_dly(1:0) | | clko_dly(1:0) | | Reserved(3:0) | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| **diffclk_dly(1:0)** | : | To allow for a wider range of interfacing, the differential input clock (CLK1/CLK1C) has programmable delay added to its tree. |

| diffclk_dly | Approximate additional delay |
|---|---|
| 00 | 0 |
| 01 | 1.0 ns |
| 10 | 2.0 ns |
| 11 | 3.0 ns |

| | | |
|---|---|---|
| **clko_dly(1:0)** | : | Same as above except these bits effect the single ended or internally generated clock |

## Register name: CONFIG4 Address: 0x04, Default 0x00

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| ser_dac_ data_ena | output_delay(1:0) | | B_equals_A | A_equals_B | unused | reva | revb |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| | | |
|---|---|---|
| **ser_dac_data_ena** | : | Muxes the ser_dac_data(15:0) to both DACs when asserted. |
| **output_delay(1:0)** | : | Delays the output to both DACs from 0 to 3 DAC clock cycles |
| **B_equals_A** | : | When set, the DACA data is driving the DACB output. |
| **A_equals_B** | : | When set, the DACB data is driving the DACA output. |

| Bit 4 B_equals_A | Bit 3 A_equals_B | DACB Output | DACA Output | Description |
|---|---|---|---|---|
| 0 | 0 | B data | A data | Normal Output |
| 0 | 1 | B data | B data | Both DACs driven by B data |
| 1 | 0 | A data | A data | Both DACs driven by A data |
| 1 | 1 | A data | B data | Swapped Output |

| | | |
|---|---|---|
| **reva** | : | Reverse the input bits of the A input port. MSB becomes LSB. |
| **revb** | : | Reverse the input bits of the B input port. MSB becomes LSB |

## Register name: CONFIG5 Address: 0x05, Default 0x22

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| sif4 | sif_ sync_sig | clkdiv_sync_ena | clkdiv_sync_sel | Reserved | clkdiv_shift | mixer_gain | unused |
| 0 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |

| | | |
|---|---|---|
| **sif4** | : | When set, the serial interface (SIF) is a 4 bit interface, otherwise it is a 3 bit interface. |
| **sif_sync_sig** | : | SIF created sync signal. Set to '1' to cause a sync and then clear to '0' to remove it. |
| **clkdiv_sync_ena** | : | Enables syncing of the clock divider using the sync or TXENABLE pins when the bit is asserted. |
| **clkdiv_sync_sel** | : | Selects the input pin to sync the clock dividers. (0 = SYNC, 1 = TXENABLE) |
| **clkdiv_shift** | : | When set, a rising edge on the selected sync (see clkdiv_sync_sel) for the clock dividers will cause a slip in the synchronous counter by 1T and is useful for multi-DAC time alignment. |
| **mixer_gain** | : | When set, adds 6dB to the mixer gain output. |

## Register name: CONFIG6 Address: 0x06, Default 0x00 (Synced)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| | | | phaseoffset(7:0) | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**phaseoffset(7:0)** : See CONFIG7 below.

## Register name: CONFIG7 Address: 0x07, Default 0x00 (Synced)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| | | | phaseoffset(15:8) | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**phaseoffset(15:8)** : This is the phase offset added to the NCO accumulator just before generation of the SIN and COS values. The phase offset is added to the upper 16bits of the NCO accumulator results and these 16 bits are used in the sin/cosine lookup tables.

## Register name: CONFIG8 Address: 0x08, Default 0x00 (Synced)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| | | | phaseadd(7:0) | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**phaseadd(7:0)** : See CONFIG11 below.

## Register name: CONFIG9 Address: 0x09, Default 0x00 (Synced)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| | | | phaseadd(15:8) | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**phaseadd(15:8)** : See CONFIG11 below.

## Register name: CONFIG10 Address: 0x0A, Default 0x00 (Synced)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| | | | phaseadd(23:16) | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**phaseadd(23:16)** : See CONFIG11 below.

### Register name: CONFIG11 Address: 0x0B, Default 0x00 (Synced)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| phaseadd(31:24) | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**phaseadd(31:24)** : The phaseadd(31:24) value is used to determine the frequency of the NCO. The two's complement formatted value can be positive or negative and the LSB is equal to Fs/(2^32).

### Register name: CONFIG12 Address: 0x0C, Default 0x00 (Synced)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| qmc_gaina(7:0) | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**qmc_gaina(7:0)** : Lower 8 bits of the 11-bit Quadrature Modulator Correction (QMC) gain word for DACA. The upper 3 bits are in the CONFIG15 register. The full 11-bit qmc_gaina(10:0) word is formatted as UNSIGNED with a range of 0 to 1.9990 and the default gain is 1.0000. The implied decimal point for the multiplication is between bit 9 and bit 10. Refer to formatting reference below.

| qmc_gaina(10:0) [Binary] | qmc_gaina(10:0) [Decimal] | Format | Gain Value |
|---|---|---|---|
| 00000000000 | 0 | 0 + 0/1024 = | 0.0000000 |
| 00000000001 | 1 | 0 + 1/1024 = | 0.0009766 |
| ….. | ….. | | …. |
| 01111111111 | 1023 | 0 + 1023/1024 = | 0.9990234 |
| 10000000000 | [Default] 1024 | 1 + 0/1024 = | 1.0000000 |
| 10000000001 | 1025 | 1 + 1/1024 = | 1.0009766 |
| ….. | ….. | | …. |
| 11111111111 | 2047 | 1 + 1023/1024 = | 1.9990234 |

### Register name: CONFIG13 Address: 0x0D, Default 0x00 (Synced)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| qmc_gainb(7:0) | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**qmc_gainb(7:0)** : Lower 8 bits of the 11-bit QMC gain word for DACB. The upper 3 bits are in CONFIG15 register. Refer to CONFIG12 above for formatting.

### Register name: CONFIG14 Address: 0x0E, Default 0x00 (Synced)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| qmc_phase(7:0) | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**qmc_phase(7:0)** : Lower 8 bits of the 10-bit Quadrature Modulator Correction (QMC) phase word. The upper 2 bits are in the CONFIG15 register. The full 11-bit **qmc_phase(9:0)** correction word is formatted as two's complement and scaled to occupy a range of −0.125 to 0.12475 and a default phase correction 0.00. To accomplish QMC phase correction, this value is multiplied by the current 'Q' sample, then summed into the 'I' sample. Refer to formatting reference below.

| qmc_phase(9:0) [Binary] | qmc_phase(9:0) [Decimal] | Format | Phase Correction |
|---|---|---|---|
| 10000000000 | −512 | (−1 + 0/512) / 8 = | −0.1250000 |
| 10000000001 | −511 | (−1 + 1/512) / 8 = | −0.1234559 |
| ….. | ….. | | …. |
| 11111111111 | −1 | (−1 + 511/512) / 8 = | −0.0002441 |
| 00000000000 | [Default] 0 | (+0 + 0/512) / 8 = | +0.0000000 |
| 00000000001 | 1 | (+0 + 1/512) / 8 = | +0.0002441 |
| ….. | ….. | | …. |
| 01111111111 | 511 | (+0 + 511/512) / 8 = | +0.1247559 |

### Register name: CONFIG15 Address: 0x0F, Default 0x24 (Synced)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| qmc_phase(9:8) | | qmc_gaina(10:8) | | | qmc_gainb(10:8) | | |
| 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |

**qmc_phase(9:8)** : Upper 2 bits of **qmc_phase** term. Defaults to zero.

**qmc_gaina(10:8)** : Upper 3 bits of **qmc_gaina** term. Defaults to unity gain.

**qmc_gainb(10:8**) : Upper 3 bits of the **qmc_gainb** term. Defaults to unity gain.

### Register name: CONFIG16 Address: 0x10, Default 0x00 (Synced)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| qmc_offseta(7:0) | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**qmc_offseta(7:0)** : Lower 8 bits of the DACA offset correction. The upper 5 bits are in CONFIG18 register. The offset is measured in DAC LSBs.

### Register name: CONFIG17 Address: 0x11, Default 0x00 (Synced)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| qmc_offsetb(7:0) | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**qmc_offsetb(7:0)** : Lower 8 bits of the DACB offset correction. The upper 5 bits are in CONFIG19 register. The offset is measured in DAC LSBs.

### Register name: CONFIG18 Address: 0x12, Default 0x00 (Synced)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| qmc_offseta(12:8) | | | | | unused | unused | unused |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**qmc_offseta(12:8)**   :   Upper 5 bits of the DACA offset correction.

### Register name: CONFIG19 Address: 0x13, Default 0x00 (Synced)

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| qmc_offsetb(12:8) | | | | | unused | unused | unused |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**qmc_offsetb(12:8)**   :   Upper 5 bits of the DACB offset correction.

### Register name: CONFIG20 Address: 0x14, Default 0x00

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ser_dac_data(7:0) | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**ser_dac_data(7:0)**          :   Lower 8 bits of the serial interface controlled DAC value. This data is routed to both DACs when enabled via **ser_dac_data_ena** in CONFIG4. Value is expected in 2s complement format.

### Register name: CONFIG21 Address: 0x15, Default 0x00

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ser_dac_data(15:8) | | | | | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**ser_dac_data(15:8)**          :   Upper 8 bits of the serial interface controlled DAC value. This data is routed to both DACs when enabled via **ser_dac_data_ena** in CONFIG4. Value is expected in 2's complement format.

### Register name: CONFIG22 Address: 0x16, Default 0x15

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| nco_sel(1:0) | | nco_reg_sel(1:0) | | qmcorr_reg_sel(1:0) | | qmoffset_reg_sel(1:0) | |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |

**nco_sel(1:0)**                    :   Selects the signal to use as the sync for the NCO accumulator.
**nco_reg_sel(1:0)**            :   Selects the signal to use as the sync for loading the NCO registers.
**qmcorr_reg_sel(1:0)**      :   Selects the signal to use as the sync for loading the QM correction registers.
**qmoffsest_reg_sel(1:0)**   :   Selects the signal to use as the sync for loading the QM offset correction registers.

| *_sel (1:0) | Sync selected |
|-------------|---------------|
| 00 | TXENABLE from FIFO output |
| 01 | SYNC from FIFO output |
| 10 | sync_SIF_sig (via CONFIG5) |
| 11 | Always zero |

Product Folder Link(s): DAC5688

### Register name: CONFIG23 Address: 0x17, Default 0x15

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| unused | unused | fifo_sel(2:0) | | | aflag_ sel | unused | unused |
| 0 | 0 | 0 | 1 | 0 | 1 | 0 | 1 |

**fifo_sel(2:0)** : Selects the sync source for the FIFO from the table below. For the case where the sync is dependent on the first transition of the input data MSB: Once the transition occurs, the only way to get another sync it to reset the device or to program **fifo_sel** to another value

| fifo_sel (2:0) | Sync selected |
|---|---|
| 000 | TXENABLE from pin |
| 001 | SYNC from pin |
| 010 | sync_SIF_sig (via CONFIG5) |
| 011 | Always zero |
| 100 | 1st transition on DA MSB |
| 101 | 1st transition on DB MSB |
| 110 | Always zero |
| 111 | Always one |

**aflag_sel** : When set, the MSB of the input opposite of incoming data is used to determine the A sample. When cleared, rising edge of TXENABLE is used. Refer to Figure 37.

### Register name: CONFIG24 Address: 0x18, Default 0x80

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| fifo_sync_strt(3:0) | | | | Unused | Unused | Unused | Unused |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**fifo_sync_strt(3:0)** : When the sync to the FIFO occurs, this is the value loaded into the FIFO output position counter. With this value the initial difference between input and output pointers can be controlled. This may be helpful in syncing multiple chips or controlling the delay through the device.

### Register name: CONFIG25 Address: 0x19, Default 0x00

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| Unused | Unused | Unused | Unused | Unused | Unused | Unused | Unused |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

### Register name: CONFIG26 Address: 0x1A, Default 0x0D

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| io_1p8_3p3 | Unused | sleepb | sleepa | isbiaslpfb_a | isbiaslpf_b | PLL_ sleep | PLL_ena |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 |

**io_1p8_3p3** : Used to program the digital input voltage threshold levels. '0'=3.3V tolerate pads and '1'=1.8V tolerate pads. Applies to following digital pins: CLKO_CLK1, LOCK_CLK1C, DA[15:0], DB[15:0], SYNC, RESETB, SCLK, SDENB, SDIO (input only) and TXENABLE.

**sleepb** : When set, DACB is put into sleep mode. Putting the DAC into single DAC mode does not automatically assert this signal, so for minimum power in single DAC mode, also program this register bit.

**sleepa** : When set, DACA is put into sleep mode. Note: If DACA channel is in sleep mode (**sleepa** = '1') the DACB channel is also forced in to sleep mode.

**isbiaslpfb_a** : Turns on the low pass filter for the current source bias in the DACA when cleared. The low pass filter will set a corner at ~472kHz when low and ~95 kHz when high.

**isbiaslpfb_b** : Turns on the low pass filter for the current source bias in the DACB when cleared. The low pass filter will set a corner at ~472kHz when low and ~95 kHz when high.

**PLL_sleep** : When set, the PLL is put into sleep mode. Bypassing the PLL does not automatically but it into sleep mode.

**PLL_ena** : When set, the PLL is on and its output clock is being used as the DAC clock.

Product Folder Link(s): DAC5688

## Register name: CONFIG27 Address: 0x1B, Default 0xFF

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| coarse_daca(3:0) | | | | coarse_dacb(3:0) | | | |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

**coarse_daca(3:0)**   :   Scales the output current is 16 equal steps.

$$\frac{V_{EXTIO}}{Rbias} \times (DACA\_gain + 1)$$

**coarse_dacb(3:0)**   :   Same as above except for DACB.

## Register name: CONFIG28 Address: 0x1C, Default 0x00

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

## Register name: CONFIG29 Address: 0x1D, Default 0x00

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PLL_m(4:0) | | | | | PLL_n(2:0) | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**PLL_m**   :   M portion of the M/N divider of the PLL thermometer encoded:

| PLL_m(4:0) | M value |
|------------|---------|
| 00000 | 1 |
| 00001 | 2 |
| 00011 | 4 |
| 00111 | 8 |
| 01111 | 16 |
| 11111 | 32 |
| All other values | Invalid |

**PLL_n**   :   N portion of the M/N divider of the PLL thermometer encoded. If supplying a high rate CLK2/C frequency, the PLL_n value should be used to divide down the input CLK2/C to maintain a maximum PFD operating of 160 MHz.

| PLL_n(2:0) | n value |
|------------|---------|
| 000 | 1 |
| 001 | 2 |
| 011 | 4 |
| 111 | 8 |
| All other values | Invalid |

**PLL Function:**

$$f_{vco} = \left[\frac{(M)}{(N)}\right] \times f_{ref}$$

where $f_{ref}$ is the frequency of the external DAC clock input on the CLK2/C pins

## Register name: CONFIG30 Address: 0x1E, Default 0x00

| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|
| PLL_LPF_ reset | VCO_div2 | PLL_gain(1:0) | | PLL_range(3:0) | | | |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

**PLL_LPF_reset** : When set, can be used to hold the PLL loop filter at 0 volts.

**VCO_div2** : When set, the PLL CLOCK output is 1/2 the PLL VCO frequency. Used to run the VCO at 2X the desired clock frequency to reduce phase noise for lower DAC clock rates.

**PLL_gain(1:0)** : Used to adjust the PLL's Voltage Controlled Oscillator (VCO) gain, $K_{VCO}$. Refer to the Electrical Characteristics table. By increasing the **PLL_gain**, the VCO can cover a broader range of frequencies; however, the higher gain also increases the phase noise of the PLL. In general, lower **PLL_gain** settings result in lower phase noise. The $K_{VCO}$ of the VCO can also affect the PLL stability and is used to determine the loop filter components. See section on determining the PLL filter components for more detail.

**PLL_range(3:0)** : Used to adjust the bias current of the VCO. By increasing the bias current, the oscillator can reach higher frequencies. Refer to the Electrical Characteristics table.
'0000' – minimum bias current and lowest VCO frequency range
'1111' – maximum bias current and highest VCO frequency range

Product Folder Link(s): *DAC5688*

# DETAILED DESCRIPTION

## EXAMPLE SYSTEM DIAGRAM
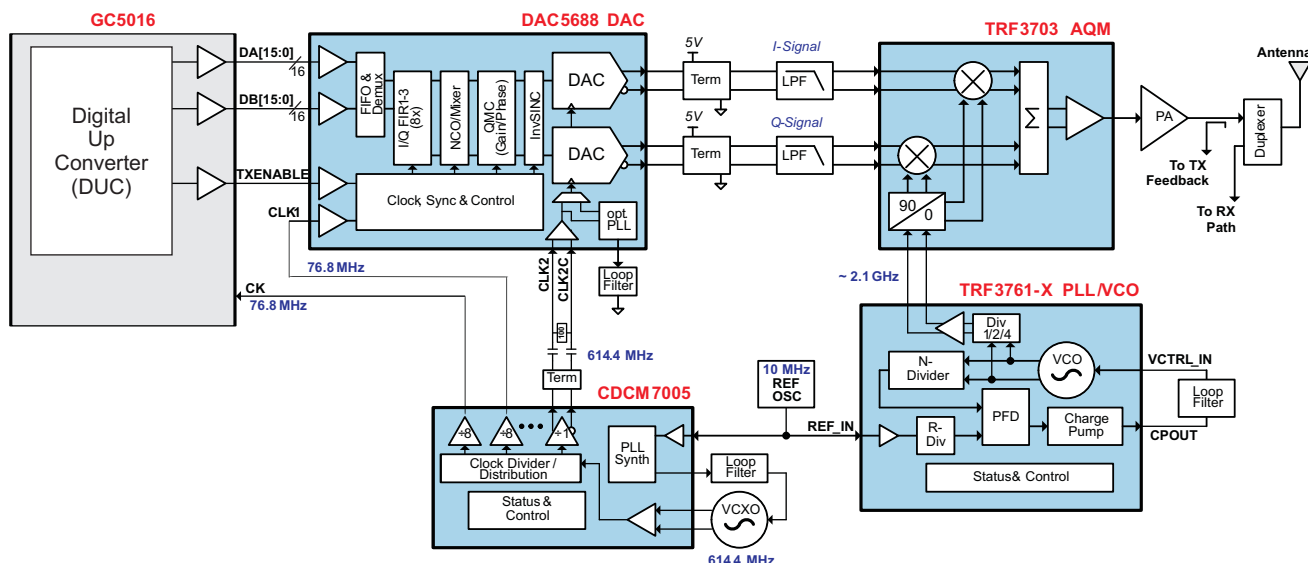


**Figure 19.  Example System Diagram: Direct Conversion with 8x interpolation**

## SERIAL INTERFACE

The serial port of the DAC5688 is a flexible serial interface which communicates with industry standard microprocessors and microcontrollers. The interface provides read/write access to all registers used to define the operating modes of DAC5688. It is compatible with most synchronous transfer formats and can be configured as a 3 or 4 pin interface by **SIF4** in register **CONFIG5**. In both configurations, **SCLK** is the serial interface input clock and **SDENB** is serial interface enable. For 3 pin configuration, **SDIO** is a bidirectional pin for both data in and data out. For 4 pin configuration, **SDIO** is data in only and **SDO** is data out only. Data is input into the device with the rising edge of **SCLK**. Data is output from the device on the falling edge of **SCLK**.

Each read/write operation is framed by signal **SDENB** (Serial Data Enable Bar) asserted low for 2 to 5 bytes, depending on the data length to be transferred (1–4 bytes). The first frame byte is the instruction cycle which identifies the following data transfer cycle as read or write, how many bytes to transfer, and what address to transfer the data. Table 2 indicates the function of each bit in the instruction cycle and is followed by a detailed description of each bit. Frame bytes 2 to 5 comprise the data transfer cycle.

**Table 2. Instruction Byte of the Serial Interface**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Description | R/W | N1 | N0 | A4 | A3 | A2 | A1 | A0 |

| | |
|---|---|
| **R/W** | Identifies the following data transfer cycle as a read or write operation. A high indicates a read operation from DAC5688 and a low indicates a write operation to DAC5688. |
| **[N1 : N0]** | Identifies the number of data bytes to be transferred per Table 3. Data is transferred MSB first. |

**Table 3. Number of Transferred Bytes Within One Communication Frame**

| N1 | N0 | Description |
|---|---|---|
| 0 | 0 | Transfer 1 Byte |
| 0 | 1 | Transfer 2 Bytes |
| 1 | 0 | Transfer 3 Bytes |
| 1 | 1 | Transfer 4 Bytes |

| | |
|---|---|
| **[A4 : A0]** | Identifies the address of the register to be accessed during the read or write operation. For multi-byte transfers, this address is the starting address. Note that the address is written to the DAC5688 MSB first and counts down for each byte |

Figure 20 shows the serial interface timing diagram for a DAC5688 write operation. **SCLK** is the serial interface clock input to DAC5688. Serial data enable **SDENB** is an active low input to DAC5688. **SDIO** is serial data in. Input data to DAC5688 is clocked on the rising edges of **SCLK**.
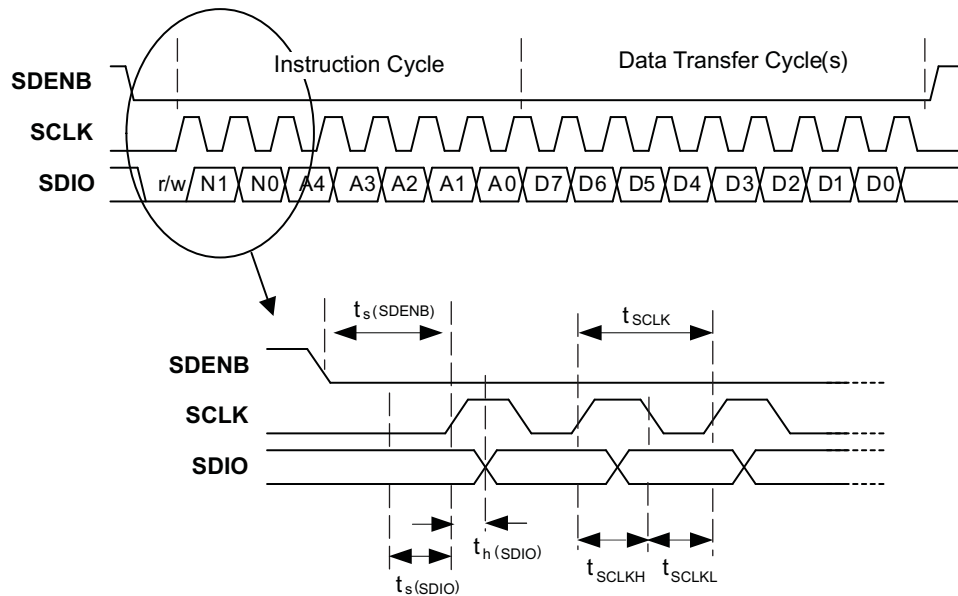


**Figure 20.  Serial Interface Write Timing Diagram**

Figure 21 shows the serial interface timing diagram for a DAC5688 read operation. **SCLK** is the serial interface clock input to DAC5688. Serial data enable **SDENB** is an active low input to DAC5688. **SDIO** is serial data in during the instruction cycle. In 3 pin configuration, **SDIO** is data out from DAC5688 during the data transfer cycle(s), while SDO is in a high-impedance state. In 4 pin configuration, **SDO** is data out from DAC5688 during the data transfer cycle(s). The **SDIO/SDO** data is output on the falling edge of **SCLK**. At the end of the data transfer, SDO will output low on the final falling edge of SCLK until the rising edge of SDENB when it will 3-state.

Product Folder Link(s): *DAC5688*
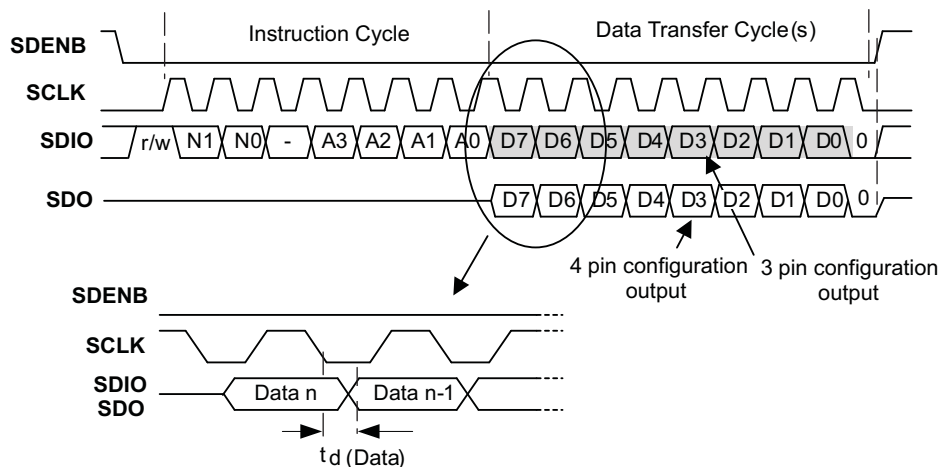
**Figure 21. Serial Interface Read Timing Diagram**

## FIR FILTERS

Figure 22 shows the magnitude spectrum response for FIR1, a 67-tap interpolating half-band filter. The transition band is from 0.4 to 0.6 × $f_{IN}$ (the input data rate for the FIR filter) with <0.002-dB of pass-band ripple and > 80-dB stop-band attenuation. Figure 23 shows the transition band region from 0.37 to 0.47 × fIN. Up to 0.458 × $f_{IN}$ there is less than 0.5 dB of attenuation.

Figure 24 shows the magnitude spectrum response for the 19-tap FIR2 filter. The transition band is from 0.25 to 0.75 × $f_{IN}$ (the input data rate for the FIR filter). For 4x interpolation modes, the composite filter response is shown in Figure 25.

Figure 26 shows the magnitude spectrum response for the 11-tap FIR3 filter. For 8x interpolation modes, the composite filter response is shown in Figure 27.

The DAC5688 also has a 9-tap non-interpolating inverse sinc filter (FIR4) running at the DAC update rate ($f_{DAC}$) that can be used to flatten the frequency response of the sample and hold output. The DAC sample and hold output set the output current and holds it constant for one DAC clock cycle until the next sample, resulting in the well known sin(x)/x or sinc(x) frequency response shown in Figure 28 (red dash-dotted line). The inverse sinc filter response (Figure 28, blue dashed line) has the opposite frequency response between 0 to 0.4 × $f_{DAC}$, resulting in the combined response (Figure 28, green solid line). Between 0 to 0.4 × $f_{DAC}$, the inverse sinc filter compensates the sample and hold rolloff with less than 0.03-dB error.

The inverse sinc filter has a gain > 1 at all frequencies. Therefore, the signal input to FIR4 must be reduced from full scale to prevent saturation in the filter. The amount of backoff required depends on the signal frequency, and is set such that at the signal frequencies the combination of the input signal and filter response is less than 1 (0 dB). For example, if the signal input to FIR4 is at 0.25 × $f_{DAC}$, the response of FIR4 is 0.9 dB, and the signal must be backed off from full scale by 0.9 dB. The gain function in the QMC block can be used to set reduce amplitude of the input signal. The advantage of FIR4 having a positive gain at all frequencies is that the user is then able to optimized backoff of the signal based on the signal frequency.

The filter taps for all digital filters are listed in Table 4. Note that the loss of signal amplitude may result in lower SNR due to decrease in signal amplitude.
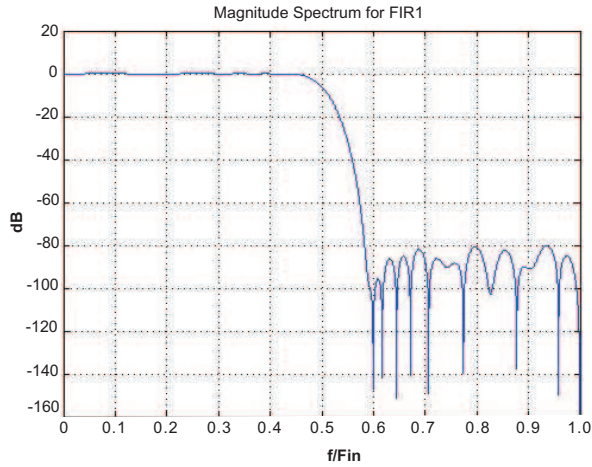
**Figure 22. Magnitude Spectrum for FIR1**
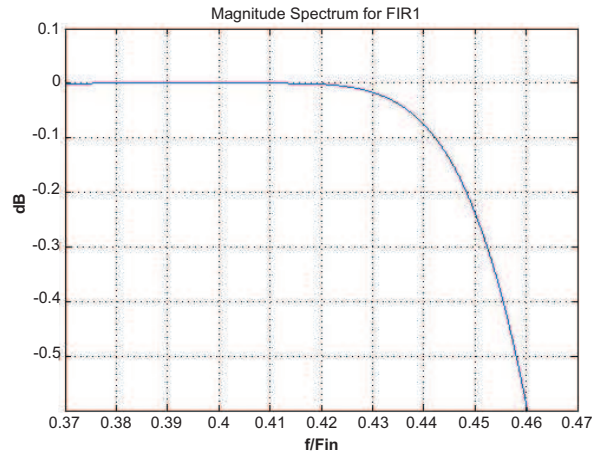


**Figure 23. FIR1 Transition Band**
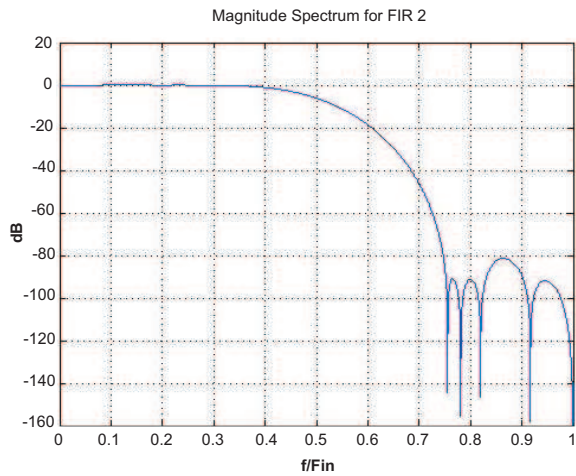


**Figure 24. Magnitude Spectrum for FIR2**
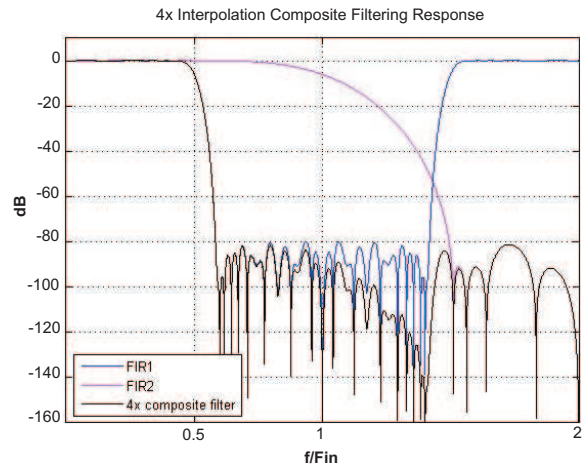


**Figure 25. 4x Interpolation Composite Response**

Product Folder Link(s): *DAC5688*
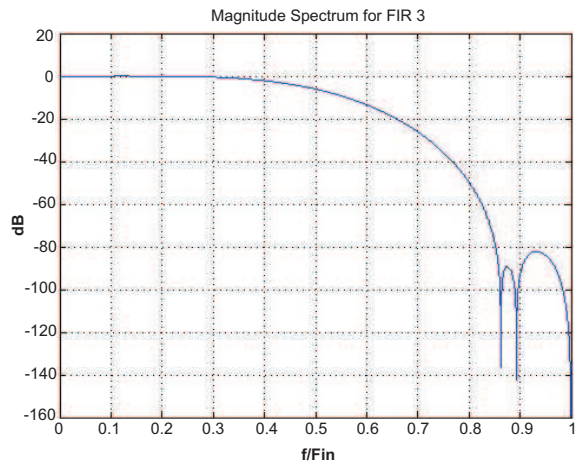
**Figure 26. Magnitude Spectrum for FIR3**
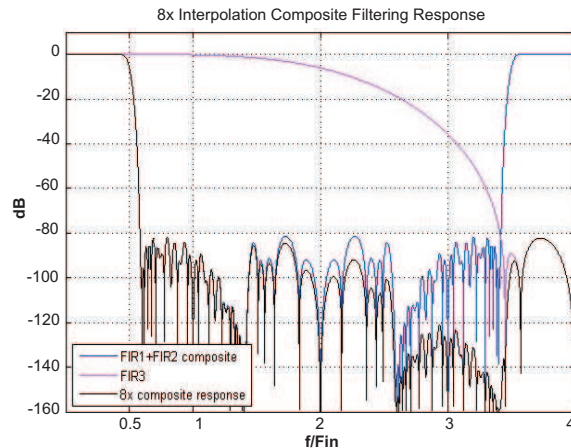


**Figure 27. 8x Interpolation Composite Response**
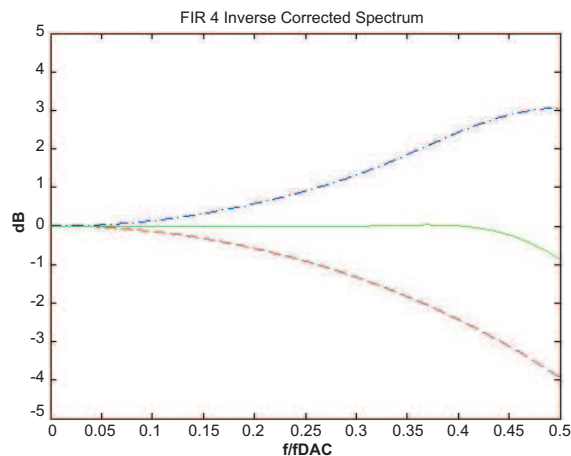


**Figure 28. Magnitude Spectrum for FIR4**

Product Folder Link(s): DAC5688

**Table 4. FIR Filter Coefficients**

| 2X Interpolating Half-band Filters | | | | | | Non-Interpolating Inverse-SINC Filter | |
|---|---|---|---|---|---|---|---|
| FIR1 | | FIR2 | | FIR3 | | FIR4 | |
| 67 Taps | | 19 Taps | | 11 Taps | | 9 Taps | |
| 2 | 2 | 9 | 9 | 31 | 31 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | -4 | −4 |
| −5 | −5 | −58 | −58 | −219 | −219 | 13 | 13 |
| 0 | 0 | 0 | 0 | 0 | 0 | −50 | −50 |
| 11 | 11 | 214 | 214 | 1212 | 1212 | **592**[1] | |
| 0 | 0 | 0 | 0 | **2048**[1] | | | |
| −21 | −21 | −638 | −638 | | | | |
| 0 | 0 | 0 | 0 | | | | |
| 37 | 37 | 2521 | 2521 | | | | |
| 0 | 0 | **4096** [1] | | | | | |
| −61 | −61 | | | | | | |
| 0 | 0 | | | | | | |
| 97 | 97 | | | | | | |
| 0 | 0 | | | | | | |
| −148 | −148 | | | | | | |
| 0 | 0 | | | | | | |
| 218 | 218 | | | | | | |
| 0 | 0 | | | | | | |
| −314 | −314 | | | | | | |
| 0 | 0 | | | | | | |
| 444 | 444 | | | | | | |
| 0 | 0 | | | | | | |
| −624 | −624 | | | | | | |
| 0 | 0 | | | | | | |
| 877 | 877 | | | | | | |
| 0 | 0 | | | | | | |
| −1260 | −1260 | | | | | | |
| 0 | 0 | | | | | | |
| 1916 | 1916 | | | | | | |
| 0 | 0 | | | | | | |
| −3372 | −3372 | | | | | | |
| 0 | 0 | | | | | | |
| 10395 | 10395 | | | | | | |
| **16384** [1] | | | | | | | |

(1)   Center Taps are highlighted in **BOLD.**

Product Folder Link(s): *DAC5688*

## Full Complex Mixer (FMIX)

The full complex Mixer (FMIX) block uses a Numerically Controlled Oscillator (NCO) with a 32-bit frequency register **phaseadd(31:0)** and a 16-bit phase register **phaseoffset(15:0)** to provide sin and cos for mixing. The NCO tuning frequency is programmed in CONFIG8 through CONFIG11 registers. Phase offset is programmed in CONFIG6 and CONFIG7 registers. A block-diagram of the NCO is shown below in Figure 29.
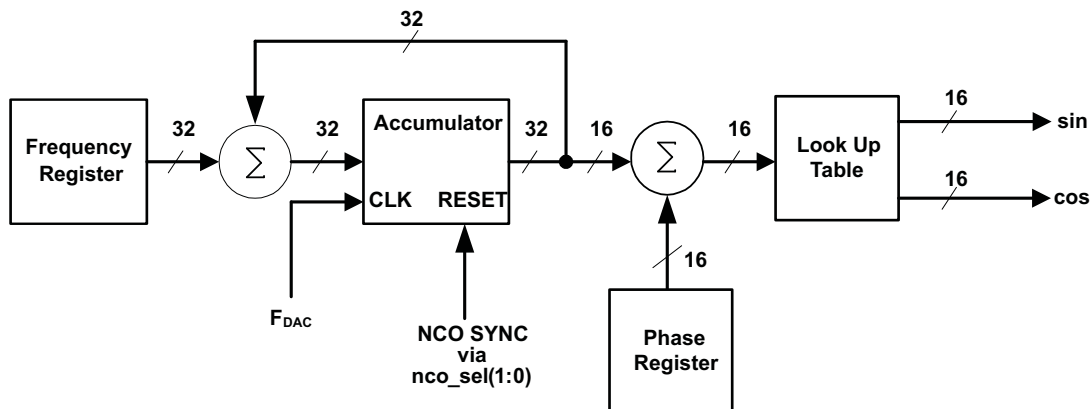


**Figure 29. Block-Diagram of the NCO**

Synchronization of the NCO occurs by resetting the NCO accumulator to zero. The synchronization source is selected by CONFIG22 **nco_sel(1:0)**. Frequency word $f_{ref}$ in the phaseadd register is added to the accumulator every clock cycle, $f_{DAC}$. The output frequency of the NCO is

$$f_{NCO} = \frac{f_{ref} \times f_{NCO\_CLK}}{2^{32}} \tag{1}$$

Treating channels A and B as a complex vector I + I×Q where I(t) = A(t) and Q(t) = B(t), the output of FMIX $I_{OUT}(t)$ and $Q_{OUT}(t)$ is

$$I_{OUT}(t) = \left(I_{IN}(t)\cos\left(2\pi f_{NCO}t + \delta\right) - Q_{IN}(t)\sin\left(2\pi f_{NCO}t + \delta\right)\right) \times 2^{(mixer\_gain - 1)} \tag{2}$$

$$Q_{OUT}(t) = \left(I_{IN}(t)\sin\left(2\pi f_{NCO}t + \delta\right) + Q_{IN}(t)\cos\left(2\pi f_{NCO}t + \delta\right)\right) \times 2^{(mixer\_gain - 1)} \tag{3}$$

Where t is the time since the last resetting of the NCO accumulator, $\delta$ is the phase offset value and **mixer_gain** is either 0 or 1. $\delta$ is given by:

$$\delta = 2\pi \times phase(15:0)/2^{16} \tag{4}$$

The maximum output amplitude of FMIX occurs if $I_{IN}(t)$ and $Q_{IN}(t)$ are simultaneously full scale amplitude and the sine and cosine arguments $2\pi f_{NCO}t + \delta$ (2N-1)×$\pi$/4 (N = 1, 2, ...).

With CONFIG5 **mixer_gain** = 0, the gain through FMIX is sqrt(2)/2 or –3 dB. This loss in signal power is in most cases undesirable, and it is recommended that the gain function of the QMC block be used to increase the signal by 3 dB to compensate. With **mixer_gain** = 1, the gain through FMIX is sqrt(2) or + 3 dB, which can cause clipping of the signal if $I_{IN}(t)$ and $Q_{IN}(t)$ are simultaneously near full scale amplitude and should therefore be used with caution.

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## Quadrature Modulator Correction (QMC)

The Quadrature Modulator Correction (QMC) block provides a means for adjusting the gain and phase of the complex signal. At a quadrature modulator output, gain and phase imbalances result in an undesired sideband signal.

The block diagram for the QMC is shown in Figure 30. The QMC block contains 3 programmable parameters: **qmc_gaina**(10:0), **qmc_gainb**(10:0) and **qmc_phase**(9:0).

Registers **qmc_gaina**(10:0) and **qmc_gainb**(10:0) control the I and Q path gains and are 11 bit values with a range of 0 to approximately 2. This value is used to scale the signal range. Register qmc_phase(9:0) controls the phase imbalance between I and Q and is a 10-bit value that ranges from –1/8 to approximately +1/8. This value is multiplied by each Q sample then summed into the I sample path. This operation is a simplified approximation of a true phase rotation and covers the range from –7.5 to +7.5 degrees in 1024 steps.
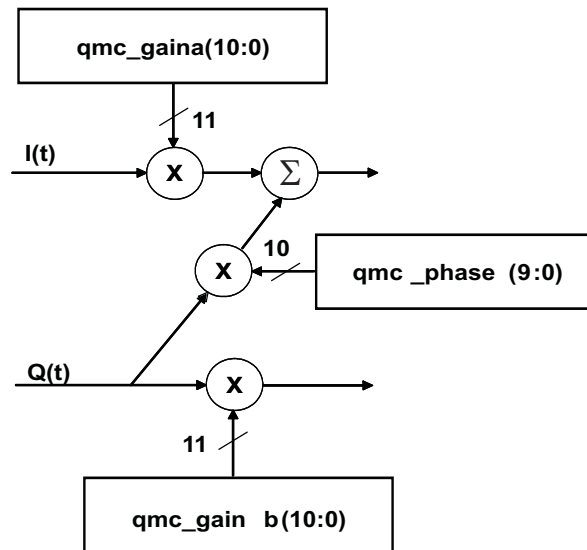


**Figure 30. QMC Block Diagram**

## DAC Offset Control

The **qmc_offseta**(12:0) and **qmc_offsetb**(12:0) values can be used to independently adjust the I and Q path DC offsets. Both offset values are in represented in 2s-complement format with a range from –4096 to 4095.

The offset value adds a digital offset to the digital data before digital-to-analog conversion. Since the offset is added directly to the data it may be necessary to back off the signal to prevent saturation. Both data and offset values are LSB aligned.
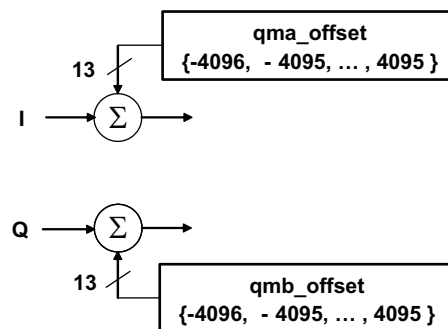


**Figure 31. DAC Offset Block**

Product Folder Link(s): *DAC5688*

## CLOCK MODES

The DAC5688 supports several different clocking modes for generating the internal clocks for the logic and DAC. The clocking modes are selected by programming the register bits below and summarized in Table 5.

| Register | Control Bits |
|---|---|
| CONFIG1 | **synchr_clkin** |
| CONFIG2 | **clk1_in_ena, clk1c_in_ena, diffclk_ena** |
| CONFIG26 | **PLL_ena** |

### Table 5. Summary of Clock Modes and Options

| Clocking Mode | Option | CLKO_CLK1 I/O | Programming Bits | | | | |
|---|---|---|---|---|---|---|---|
| | | | synchr_clkin | clk1_in_en | clk1c_in_ena | diffclk_ena | PLL_ena |
| Dual Synchronous Clock Mode | Diff. CLK1 | Input | 1 | 1 | 1 | 1 | 0 |
| | S/E CLK1 | Input | 1 | 1 | X | 0 | 0 |
| Dual Clock Mode | Diff. CLK1 | Input | 0 | 1 | 1 | 1 | 0 |
| | S/E CLK1 | Input | 0 | 1 | X | 0 | 0 |
| External Clock Mode | CLKO | Output | 0 | 0 | X | 0 | 0 |
| PLL Clock Mode | Diff. CLK1 | Input | 0 | 1 | 1 | 1 | 1 |
| | S/E CLK1 | Input | 0 | 1 | X | 0 | 1 |
| | CLKO | Output | 0 | 0 | X | 0 | 1 |

## DUAL SYNCHRONOUS CLOCK MODE

In DUAL SYNCHRONOUS CLOCK MODE, the user provides the CLK2/C clock signal at the DAC sample rate and also provides a divided down CLK1 at the input data rate. The CLK1 signal can be differential or single-ended. Refer to Figure 16 for the timing diagram. In this mode the relationship between CLK2 and CLK1 ($t_{\_align}$) is critical and used as a synchronizing mechanism for the internal logic. This facilitates multi-DAC synchronization by using dual external clock inputs CLK1 and CLK2 while FIFO data is always written and read from location zero. It is highly recommended that a clock synchronizer device such as the CDCM7005 provide both CLK2/C and CLK1/C inputs. Although CLK1 could be single-ended it is recommended to use a differential clock to ensure proper skews between the two clock inputs.

## DUAL CLOCK MODE

In DUAL CLOCK MODE, the user provides the CLK2/C clock signal at the DAC sample rate and also provides a divided down CLK1 at the input data rate. The CLK1 signal can be differential or single-ended. Refer to Figure 32 for the timing diagram. Unlike the DUAL SYNCHRONOUS CLOCK MODE, the $t_{\_align}$ parameter is not critical because these clocks are not used as a synchronizing mechanism for the internal logic and the FIFO is used as an elastic buffer for the data. Synchronizing in this mode is provided by separate control inputs.
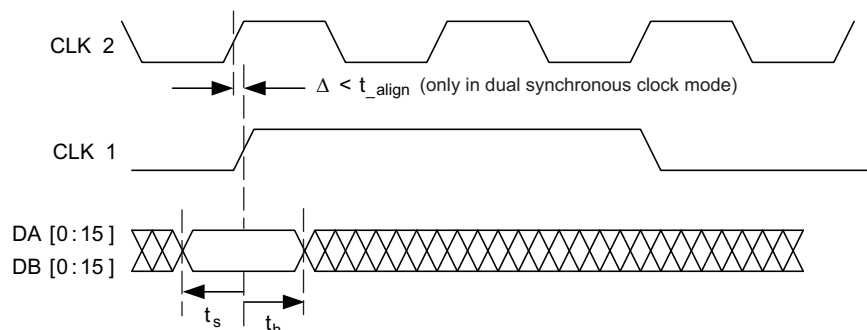


**Figure 32.  DUAL (SYNCHRONOUS) CLOCK MODE Timing Diagram**

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## EXTERNAL CLOCK MODE

In EXTERNAL CLOCK MODE, the user provides a clock signal at the DAC output sample rate through CLK2/C. The CLKO_CLK1 pin is configured as an output in this mode and will toggle at a required frequency for the configured interpolation rate and data mode. The CLKO_CLK1 clock can be used to drive the input data source (such as digital upconverter) that sends the data to the DAC. Note that the CKO_CLK1 delay relative to the input CLK2 rising edge ($t_{d(CLKO)}$ in Figure 33) will increase with increasing loads.
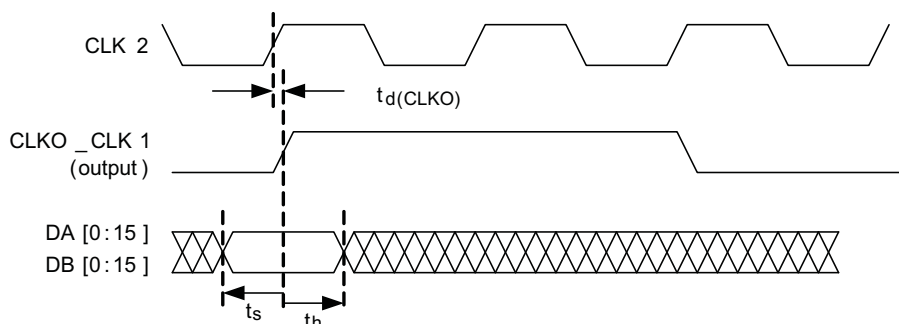


**Figure 33. EXTERNAL CLOCK MODE Timing Diagram**

## PLL CLOCK MODE

In PLL CLOCK MODE, the user provides an external reference clock to the CLK2/C input pins. Refer to Figure 34. An internal clock multiplying PLL uses the lower-rate reference clock to generate a high-rate clock for the DAC. This function is very useful when a high-rate clock is not already available at the system level; however, the internal VCO phase noise in PLL Clock Mode may degrade the quality of the DAC output signal when compared to an external low jitter clock source.
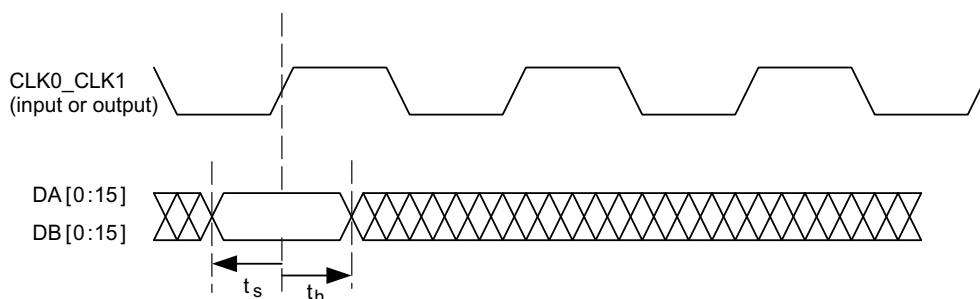


**Figure 34. PLL CLOCK MODE Timing Diagram**

The internal PLL has a type four phase-frequency detector (PFD) comparing the CLK2/C reference clock with a feedback clock to drive a charge pump controlling the VCO operating voltage and maintaining synchronization between the two clocks. An external low-pass filter is required to control the loop response of the PLL. See the *Low-Pass Filter* section for the filter setting calculations. This is the only mode where the LPF filter applies.

The input reference clock N-Divider is selected by CONFIG29 **PLL_n(2:0)** for values of ÷1, ÷2, ÷4 or ÷8. The VCO feedback clock M-Divider is selected by CONFIG29 **PLL_m(4:0)** for values of ÷1, ÷2, ÷4, ÷8, ÷16 or ÷32. The combination of M-Divider and N-Divider form the clock multiplying ratio of M/N. If the reference clock frequency is greater than 160MHz, use a N-Divider of ÷2, ÷4 or ÷8 to avoid exceeding the maximum PFD operating frequency.

For DAC sample rates less than the maximum VCO operating frequency of 910/2 or **455** MHz. The phase noise of PLL may improved by using the output divider via CONFIG30 **VCO_div2**. If not using the PLL, clear CONFIG26 **PLL_ena** and set CONFIG26 **PLL_sleep** to reduce power consumption. In some cases, it may be useful to reset the VCO control voltage by toggling CONFIG30 **PLL_LPF_reset**.
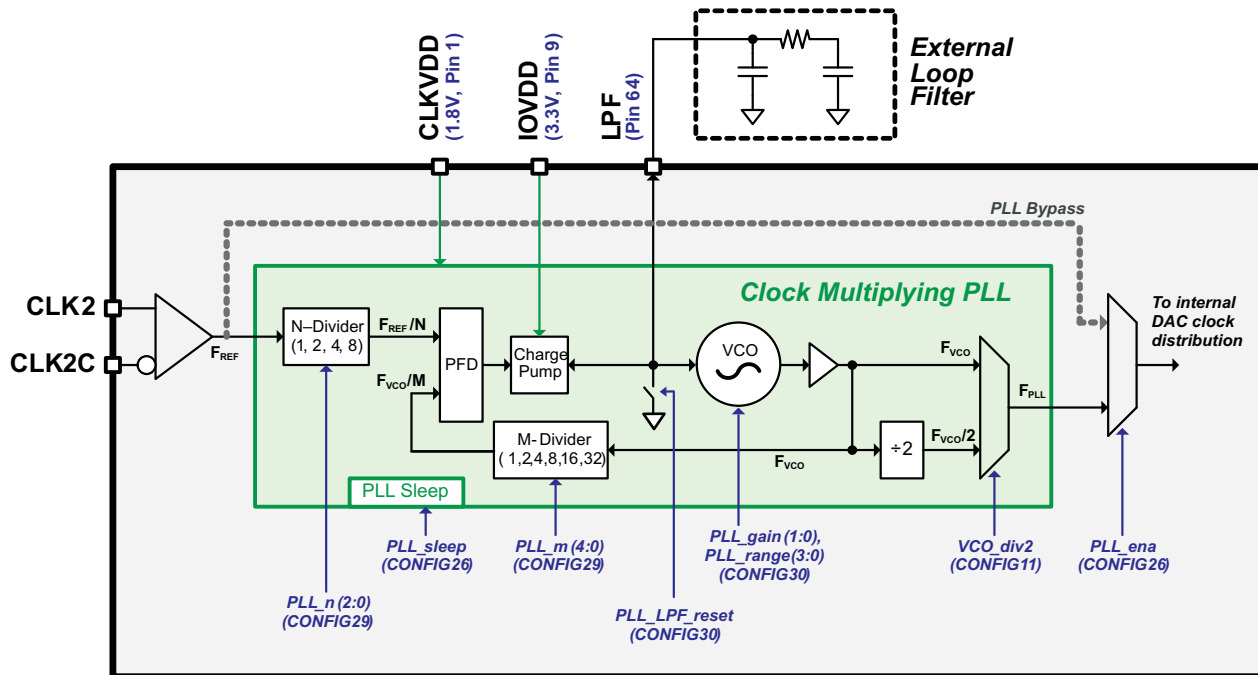
**Figure 35. Functional Block Diagram for PLL**

## DATA BUS MODES

The DAC5688 supports three DATA BUS MODES:

1. DUAL BUS MODE
2. INTERLEAVED BUS MODE
3. HALF RATE BUS MODE

## DUAL BUS MODE

In DUAL BUS MODE, the user inputs data on both DA[15:0] and DB[15:0] ports. This mode is selected by setting CONFIG1 **insel_mode(1:0)** = '00'. Refer to Figure 36.
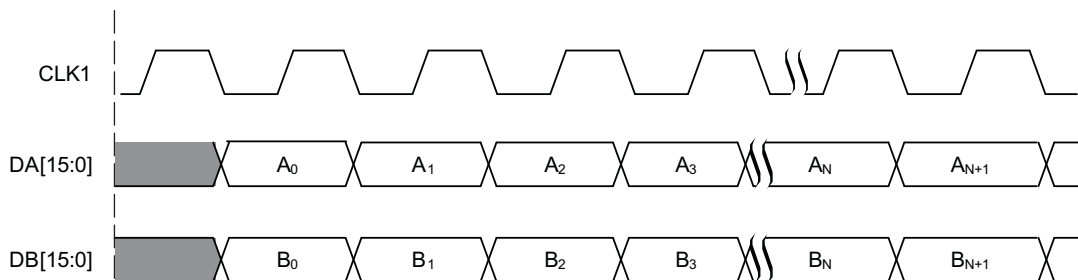


**Figure 36. DUAL BUS MODE (Dual Clock Mode)**

## INTERLEAVED BUS MODE

In INTERLEAVED BUS MODE, the user inputs dual-channel data as an interleaved single data stream to either DA[15:] or DB[15:0] ports. The DAC5688 de-interleaves the input data stream and routes to both A and B data paths. For input data on DA[15:0], set CONFIG1 **insel_mode[15:0]** = '01'. For input data on DB[15:0], set CONFIG1 **insel_mode[15:0]** = '10'. In this bus mode, a separate input flag is required to distinguish an A sample from a B sample in the interleaved data stream. This flag can either be the single event rising edge of TXENABLE or the continuous toggling MSB of the port inactive data port. For the TXENABLE flag option, set the CONFIG23 **aflag_sel** bit and the A sample will be expected to be aligned with the rising edge of TXENABLE. For the toggling MSB option, clear the CONFIG23 **aflag_**sel bit and the A sample will be expected for each '1' of the MSB with the B sample is flagged for each '0' of the MSB. Refer to Figure 37.
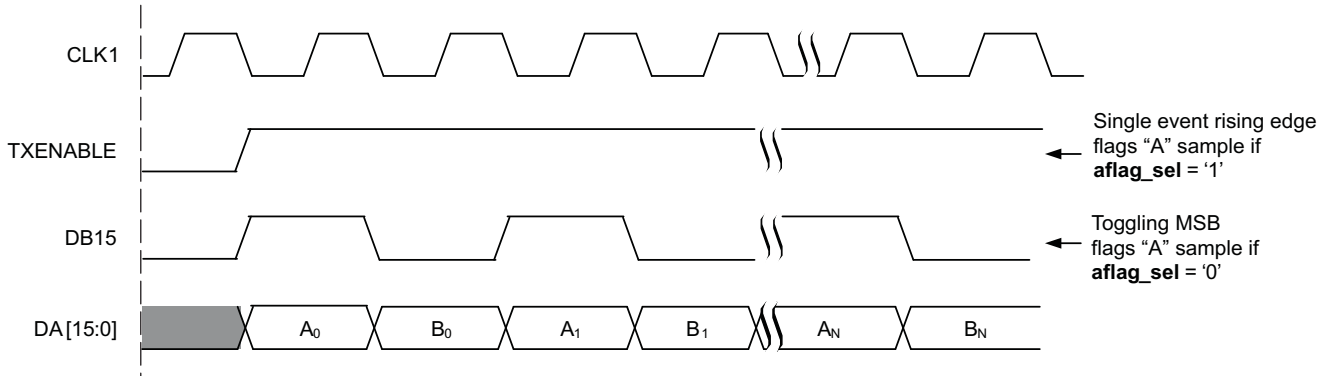


**Figure 37. INTERLEAVED BUS MODE on DA[15:0] port (Dual Clock Mode)**

## HALF RATE BUS MODE

In HALF RATE BUS MODE, the user inputs data on both DA[15:0] and DB[15:0] ports at half rate and input logic merges both data streams into one DAC channel (A). This mode is selected by setting CONFIG1 **insel_mode[15:0]** = '11'. Refer to Figure 38.
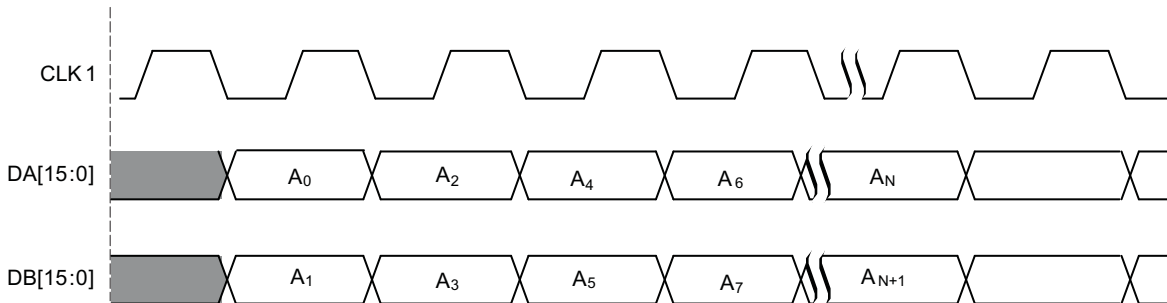


**Figure 38. HALF RATE BUS MODE (Dual Clock Mode)**

Product Folder Link(s): *DAC5688*

## CLK2 and CLK2C Inputs

Figure 39 shows an equivalent circuit for the DAC input clock (CLK2/C).
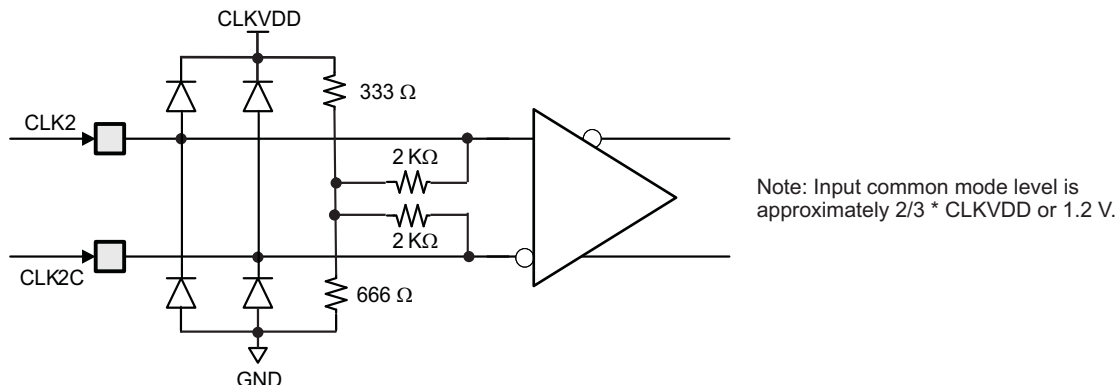


**Figure 39.  CLK2/C Equivalent Input Circuit**

Figure 40 shows the preferred configuration for driving the CLK2/CLK2C input clock with a differential ECL/PECL source.
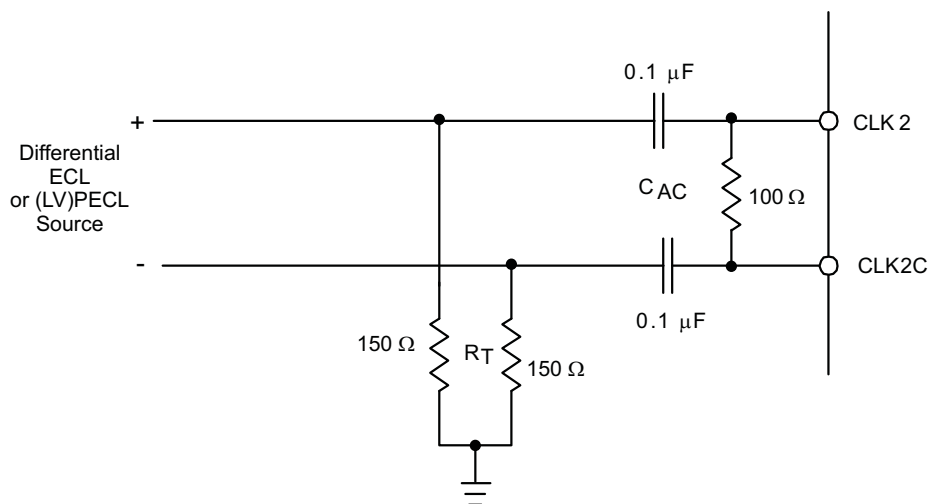


**Figure 40.  Preferred Clock Input Configuration With a Differential ECL/PECL Clock Source**

## CLKO_CLK1 and LOCK_CLK1C Pins

Figure 41 shows the functionality of the CLKO_CLK1 and LOCK_CLK1C pins. Refer to Table 5. The controls for these pins are found in the CONFIG2 register and are used in selection of device clocking mode. In single-ended mode (CONFIG2 **diffclk_ena** = '0') refer to Figure 43, both CLKO_CLK1 and LOCK_CLK1C pins have an internal pull-down resistor approximately equivalent to 100kΩ.
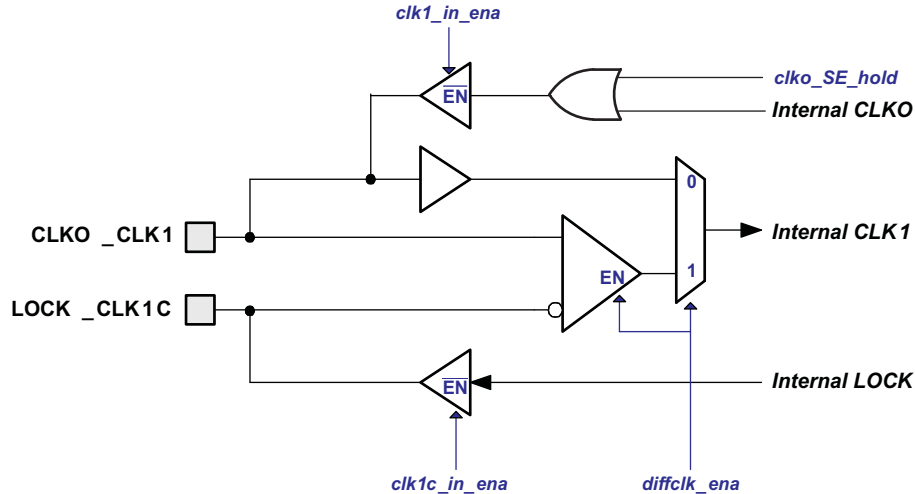


**Figure 41. CLKO_CLK1 and LOCK_CLK1C pins bi-directional control**

In differential mode (CONFIG2 **diffclk_ena** = '1') the CLKO_CLK1 and LOCK_CLK1C input pins are configured as a differential CLK1/C clock input. Refer Figure 39 for the equivalent circuit.
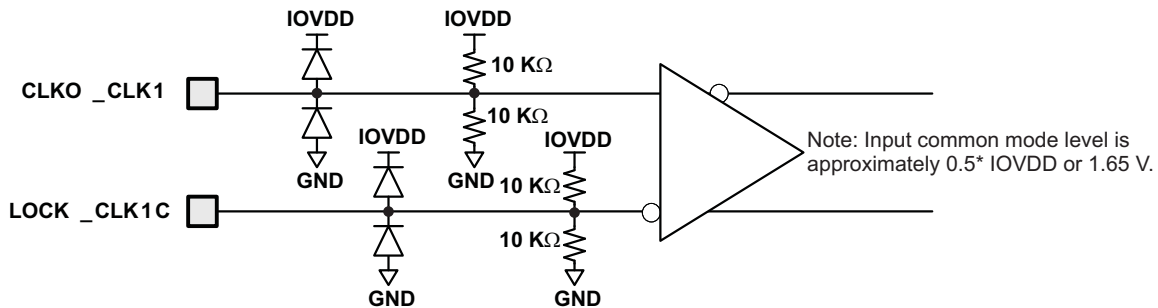


**Figure 42. CLKO_CLK1 and LOCK_CLK1C Differential Input Mode Equivalent Circuit**

Product Folder Link(s): *DAC5688*

## CMOS DIGITAL INPUTS

Figure 43 shows a schematic of the equivalent CMOS digital inputs of the DAC5688. SDIO, SCLK, SYNC, TXENABLE, DA[15:0] and DB[15:0] have pull-down resistors while RESETB and SDENB have pull-up resistors internal the DAC5688. See specification table for logic thresholds. The pull-up and pull-down circuitry is approximately equivalent to 100kΩ.

The input switches levels for all CMOS digital inputs can be changed from 3.3V input levels to 1.8V input levers by programming the CONFIG26 **io_1p8_3p3** register bit. If **io_1p8_3p3** is cleared, the input thresholds are set for 3.3V CMOS levels. If **io_1p8_3p3** is set, the input thresholds are set for 1.8V levels.
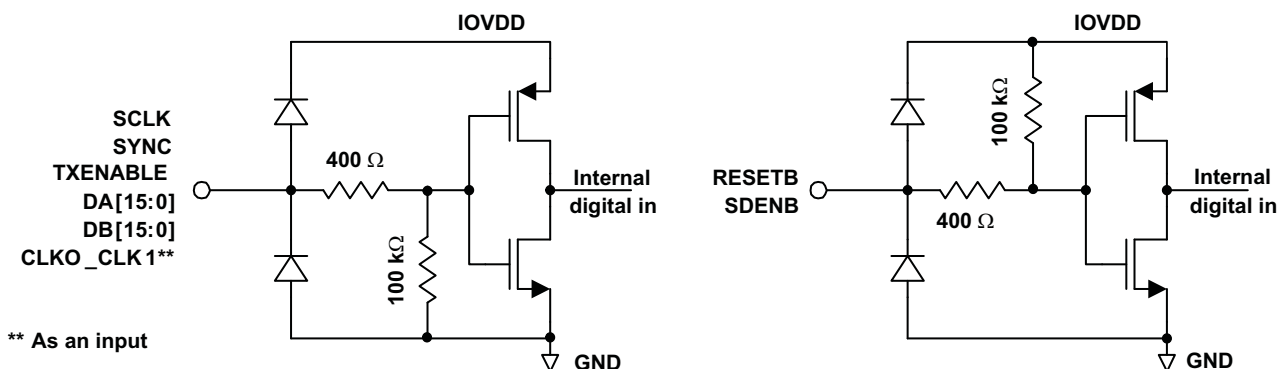


**Figure 43. CMOS/TTL Digital Equivalent Input**

## REFERENCE OPERATION

The DAC5688 uses a bandgap reference and control amplifier for biasing the full-scale output current. The full-scale output current is set by applying an external resistor $R_{BIAS}$ to pin BIASJ. The bias current $I_{BIAS}$ through resistor $R_{BIAS}$ is defined by the on-chip bandgap reference voltage and control amplifier. The default full-scale output current equals 16 times this bias current and can thus be expressed as:

$$IOUT_{FS} = 16 \times I_{BIAS} = 16 \times V_{EXTIO} / R_{BIAS}$$

Each DAC has a 4-bit independent coarse gain control via **coarse_daca(3:0)** and **coarse_dacb (3:0)** in the CONFIG27 register. Using gain control, the $IOUT_{FS}$ can be expressed as:

$$IOUTA_{FS} = (DACA\_gain + 1) \times I_{BIAS} = (DACA\_gain + 1) \times V_{EXTIO} / R_{BIAS}$$
$$IOUTB_{FS} = (DACB\_gain + 1) \times I_{BIAS} = (DACB\_gain + 1) \times V_{EXTIO} / R_{BIAS}$$

where $V_{EXTIO}$ is the voltage at terminal EXTIO. The bandgap reference voltage delivers an accurate voltage of 1.2 V. This reference is active when terminal EXTLO is connected to AGND. An external decoupling capacitor $C_{EXT}$ of 0.1 μF should be connected externally to terminal EXTIO for compensation. The bandgap reference can additionally be used for external reference operation. In that case, an external buffer with high impedance input should be applied in order to limit the bandgap load current to a maximum of 100 nA. The internal reference can be disabled and overridden by an external reference by connecting EXTLO to AVDD. Capacitor $C_{EXT}$ may hence be omitted. Terminal EXTIO thus serves as either input or output node.

The full-scale output current can be adjusted from 20 mA down to 2 mA by varying resistor $R_{BIAS}$ or changing the externally applied reference voltage. The internal control amplifier has a wide input range, supporting the full-scale output current range of 20 dB.

## DAC TRANSFER FUNCTION

The CMOS DAC's consist of a segmented array of NMOS current sinks, capable of sinking a full-scale output current up to 20 mA. Differential current switches direct the current to either one of the complementary output nodes IOUT1 or IOUT2. (DACA = IOUTA1 or IOUTA2 and DACB = IOUTB1 or IOUTB2.) Complementary output currents enable differential operation, thus canceling out common mode noise sources (digital feed-through, on-chip and PCB noise), dc offsets, even order distortion components, and increasing signal output power by a factor of two.

The full-scale output current is set using external resistor RBIAS in combination with an on-chip bandgap voltage reference source (+1.2 V) and control amplifier. Current $I_{BIAS}$ through resistor $R_{BIAS}$ is mirrored internally to provide a maximum full-scale output current equal to 16 times $I_{BIAS}$.

The relation between IOUT1 and IOUT2 can be expressed as:

$IOUT1 = - IOUT_{FS} - IOUT2$

We will denote current flowing into a node as – current and current flowing out of a node as + current. Since the output stage is a current sink the current can only flow from AVDD into the IOUT1 and IOUT2 pins. The output current flow in each pin driving a resistive load can be expressed as:

$IOUT1 = IOUT_{FS} \times (65536 - CODE) / 65536$

$IOUT2 = IOUT_{FS} \times CODE / 65536$

where CODE is the decimal representation of the DAC data input word.

For the case where IOUT1 and IOUT2 drive resistor loads $R_L$ directly, this translates into single ended voltages at IOUT1 and IOUT2:

$VOUT1 = AVDD - | IOUT1 | \times R_L$

$VOUT2 = AVDD - | IOUT2 | \times R_L$

Assuming that the data is full scale (65536 in offset binary notation) and the $R_L$ is 25 Ω, the differential voltage between pins IOUT1 and IOUT2 can be expressed as:

$VOUT1 = AVDD - | -0mA | \times 25\ Ω = 3.3\ V$

$VOUT2 = AVDD - | -20mA | \times 25\ Ω = 2.8\ V$

$VDIFF = VOUT1 - VOUT2 = 0.5V$

Note that care should be taken not to exceed the compliance voltages at node IOUT1 and IOUT2, which would lead to increased signal distortion.

## DAC OUTPUT SINC RESPONSE

Due to sampled nature of a high-speed DAC's, the well known sin(x)/x (or SINC) response can significantly attenuate higher frequency output signals. Refer to Figure 44 which shows the unitized SINC attenuation roll-off with respect to the final DAC sample rate in 4 Nyquist zones. For example, if the final DAC sample rate $F_S$ = 1.0 GSPS, then a tone at 440MHz will be attenuated by 3.0dB. Although the SINC response can create challenges in frequency planning, one side benefit is the natural attenuation of Nyquist images. The increased over-sampling ratio of the input data provided by the DAC5688's 2x, 4x and 8x digital interpolation modes improve the SINC roll-off (droop) within the original signal's band of interest.
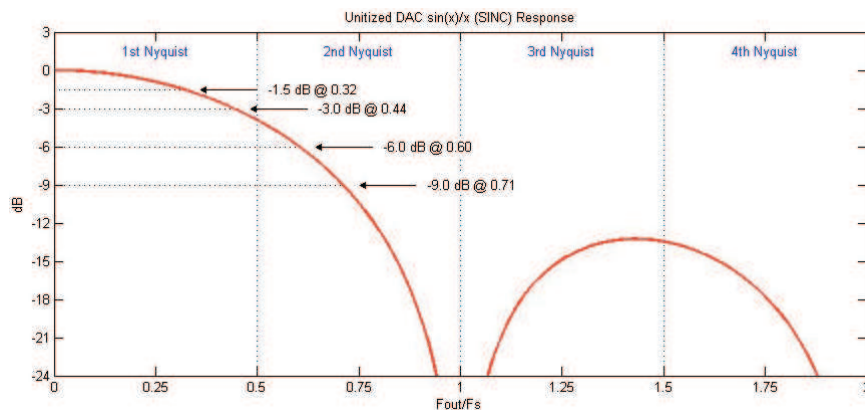


**Figure 44. Unitized DAC sin(x)/x (SINC) Response**

## ANALOG CURRENT OUTPUTS

Figure 45 shows a simplified schematic of the current source array output with corresponding switches. Differential switches direct the current of each individual NMOS current source to either the positive output node IOUT1 or its complementary negative output node IOUT2. The output impedance is determined by the stack of the current sources and differential switches, and is typically >300 kΩ in parallel with an output capacitance of 5 pF.

The external output resistors are referred to an external ground. The minimum output compliance at nodes IOUT1 and IOUT2 is limited to AVDD – 0.5 V, determined by the CMOS process. Beyond this value, transistor breakdown may occur resulting in reduced reliability of the DAC5688 device. The maximum output compliance voltage at nodes IOUT1 and IOUT2 equals AVDD + 0.5 V. Exceeding the minimum output compliance voltage adversely affects distortion performance and integral non-linearity. The optimum distortion performance for a single-ended or differential output is achieved when the maximum full-scale signal at IOUT1 and IOUT2 does not exceed 0.5 V.
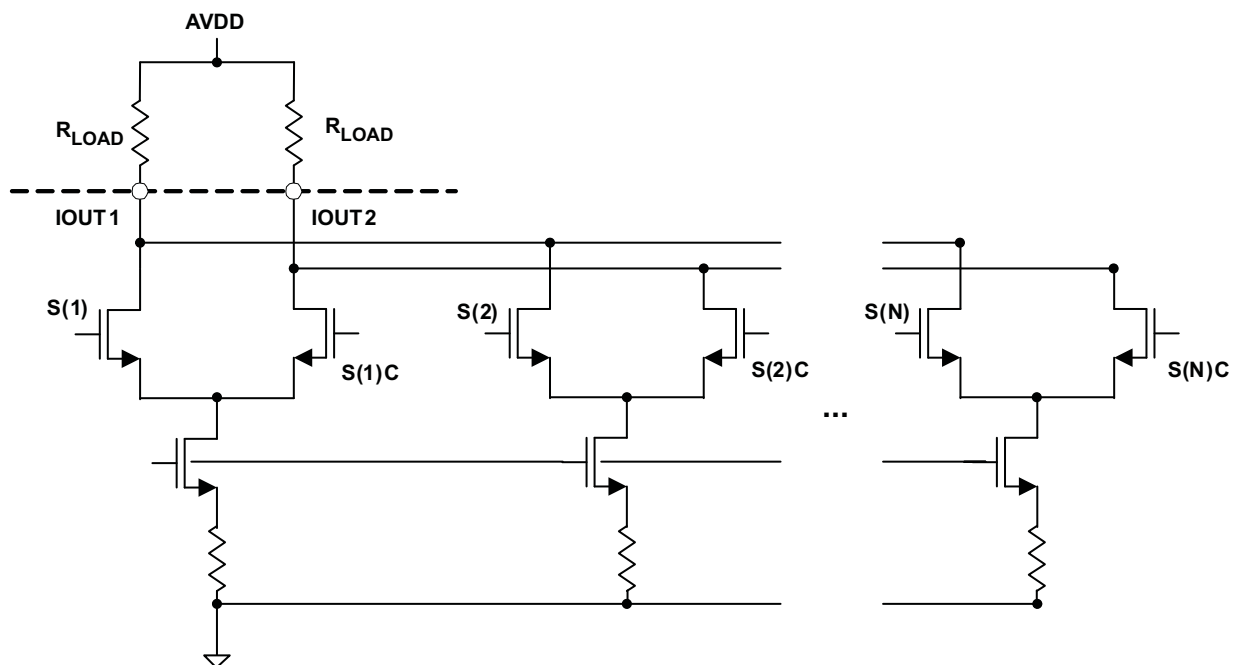


**Figure 45. Equivalent Analog Current Output**

The DAC5688 can be easily configured to drive a doubly terminated 50Ω cable using a properly selected RF transformer. Figure 46 and Figure 47 show the 50Ω doubly terminated transformer configuration with 1:1 and 4:1 impedance ratio, respectively. Note that the center tap of the primary input of the transformer has to be connected to AVDD to enable a cd current flow. Applying a 20mA full-scale output current would lead to a 0.5 $V_{PP}$ for a 1:1 transformer and a 1 $V_{PP}$ output for a 4:1 transformer. The low dc-impedance between IOUT1 or IOUT2 and the transformer center tap sets the center of the ac-signal at AVDD, so the 1 $V_{PP}$ output for the 4:1 transformer results in an output between AVDD + 0.5 V and AVDD – 0.5 V.

Product Folder Link(s): DAC5688
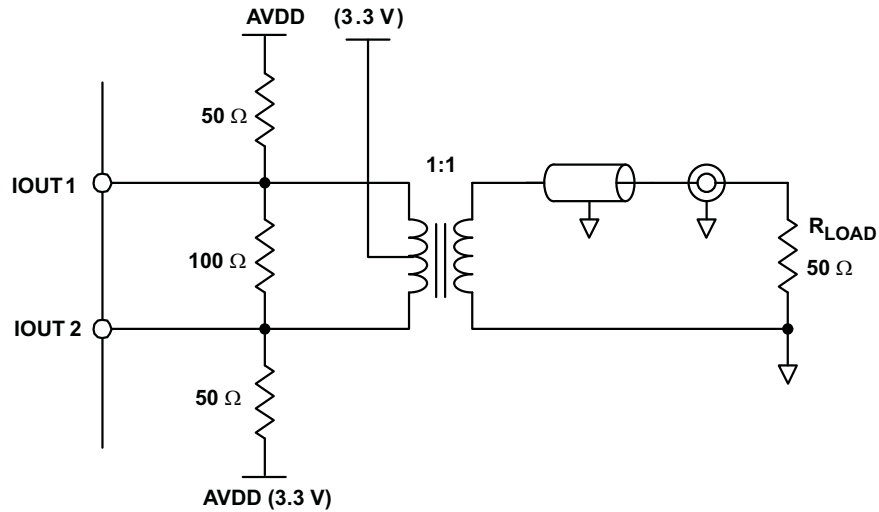
**Figure 46. Driving a Doubly Terminated 50Ω Cable Using a 1:1 Impedance Ratio Transformer**
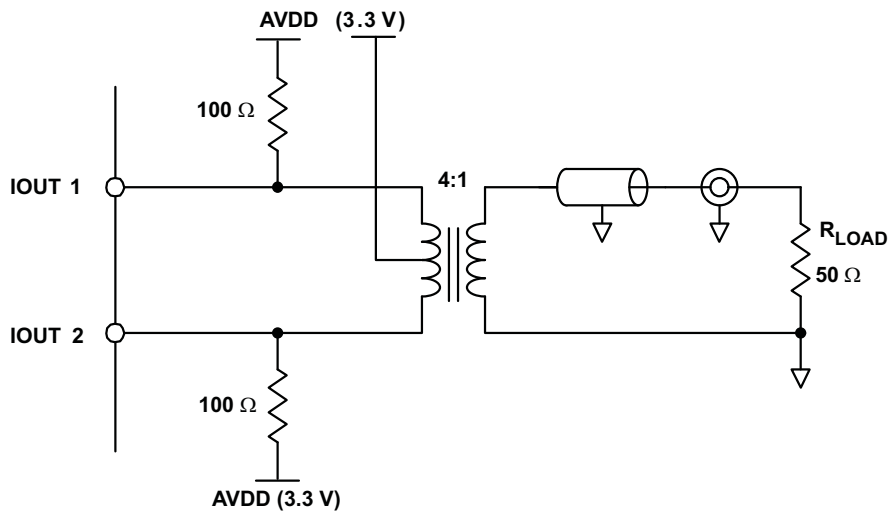


**Figure 47. Driving a Doubly Terminated 50Ω Cable Using a 4:1 Impedance Ratio Transformer**

## PASSIVE INTERFACE TO ANALOG QUADRATURE MODULATORS

A common application in communication systems is to interface the DAC to an IQ modulator like the TRF3703 family of modulators from Texas Instruments. The input of the modulator is generally of high impedance and requires a specific common-mode voltage. A simple resistive network can be used to maintain 50Ω load impedance for the DAC5688 and also provide the necessary common-mode voltages for both the DAC and the modulator.

**V<sub>out</sub> ~ 2.8 to 3.8 V**   **V<sub>in</sub> ~ Varies**
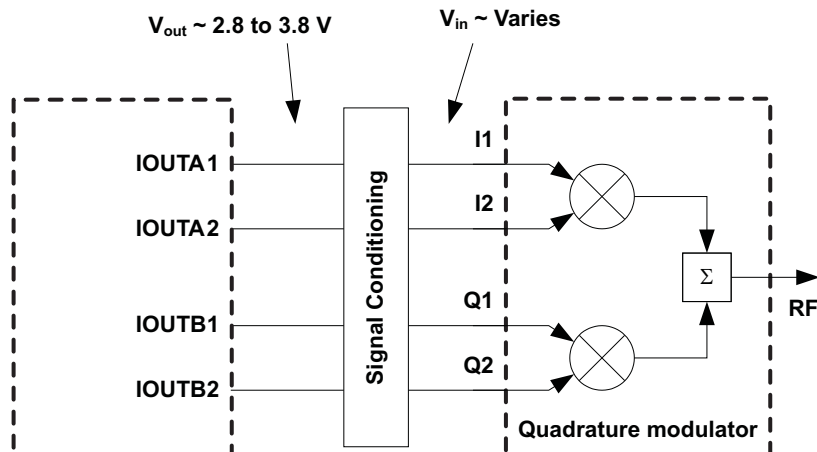


**Figure 48. DAC to Analog Quadrature Modulator Interface**

The DAC5688 has a maximum 20mA full-scale output and a voltage compliance range of AVDD ± 0.5 V. The TRF3703 IQ modulator family can be operated at three common-mode voltages: 1.5V, 1.7V, and 3.3V.

Figure 49 shows the recommended passive network to interface the DAC5688 to the TRF3703-17 which has a common mode voltage of 1.7V. The network generates the 3.3V common mode required by the DAC output and 1.7V at the modulator input, while still maintaining 50Ω load for the DAC.
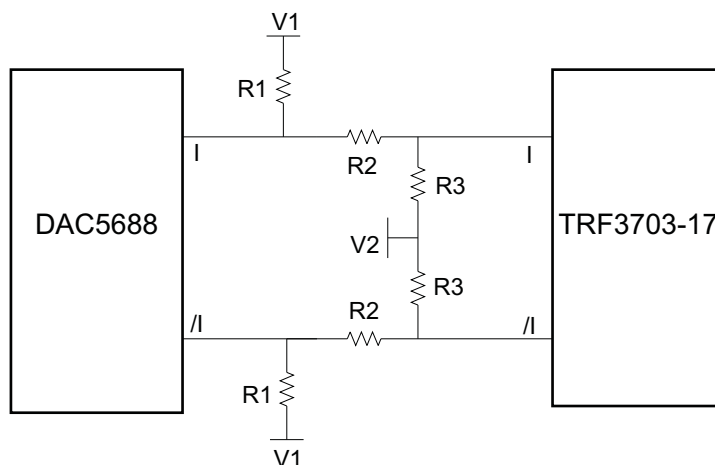


**Figure 49. DAC5688 to TRF3703-17 Interface**

If V1 is set to 5V and V2 is set to -5V, the corresponding resistor values are R1 = 57Ω, R2 = 80Ω, and R3 = 336Ω. The loss developed through R2 is about -1.86 dB. In the case where there is no −5V supply available and V2 is set to 0V, the resistor values are R1 = 66Ω, R2 = 101Ω, and R3 = 107Ω. The loss with these values is −5.76dB.

Figure 50 shows the recommended network for interfacing with the TRF3703-33 which requires a common mode of 3.3V. This is the simplest interface as there is no voltage shift. Because there is no voltage shift there is any loss in the network. With V1 = 5V and V2 = 0V, the resistor values are R1 = 66Ω and R3 = 208Ω.
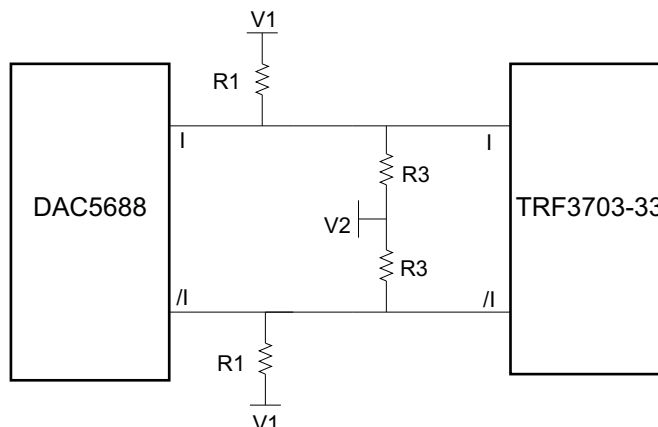
**Figure 50. DAC5688 to TRF3703-33 Interface**

In most applications a baseband filter is required between the DAC and the modulator to eliminate the DAC images. This filter can be placed after the common-mode biasing network. For the DAC to modulator network shown in Figure 51, R2 and the filter load R4 need to be considered into the DAC impedance. The filter has to be designed for the source impedance created by the resistor combination of R3 // (R2+R1). The effective impedance seen by the DAC is affected by the filter termination resistor resulting in R1 // (R2+R3 // (R4/2)).
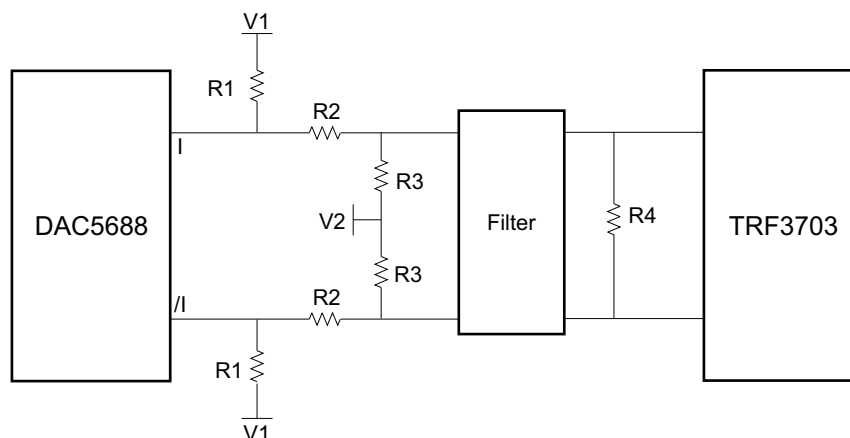


**Figure 51. DAC5688 to Modulator Interface with Filter**

Factoring in R4 into the DAC load, a typical interface to the TRF3703-17 with V1 = 5V and V2 = 0V results in the following values: R1 = 72Ω, R2 = 116Ω, R3 = 124Ω and R4 = 150Ω. This implies that the filter needs to be designed for 75Ω input and output impedance (single-ended impedance). The common mode levels for the DAC and modulator are maintained at 3.3V and 1.7V and the DAC load is 50Ω. The added load of the filter termination causes the signal to be attenuated by −10.8 dB.

A filter can be implemented in a similar manner to interface with the TRF3703-33. In this case it is much simpler to balance the loads and common mode voltages due to the absence of R2. An added benefit is that there is no loss in this network. With V1 = 5V and V2 = 0V the network can be designed such that R1 = 115Ω, R3 = 681Ω, and R4 = 200Ω. This results in a filter impedance of R1 // R2=100Ω, and a DAC load of R1 // R3 // (R4/2) which is equal to 50Ω. R4 is a differential resistor and does not affect the common mode level created by R1 and R3. The common-mode voltage is set at 3.3 V for a full-scale current of 20mA.

For more information on how to interface the DAC5688 to an analog quadrature modulator please refer to the application reports *Passive Terminations for Current Output DACs* (SLAA399) and *Design of Differential Filters for High-Speed Signal Chains* (SLWA053).

Product Folder Link(s): *DAC5688*

## RECOMMENDED STARTUP SEQUENCE

The following startup sequence is recommend to initialization the DAC5688:

1. Supply all 1.8V (CLKVDD, DVDD, VFUSE) and 3.3V (AVDD and IOVDD) voltages.
2. Toggle RESETB pin for a minimum 25 nSec active low pulse width.
3. Provide a stable CLK2/C input clock.
4. Program all desired SIF registers.
5. Provide a sync signal to all digital blocks. The sync input source may be either TXENABLE pin, SYNC pin or a software sync via CONFIG5 **sif_sync_sig** bit; however, only the TXENABLE or SYNC pins are recommended for multi-DAC synchronization. Refer to CONFIG5, CONFIG22 and CONFIG23 registers for sync source selection. Note: Registers CONFIG6 through CONFIG13 all require a sync input to transfer the contents of the control register inputs to the active digital blocks.
6. Provide data flow.

## MULTI-DAC SYNCHRONIZATION

If the system has two or more DACs requiring synchronization, the sync signal in Step 5 of the RECOMMENDED STARTUP SEQUENCE must be provided to all the DACs simultaneously. The sync input source must be either the TXENABLE pin or the SYNC pin (the software sync is not recommended).

In some applications such as beamforming it is required that the multiple DACs in the system have constant latency thus resulting in phase aligned outputs. As a result of the clock domain transfer on the DAC5688 FIFO, the outputs of all DACs can only be synchronized to within ±1 DAC clock cycle in the External and Dual Clock modes. In order to guarantee exact phase alignment between all devices it is required to set up the device in Dual Synchronous Clock mode.

## DESIGNING THE PLL LOOP FILTER

To minimize phase noise given for a given $f_{DAC}$ and M/N, the values of **PLL_gain** and **PLL_range** are selected so that $G_{VCO}$ is minimized and within the MIN and MAX frequency for a given setting.

The external loop filter components C1, C2, and R1 are set by the $G_{VCO}$, M/N, the loop phase margin $\phi_d$ and the loop bandwidth $\omega_d$. Except for applications where abrupt clock frequency changes require a fast PLL lock time, it is suggested that $\phi_d$ be set to at least 80 degrees for stable locking and suppression of the phase noise side lobes. Phase margins of 60 degrees or less can be sensitive to board layout and decoupling details.

See Figure 52 for the recommend external loop filter topology. C1, C2, and R1 are calculated by the following equations

$$C1 = \tau1\left(1 - \frac{\tau2}{\tau3}\right) \qquad C2 = \frac{\tau1 - \tau2}{\tau3} \qquad R1 = \frac{\tau3^2}{\tau1(\tau3 - \tau2)}$$

(5)

where

$$\tau1 = \frac{K_d K_{vco}}{\omega_d^2}\left(\tan\phi_d + \sec\phi_d\right) \qquad \tau2 = \frac{1}{\omega_d\left(\tan\phi_d + \sec\phi_d\right)} \qquad \tau3 = \frac{\tan\phi_d + \sec\phi_d}{\omega_d}$$

(6)

charge pump current: $I_{qp}$ = 1 mA
vco gain: $K_{VCO} = 2\pi \times G_{VCO}$ rad/V
PFD Frequency: $\omega_d \leq$ 160 MHz
phase detector gain: $K_d = I_{qp} \div (2 \times \pi \times M)$ A/rad

An Excel spreadsheet is provided by Texas Instruments for automatically calculating the values for C1, R1 and C2.
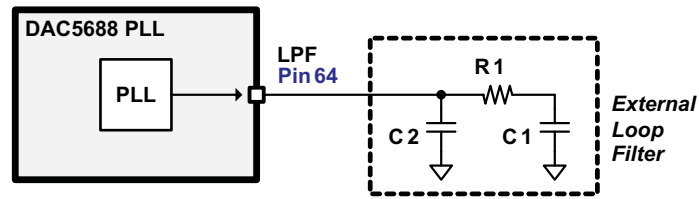


**Figure 52. Recommended External Loop Filter Topology**

# REVISION HISTORY

NOTE: Page numbers of previous versions may differ from current version.

**Changes from Revision B (August 2010) to Revision C**         **Page**

Product Folder Link(s): *DAC5688*

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| DAC5688IRGCR | ACTIVE | VQFN | RGC | 64 | 2000 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | DAC5688I | Samples |
| DAC5688IRGCT | ACTIVE | VQFN | RGC | 64 | 250 | RoHS & Green | NIPDAU \| NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | DAC5688I | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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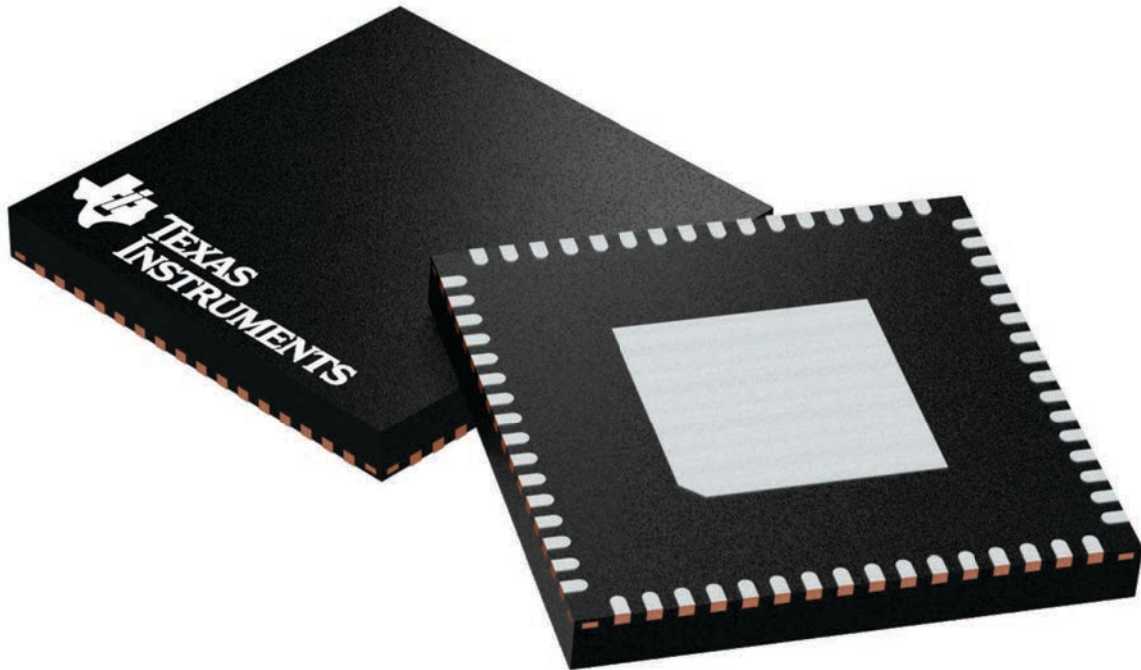
**RGC 64**

**9 x 9, 0.5 mm pitch**
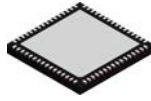
Images above are just a representation of the package family, actual package may vary.
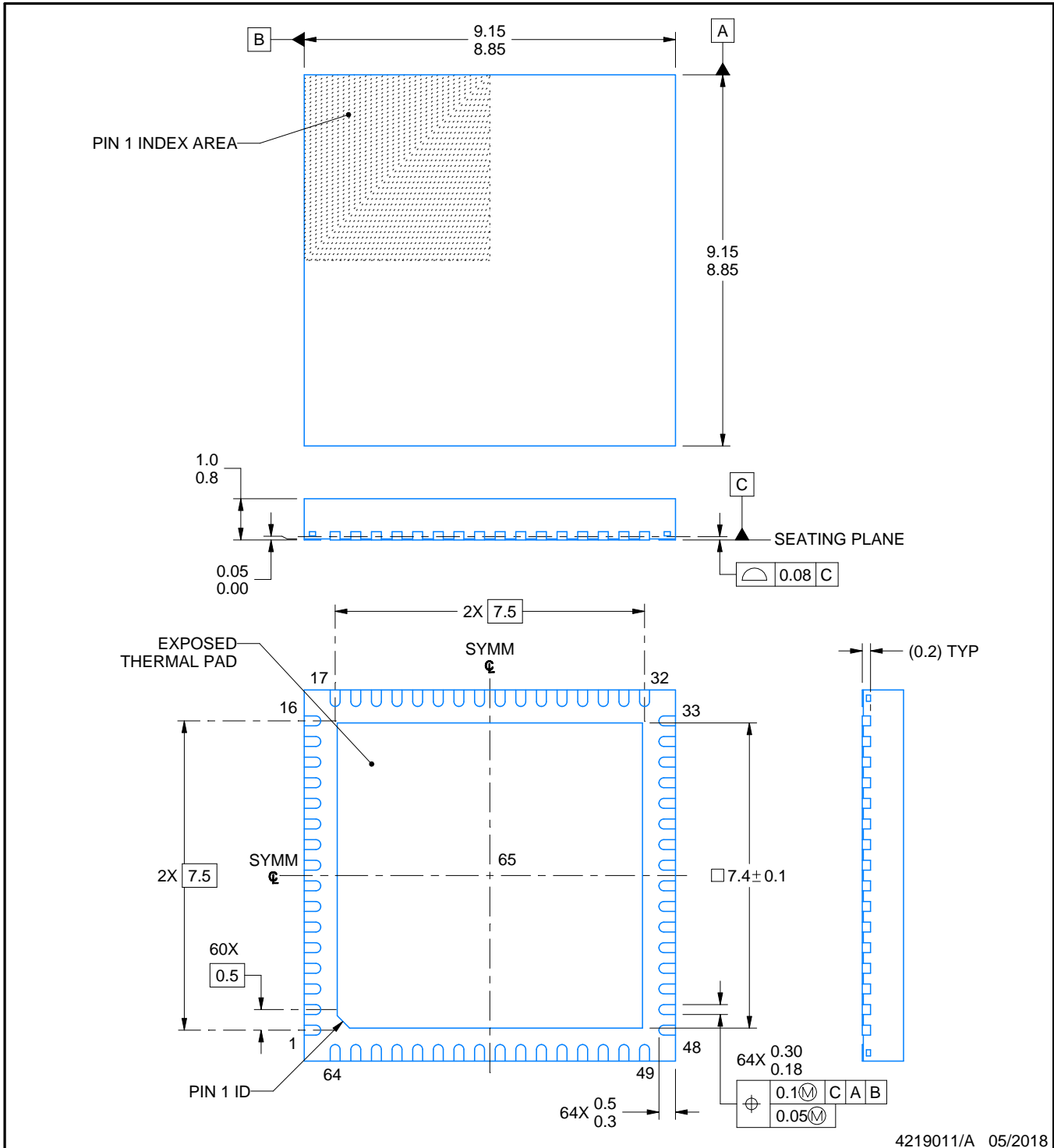Refer to the product data sheet for package details.

4224597/A

B

9.15
8.85

A

PIN 1 INDEX AREA

9.15
8.85

1.0
0.8

C

SEATING PLANE

0.05
0.00

$\bigtriangleup$ | 0.08 | C

2X | 7.5

EXPOSED
THERMAL PAD

SYMM
¢

17

32

16

33

SYMM
¢

2X | 7.5

65

□ 7.4 ± 0.1

(0.2) TYP

60X
0.5

1

48

64X | 0.30
0.18

64

49

PIN 1 ID

64X | 0.5
0.3

⊕ | 0.1 Ⓜ | C | A | B
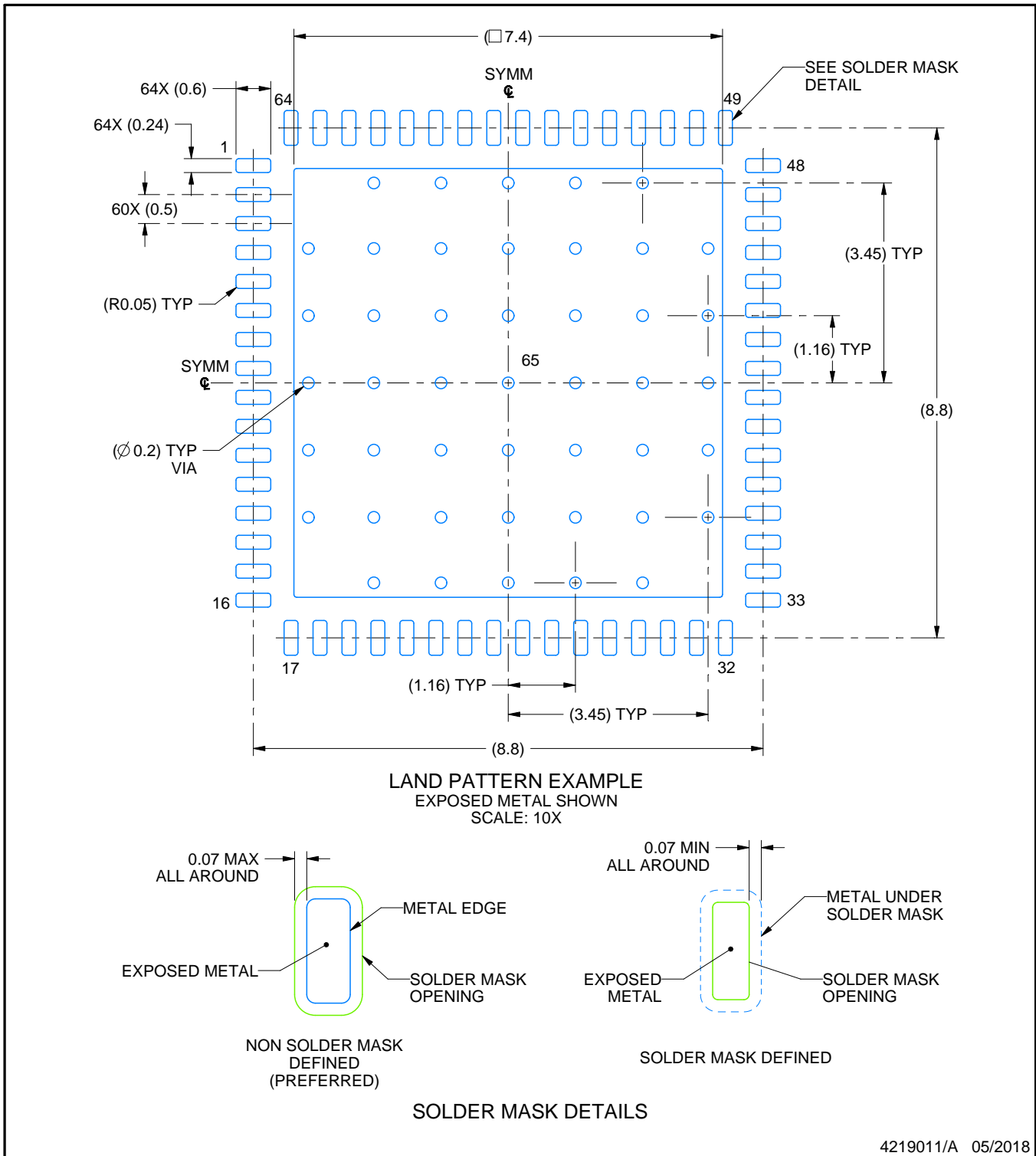0.05 Ⓜ

4219011/A   05/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SEE SOLDER MASK DETAIL

64X (0.6)
64X (0.24)
60X (0.5)
(R0.05) TYP
SYMM
(⌀ 0.2) TYP VIA
(☐ 7.4)
SYMM
(3.45) TYP
(1.16) TYP
(8.8)
65
(1.16) TYP
(3.45) TYP
(8.8)

0.07 MAX
ALL AROUND

METAL EDGE

EXPOSED METAL

SOLDER MASK
OPENING

NON SOLDER MASK
DEFINED
(PREFERRED)

0.07 MIN
ALL AROUND

METAL UNDER
SOLDER MASK

EXPOSED
METAL

SOLDER MASK
OPENING

SOLDER MASK DEFINED

SOLDER MASK DETAILS
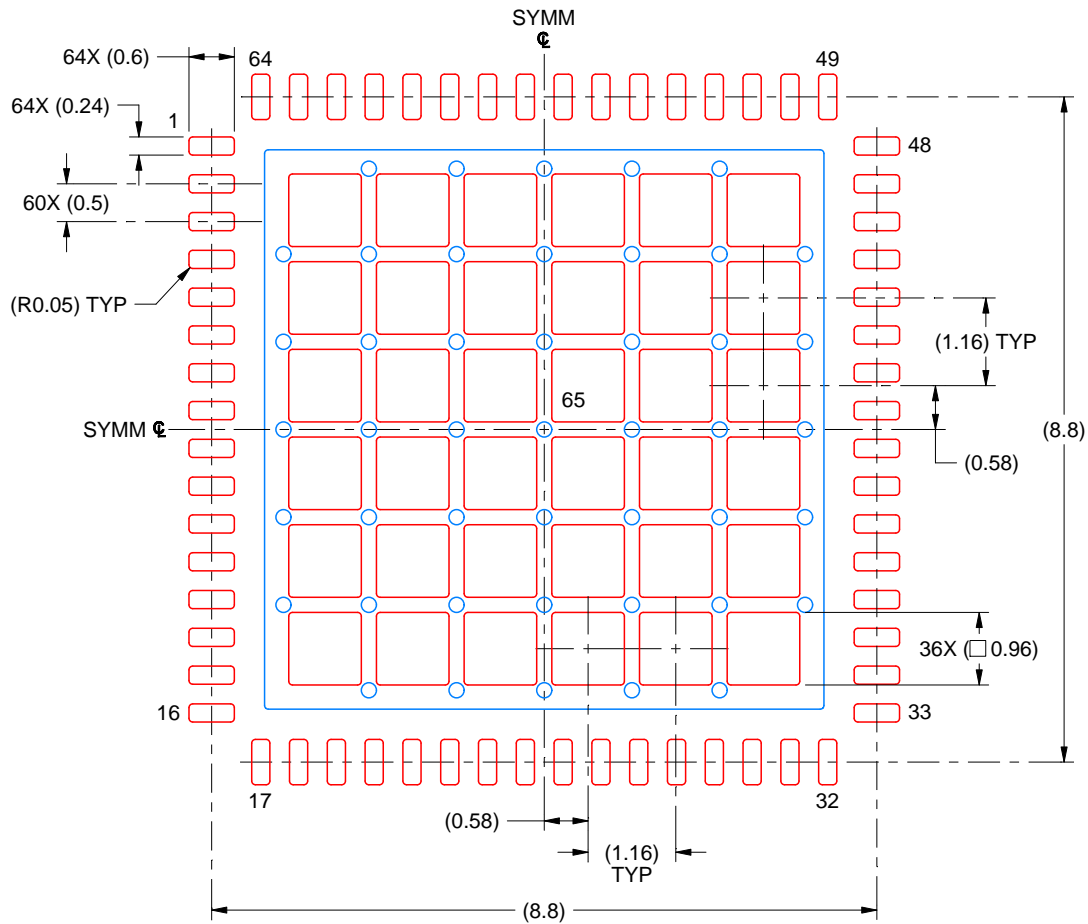
4219011/A   05/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 10X

EXPOSED PAD 65
61% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4219011/A   05/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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