LED DRIVER

Check for Samples: TLC5922

FEATURES

- 16 Channels
- Drive Capability
  - 0 to 80 mA (Constant-Current Sink)
- Constant Current Accuracy
  - ±1% (typical)
- Serial Data Interface, SPI Compatible
- Fast Switching Output: T_r / T_f = 10ns (typical)
- CMOS Level Input/Output
- 30 MHz Data Transfer Rate
- V_{CC} = 3.0 V to 5.5 V
- Operating Temperature = –20°C to 85 °C
- LED Supply Voltage up to 17 V
- 32-pin HTSSOP (PowerPAD™) Package
- Dot Correction
  - 7 bit (128 Steps)
  - Individually Adjustable For Each Channel
- Controlled In-Rush Current

APPLICATIONS

- Monocolor, Multicolor, Fullcolor LED Display
- Monocolor, Multicolor LED Signboard
- Display Backlighting
- Multicolor LED Lighting Applications

DESCRIPTION

The TLC5922 is a 16-channel constant-current sink driver. Each channel has an On/Off state and a 128-step adjustable constant-current sink (dot correction). The dot correction adjusts the brightness variations between LED, LED channels, and other LED drivers. Both dot correction and On/Off state are accessible via a serial data interface. A single external resistor sets the maximum current of all 16 channels.

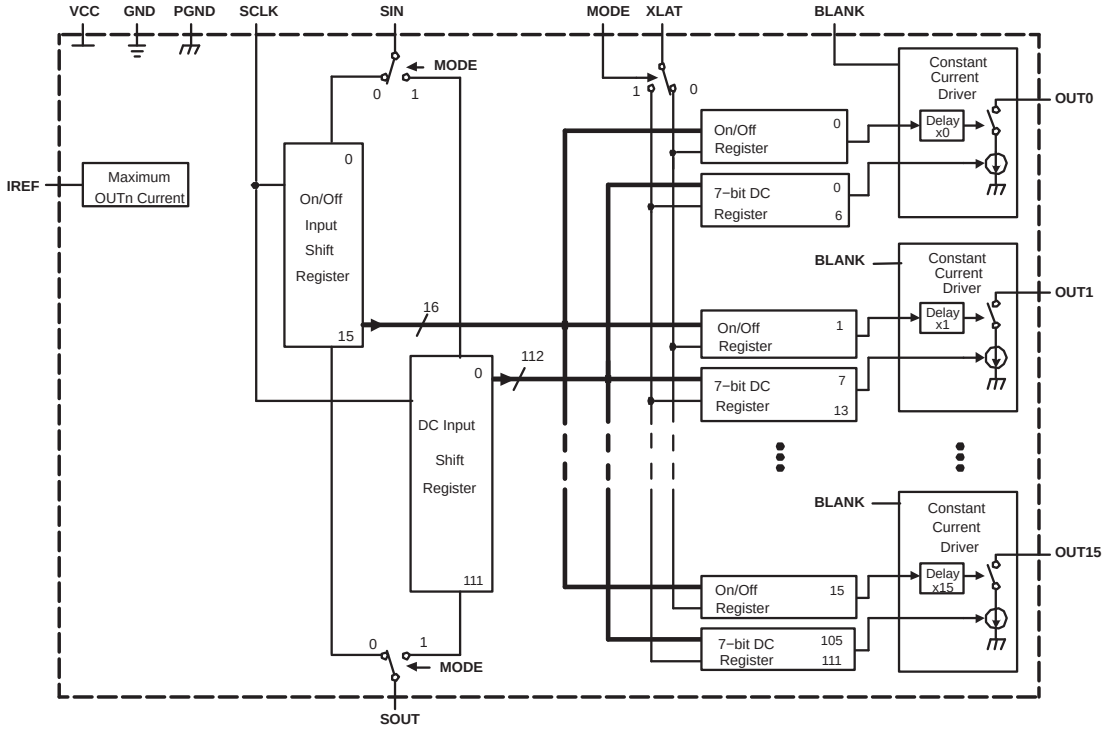


Figure 1. Functional Block Diagram

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

T_A	Package	Part Number (2)
–20 °C to 85 °C	4 mm x 4 mm, 32-pin HTSSOP	TLC5922DAP

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
(2) The DAP package is available in tape and reel. Add R suffix (TLC5922DAPR) to order quantities of 2000 parts per reel.

ABSOLUTE MAXIMUM RATINGS (1) (2)

			TLC5922	UNIT
V_{CC}	Supply voltage(2)		–0.3 to 6	V
I_O	Output current (dc)	$I_{L(LC)}$	90	mA
V_I	Input voltage range(2)	$V_{(BLANK)}$, $V_{(XLAT)}$, $V_{(SCLK)}$, $V_{(SIN)}$, $V_{(MODE)}$	–0.3 to V_{CC} + 0.3	V
V_O	Output voltage range(2)	$V_{(SOUT)}$	–0.3 to V_{CC} + 0.3	V
		$V_{(OUT0)}$ – $V_{(OUT15)}$	–0.3 to 18	V
	ESD rating	HBM (JEDEC JESD22-A114, Human Body Model)	2	kV
		CDM (JEDEC JESD22-C101, Charged Device Model)	500	V
T_{stg}	Storage temperature range		–40 to 150	°C
	Continuous total power dissipation at (or below) T_A = 25°C		3.9	W
	Power dissipation rating at (or above) T_A = 25°C		31.4	mW/°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

RECOMMENDED OPERATING CONDITIONS
DC Characteristics

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		5.5	V
V_O	Voltage applied to output, (Out0 - Out15)				17	V
V_{IH}	High-level input voltage		0.8 VCC		VCC	V
V_{IL}	Low-level input voltage		GND		0.2 VCC	V
I_{OH}	High-level output current	V_{CC} = 5 V at SOUT			–1	mA
I_{OL}	Low-level output current	V_{CC} = 5 V at SOUT			1	mA
I_{OLC}	Constant output current	OUT0 to OUT15			80	mA
T_A	Operating free-air temperature range(1)		–20		85	°C

(1) Contact TI sales for slightly extended temperature range.

AC Characteristics

V_{CC} = 3 V to 5.5 V, T_A = –20°C to 85°C (unless otherwise noted)

			MIN	TYP	MAX	UNIT
f_{SCLK}	Clock frequency	SCLK			30	MHz
t_{wh0}/t_{wl0}	CLK pulse duration	SCLK = H/L	16			ns
t_{wh1}	XLAT pulse duration	XLAT = H	20			ns
t_{su0}	Setup time	SIN – SCLK↑	10			ns
t_{su1}		SCLK↑ – XLAT↓	10			ns
t_{su2}		MODE↑↓ – SCLK↑	10			ns
t_{su3}		MODE↑↓ – XLAT↓	10			ns
t_{h0}	Hold time	SCLK↑ – SIN	10			ns
t_{h1}		XLAT↓ – SCLK↑	10			ns
t_{h2}		SCLK↑ – MODE↑↓	10			ns
t_{h3}		XLAT↓ – MODE↑↓	10			ns

ELECTRICAL CHARACTERISTICS

V_{CC} = 3 V to 5.5 V, T_A = –20°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –1 mA, SOUT	V_{CC} –0.5			V
V_{OL}	Low-level output voltage	I_{OL} = 1 mA, SOUT			0.5	V
I_I	Input current	V_I = V_{CC} or GND, BLANK, XLAT, SCLK, SIN, MODE	–1		1	µA
I_{CC}	Supply current	No data transfer, All output OFF, V_O = 1 V, $R_{(IREF)}$ = 10 kΩ			6	mA
		No data transfer, All output OFF, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ			12	
		Data transfer 30 MHz, All output ON, V_O = 1 V, $R_{(IREF)}$ = 1.3 kΩ			25	
		Data transfer 30 MHz, All output ON, V_O = 1 V, $R_{(IREF)}$ = 600 kΩ		36	65 (1)	
I_{OLC}	Constant output current	All output ON, V_O = 1 V, $R_{(IREF)}$ = 600 Ω	70	80	90	mA
I_{LO0}	Leakage output current	All output OFF, V_O = 15 V, $R_{(IREF)}$ = 600 Ω , OUT0 to OUT15			0.1	µA
ΔI_{OLC0}	Constant current error	All output ON, V_O = 1 V, $R_{(IREF)}$ = 600 Ω, OUT0 to OUT15		±1%	±4%	
ΔI_{OLC1}	Constant current error	device to device, averaged current from OUT0 to OUT15, $R_{(IREF)}$ = 600 Ω		±4%	±8.5%	
ΔI_{OLC2}	Power supply rejection ratio	All output ON, V_O = 1 V, $R_{(IREF)}$ = 600 Ω, OUT0 to OUT15		±1	±4	%/V
ΔI_{OLC3}	Load regulation	All output ON, V_O = 1 V to 3 V, $R_{(IREF)}$ = 600 Ω, OUT0 to OUT15		±2	±6	%/V
$V_{(IREF)}$	Reference voltage output	$R_{(IREF)}$ = 600 Ω	1.20	1.24	1.28	V

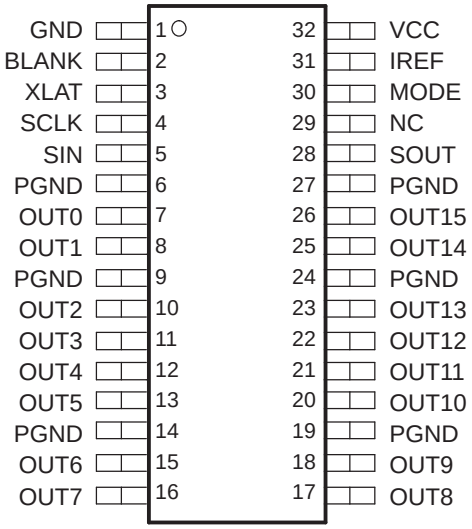
(1) Measured at device start-up temperature. Once the IC is operating (self heating), lower I_{CC} values are seen. See Figure 12 .

SWITCHING CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{r0}	Rise time	SOUT(see (1))			16	ns
t_{r1}		OUTx, V_{CC} = 5 V, T_A = 60°C, DCx = 7F (see (2))		10	30	
t_{f0}	Fall time	SOUT (see (1))			16	ns
t_{f1}		OUTx, V_{CC} = 5 V, T_A = 60°C, DCx = 7F (see (2))		10	30	
t_{pd0}	Propagation delay time	SCLK↑ – SOUT↑ ↓ (see (3))			30	ns
t_{pd1}		MODE↑↓ – SOUT↑↓ (see (3))			30	
t_{pd2}		BLANK↓ – OUT0↑↓ (see (4))			60	
t_{pd3}		XLAT↑ – OUT0↑↓ (see (4))			60	
t_{pd4}		XLAT↑ – I_{OUT}(dot-correction) (see (5))			1000	
t_d	Output delay time	OUTn↑↓ – OUT(n+1)↑↓ (see (4))	14	22	30	ns

(1) See Figure 4 . Defined as from 10% to 90%
(2) See Figure 5 . Defined as from 10% to 90%
(3) See Figure 4 . Figure 10
(4) See Figure 5 and Figure 10
(5) See Figure 5 and Figure 10

DAP PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
BLANK	2	2	Blank (Light OFF). When BLANK = H, All OUTx outputs are forced OFF. When BLANK = L, ON/OFF of OUTx outputs are controlled by input data.
GND	1		Ground
IREF	31	I/O	Reference current terminal
MODE	30	I	Mode select. When MODE = L, SIN, SOUT, SCLK, XLAT are connected to ON/OFF control logic. When MODE = H, SIN, SOUT, SCLK, XLAT are connected to dot-correction logic.
OUT0	7	O	Constant current output
OUT1	8	O	Constant current output
OUT2	10	O	Constant current output
OUT3	11	O	Constant current output
OUT4	12	O	Constant current output
OUT5	13	O	Constant current output

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
OUT6	15	O	Constant current output
OUT7	16	O	Constant current output
OUT8	17	O	Constant current output
OUT9	18	O	Constant current output
OUT10	20	O	Constant current output
OUT11	21	O	Constant current output
OUT12	22	O	Constant current output
OUT13	23	O	Constant current output
OUT14	25	O	Constant current output
OUT15	26	O	Constant current output
PGND	6, 14, 19, 24, 27		Power ground
SCLK	4	I	Data shift clock. Note that the internal connections are switched by MODE (pin #30). At SCLK↑, the shift-registers selected by MODE shift the data.
SIN	5	I	Data input of serial I/F
SOUT	28	O	Data output of serial I/F
VCC	32		Power supply voltage
NC	29	–	Not Connected
XLAT	3	I	Data latch. Note that the internal connections are switched by MODE (pin #30). At XLAT↑, the latches selected by MODE get new data.

PIN EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

(Note: Resistor values are equivalent resistance and not tested).

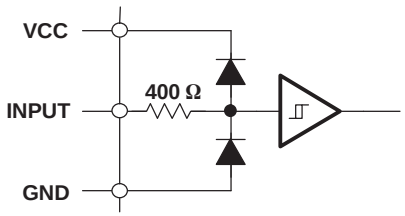


Figure 2. Input Equivalent Circuit (BLANK, XLAT, SCLK, SIN, MODE)

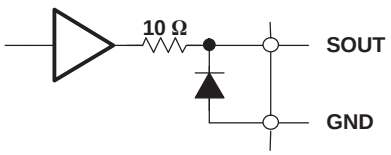


Figure 3. Output Equivalent Circuit

PARAMETER MEASUREMENT INFORMATION

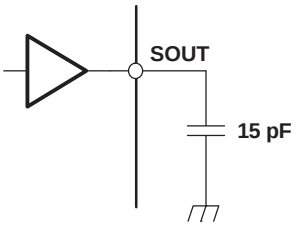


Figure 4. Test Circuit for t_{r0}, t_{f0}, t_{d0}, t_{d1}

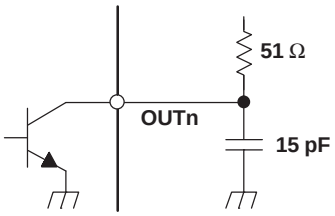


Figure 5. Test Circuit for t_{r1}, t_{f1}, t_{pd2}, t_{pd3}, t_{pd4}

PRINCIPLES OF OPERATION

Setting Maximum Channel Current

The maximum output current per channel is set by a single external resistor, $R_{(IREF)}$, which is placed between IREF and GND. The voltage on IREF is set by an internal band gap $V_{(IREF)}$ with a typical value of 1.24V. The maximum channel current is equivalent to the current flowing through $R_{(IREF)}$ multiplied by a factor of 40. The maximum output current can be calculated by Equation 1:

$$I_{MAX} = \frac{V_{IREF}}{R_{IREF}} \times 40 \quad (1)$$

where:

V_{IREF} = 1.24V typ.

R_{IREF} = User selected external resistor (R_{IREF} should not be smaller than 600 Ω)

Figure 6 shows the maximum output current, $I_{O(LC)}$, versus $R_{(IREF)}$. In Figure 6, $R_{(IREF)}$ is the value of the resistor between IREF terminal to ground, and $I_{O(LC)}$ is the constant output current of OUT0,.....OUT15.

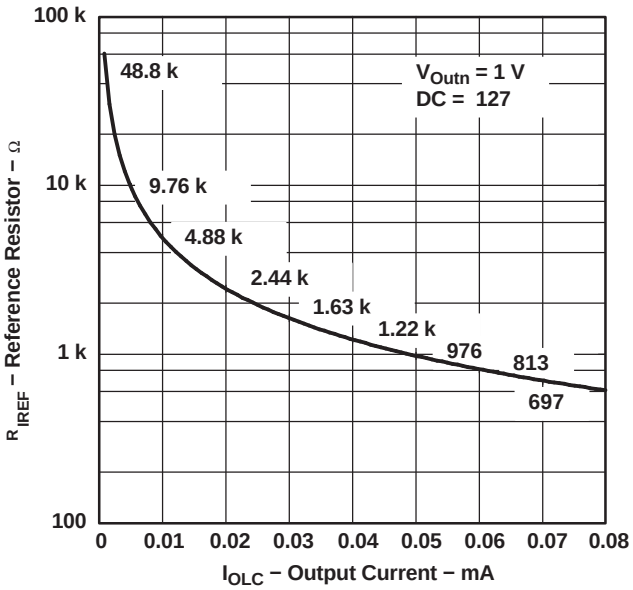


Figure 6. Reference Resistor vs Output Current

Setting Dot-Correction

The TLC5922 has the capability to fine adjust the current of each channel, OUT0 to OUT15 independently. This is also called dot correction. This feature is used to adjust the brightness deviations of LED connected to the output channels OUT0 to OUT15. Each of the 16 channels can be programmed with a 7-bit word. The channel output can be adjusted in 128 steps from 0% to 100% of the maximum output current I_{MAX}. Equation 2 determines the output current for each OUTn:

$$I_{Outn} = \frac{I_{MAX} \times DC_n}{127} \quad (2)$$

where:

I_{Max} = the maximum programmable current of each output

DCn = the programmed dot-correction value for output n (DCn = 0, 1, 2 ...127)

n = 0, 1, 2 ... 15

Dot-correction data are entered for all channels at the same time. The complete dot-correction data format consists of 16 x 7-bit words, which forms a 112-bit wide serial data packet. The channel data is put one after another. All data is clocked in with MSB first. Figure 7 shows the DC data format.

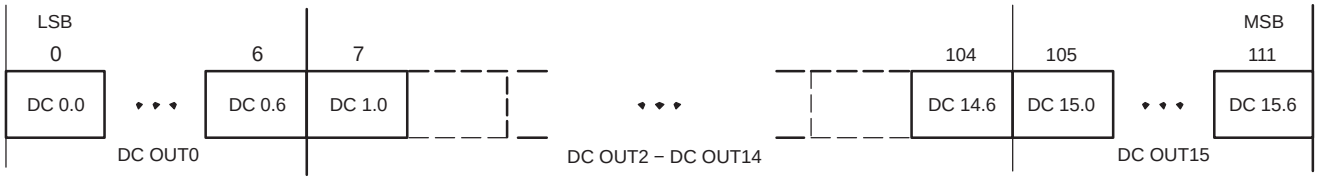


Figure 7. DC Data Format

MODE must be set to high to input data into the dot-correction register. The internal input shift register is then set to 112-bit width. After all serial data is clocked in, a rising edge of XLAT latches the data to the dot-correction register (Figure 10).

Output Enable

All OUTn channels of TLC5922 can switched off with one signal. When BLANK signal is set to high, all OUTn are disabled, regardless of On/Off status of each OUTn. When BLANK is set to low, all OUTn work under normal conditions.

Table 1. BLANK Signal Truth Table

BLANK	OUT0 - OUT15
LOW	Normal condition
HIGH	Disabled

Setting Channel On/Off Status

All OUTn channels of TLC5922 can be switched on or off independently. Each of the channels can be programmed with a 1-bit word. On/Off data are entered for all channels at the same time. The complete On/Off data format consists of 16 x 1-bit words, which form a 16-bit wide data packet. The channel data is put one after another. All data is clocked in with MSB first. Figure 8 shows the On/Off data format.

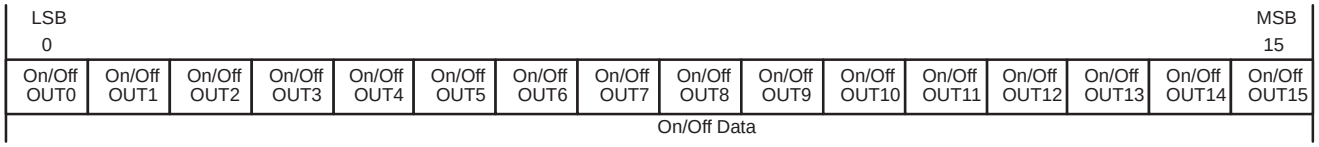


Figure 8. On/Off Data

MODE must be set to low to input On/Off data into the On/Off register. The internal input shift register is then set to 16-bit width. After all serial data is clocked in, a rising edge of XLAT, during BLANK = high, is used to latch data into the On/Off register. Figure 10 shows the On/Off data input timing chart.

Delay Between Outputs

The TLC5922 has graduated delay circuits between outputs. These delay circuits can be found in the constant current block of the device (see Figure 1). The fixed delay time is 20 ns (typical), OUT0 has no delay, OUT1 has 20-ns delay, OUT2 has 40-ns delay, etc. This delay prevents large inrush currents, which reduce power supply bypass capacitor requirements when the outputs turn on.

Serial Interface Data Transfer Rate

The TLC5922 includes a flexible serial interface, which can be connected to a microcontroller or digital signal processor. Only 3 pins are required to input data into the device. The rising edge of SCLK signal shifts the data from SIN pin to internal shift register. After all data is clocked in, a rising edge of XLAT latches the serial data to the internal registers. All data is clocked in with MSB first. Multiple TLC5922 devices can be cascaded by connecting SOUT pin of one device to the SIN pin of following device.

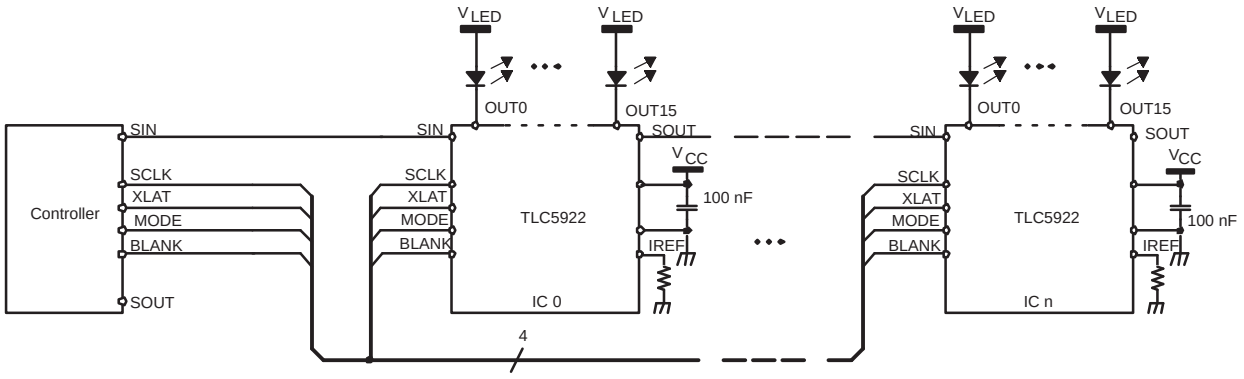


Figure 9. Cascading Devices

Figure 9 shows an example application with *n* cascaded TLC5922 devices connected to a controller. The maximum number of cascaded TLC5922 devices depends on the application system, and data transfer rate. Equation 3 calculates the minimum data input frequency needed.

$$f\_(SCLK) = 112 \times f\_(update) \times n \quad (3)$$

where:

f_(SCLK): The minimum data input frequency for SCLK and SIN.

f_(update): The update rate of the whole cascaded system.

n: The number of cascaded TLC5922 devices.

Operating Modes

The TLC5922 has different operating modes, depending on the MODE signal. Table 2 shows the available operating modes.

Table 2. TLC5922 Operating Modes Truth Table

MODE SIGNAL	INPUT SHIFT REGISTER	MODE
LOW	16 bit	On/Off Mode
HIGH	112 bit	Dot-Correction Data Input Mode

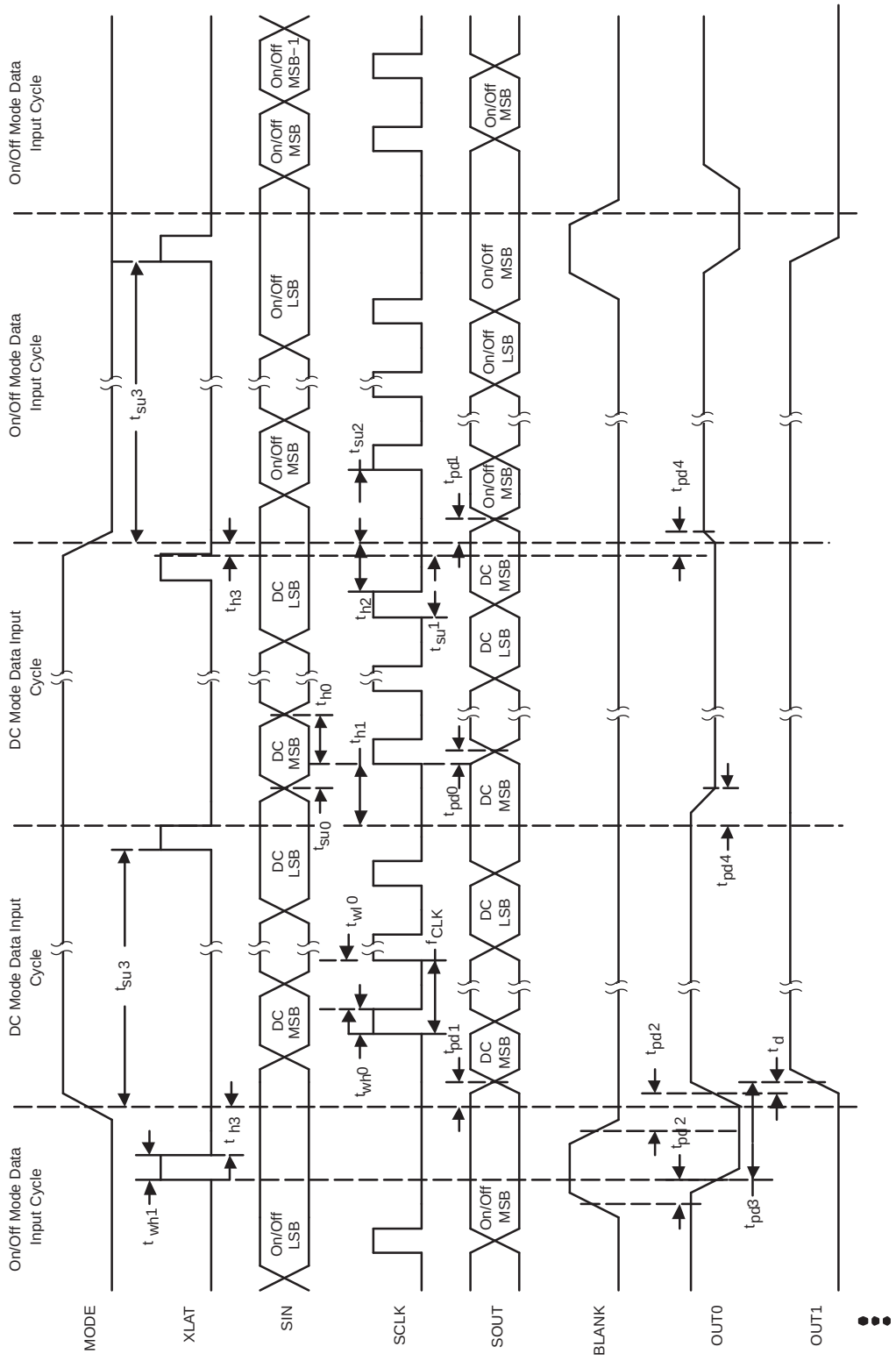


Figure 10. Timing Chart Example for ON/OFF Setting to Dot-Correction

Power Rating - Free-Air Temperature

Figure 11 shows total power dissipation. Figure 12 shows supply current versus free-air temperature.

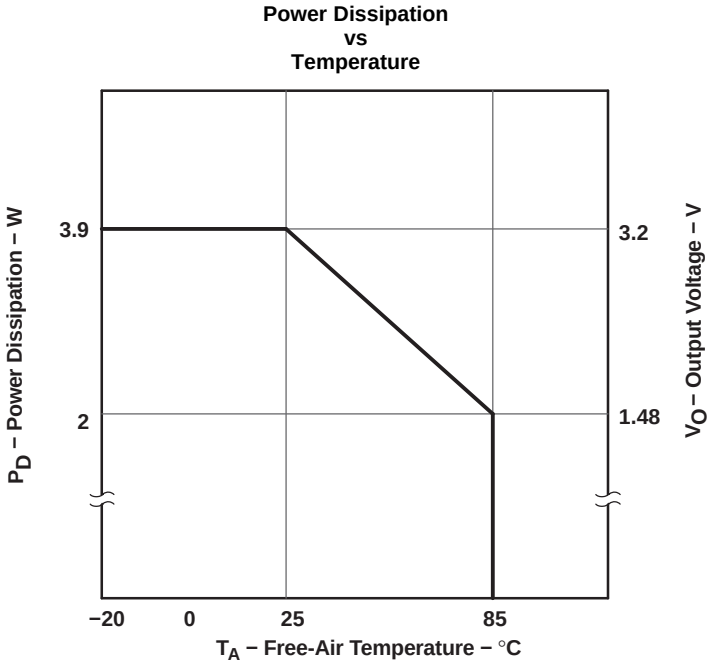
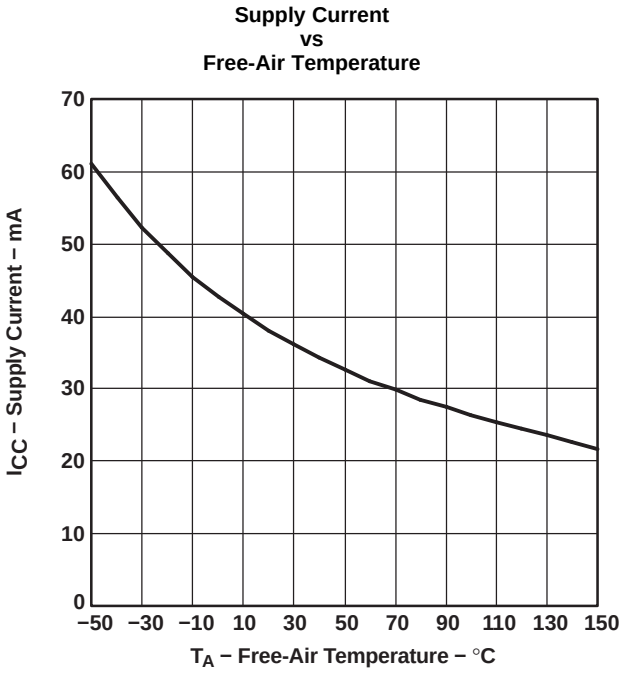


Figure 11.



Data Transfer = 30 MHz / All Outputs, ON/VO = 1 V / RIREF = 600 Ω / AVDD = 5 V

Figure 12.

REVISION HISTORY

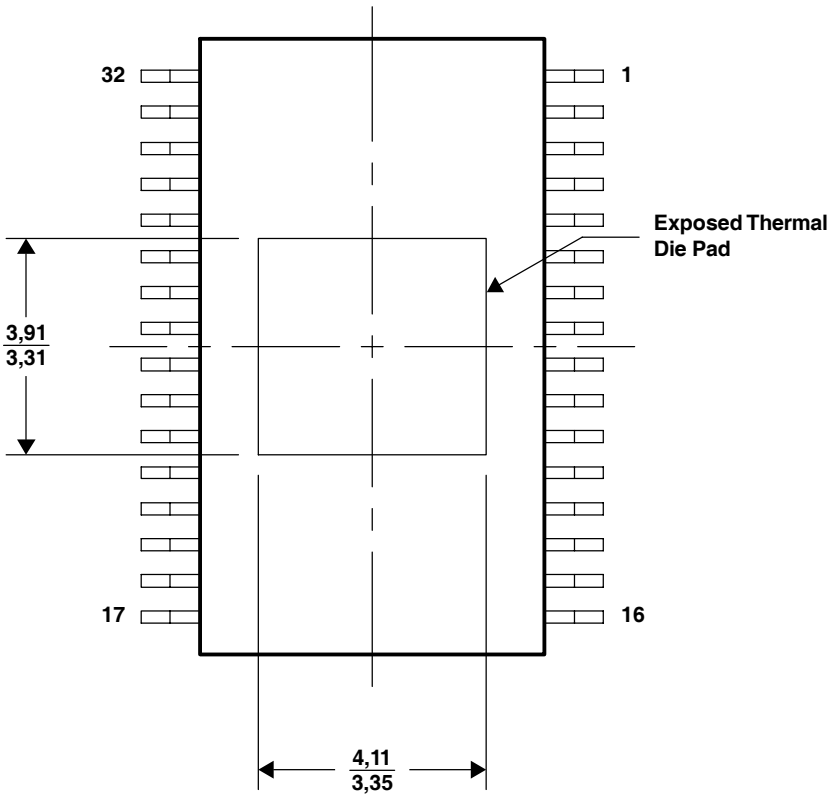
NOTE: Page numbers of current version may differ from previous versions.

Changes from Revision A (March 2005) to Revision B	Page
• Changed Propogation delay time t_{PD0} and t_{PD1} from 300 ns MAX(typographical error) to 30 ns MAX	4

THERMAL INFORMATION

The DAP PowerPAD™ package incorporates an exposed thermal die pad that is designed to be attached directly to an external heat sink. When the thermal die pad is soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal die pad can be attached directly to a ground plane or special heat sink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, *PowerPAD Thermally Enhanced Package*, Texas Instruments Literature No. SLMA002 and Application Brief, *PowerPAD Made Easy*, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com. See Figure 1 for DAP package exposed thermal die pad dimensions.



NOTE: All linear dimensions are in millimeters.

Figure 1. DAP Package Exposed Thermal Die Pad Dimensions

PowerPAD is a trademark of Texas Instruments.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC5922DAP	ACTIVE	HTSSOP	DAP	32	46	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-20 to 85	TLC5922	Samples
TLC5922DAPG4	ACTIVE	HTSSOP	DAP	32	46	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-20 to 85	TLC5922	Samples
TLC5922DAPR	ACTIVE	HTSSOP	DAP	32	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-20 to 85	TLC5922	Samples
TLC5922DAPRG4	ACTIVE	HTSSOP	DAP	32	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-20 to 85	TLC5922	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

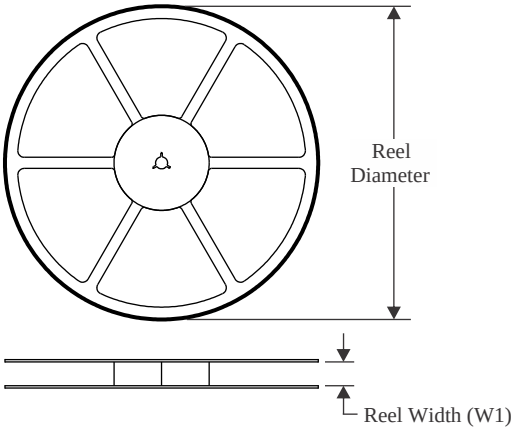
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

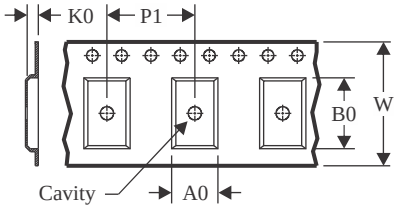
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

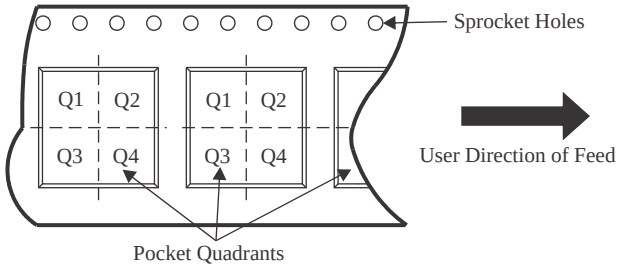


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

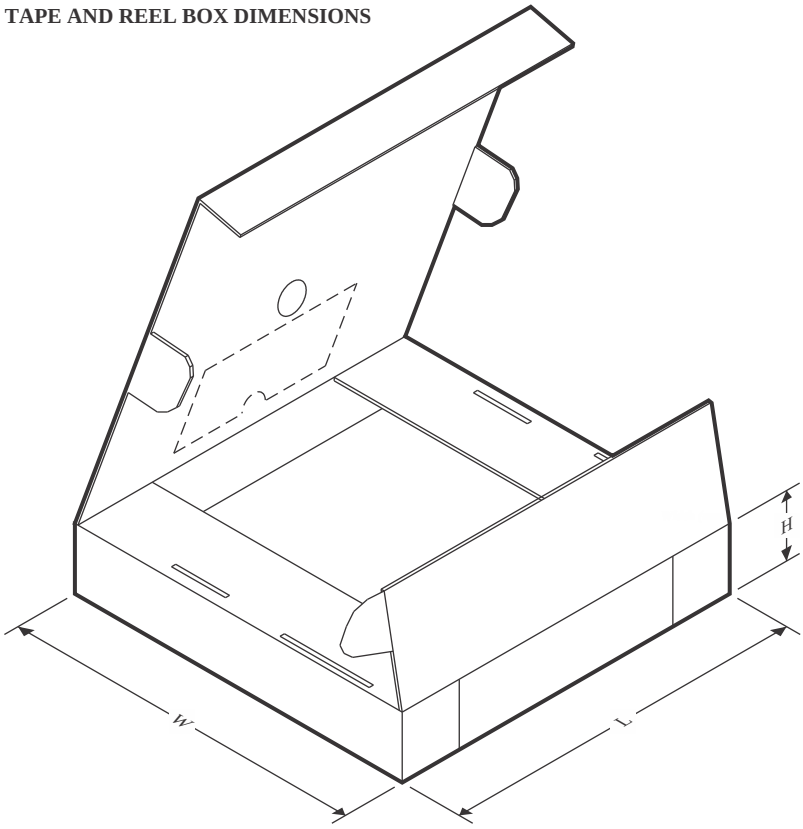
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5922DAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1

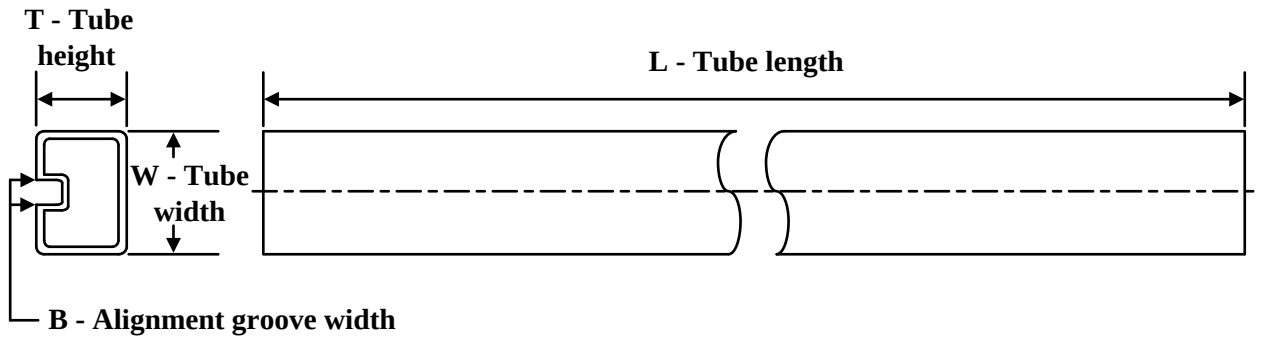
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5922DAPR	HTSSOP	DAP	32	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TLC5922DAP	DAP	HTSSOP	32	46	530	11.89	3600	4.9
TLC5922DAPG4	DAP	HTSSOP	32	46	530	11.89	3600	4.9

GENERIC PACKAGE VIEW

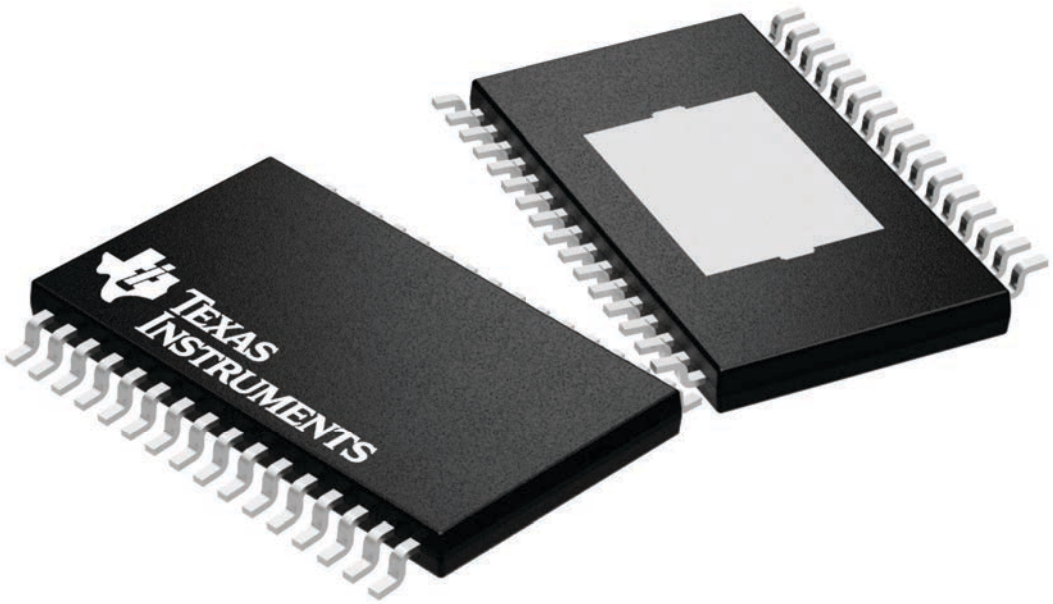
DAP 32

PowerPAD™ TSSOP - 1.2 mm max height

8.1 x 11, 0.65 mm pitch

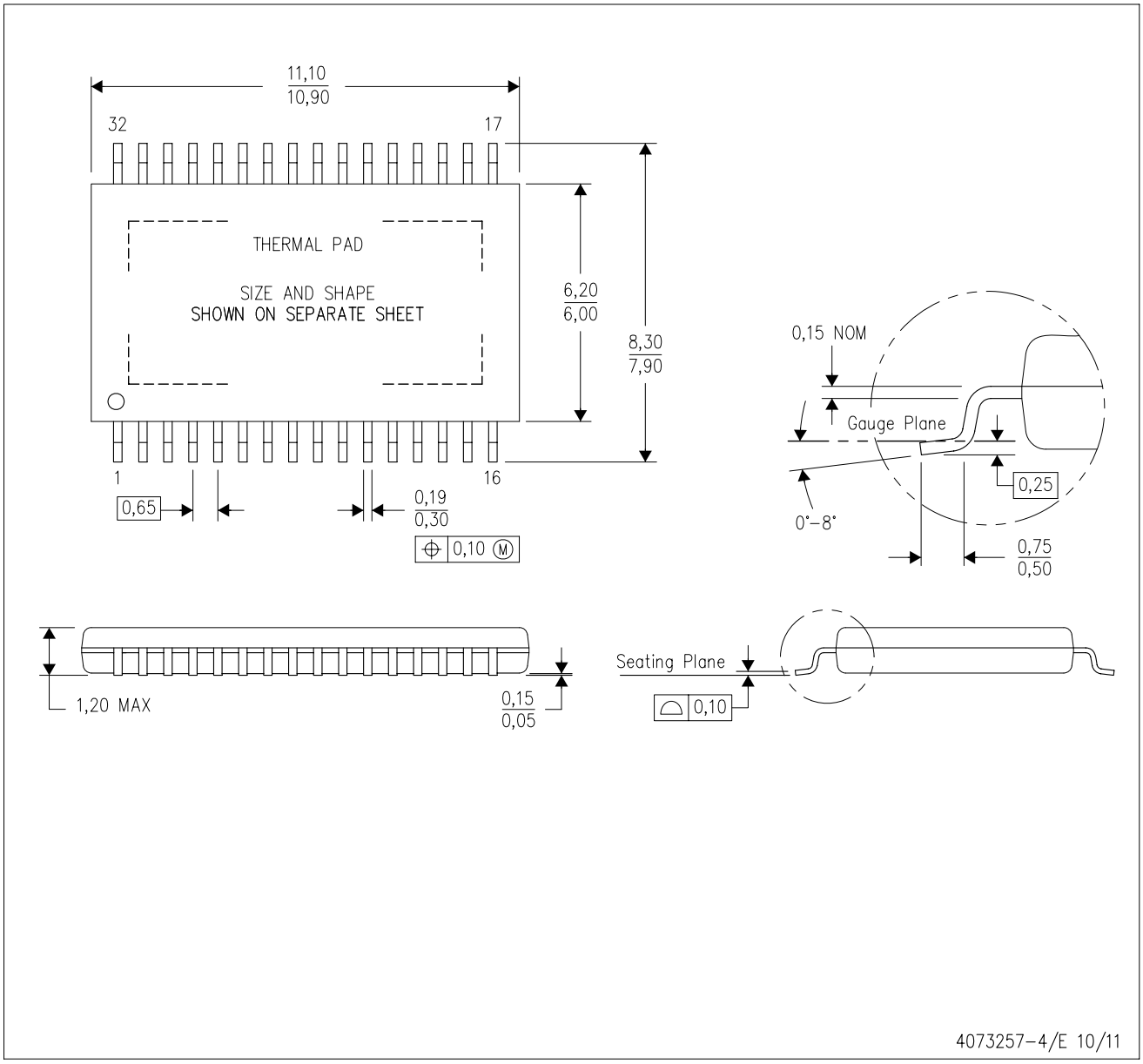
PLASTIC SMALL OUTLINE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225303/A

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
F. Falls within JEDEC MO–153 Variation DCT.

PowerPAD is a trademark of Texas Instruments.

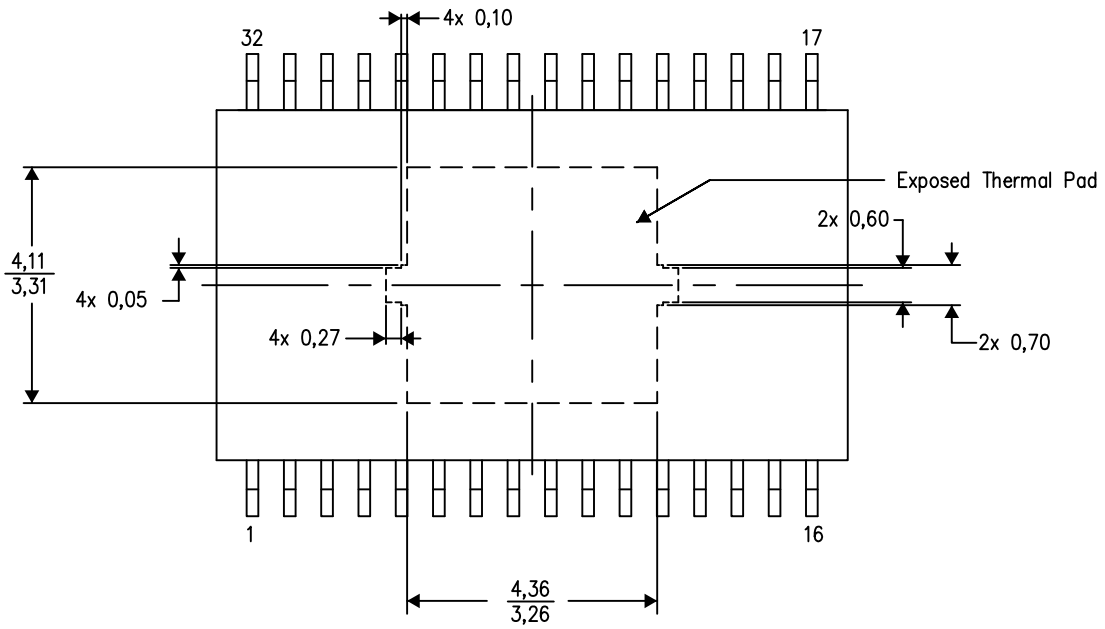
DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

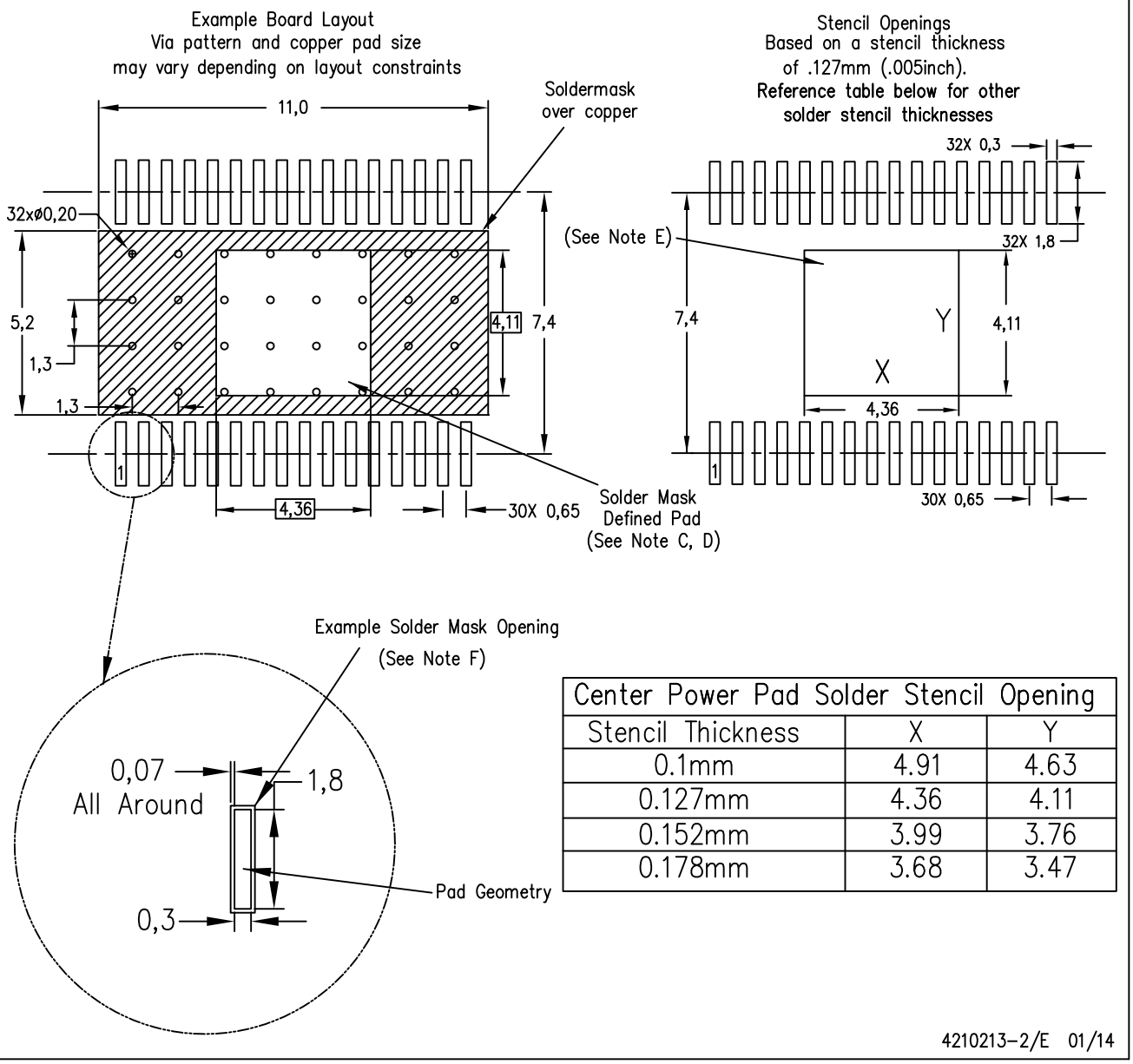
Exposed Thermal Pad Dimensions

4206319–3/M 09/13

NOTE: All linear dimensions are in millimeters

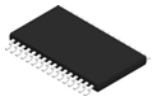
PowerPAD is a trademark of Texas Instruments.

DAP (R–PDSO–G32) PowerPAD™ PLASTIC SMALL OUTLINE PACKAGE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	4.91	4.63
0.127mm	4.36	4.11
0.152mm	3.99	3.76
0.178mm	3.68	3.47

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
F. Contact the board fabrication site for recommended soldermask tolerances.

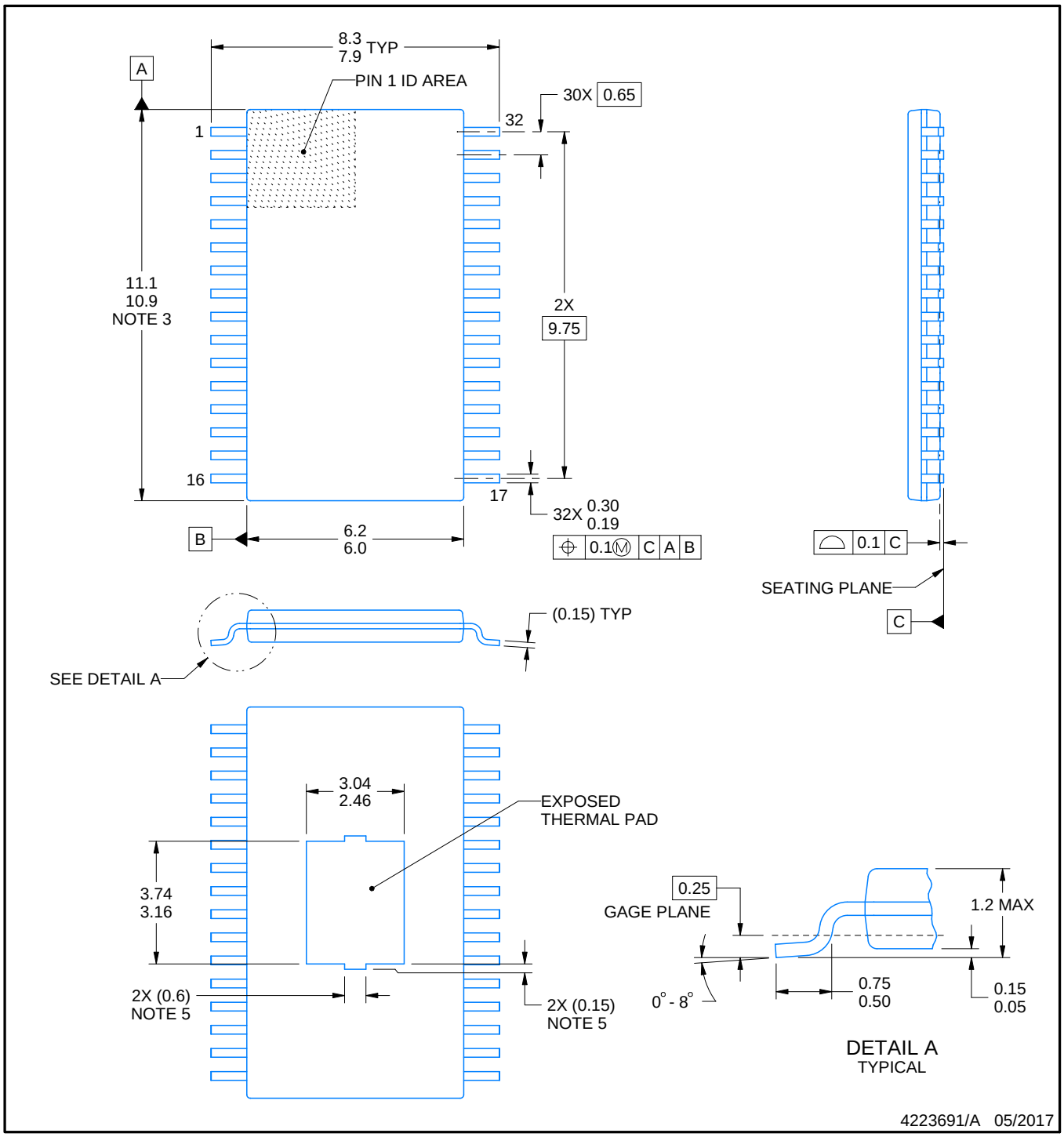


PACKAGE OUTLINE

DAP0032C

PowerPAD™ TSSOP - 1.2 mm max height

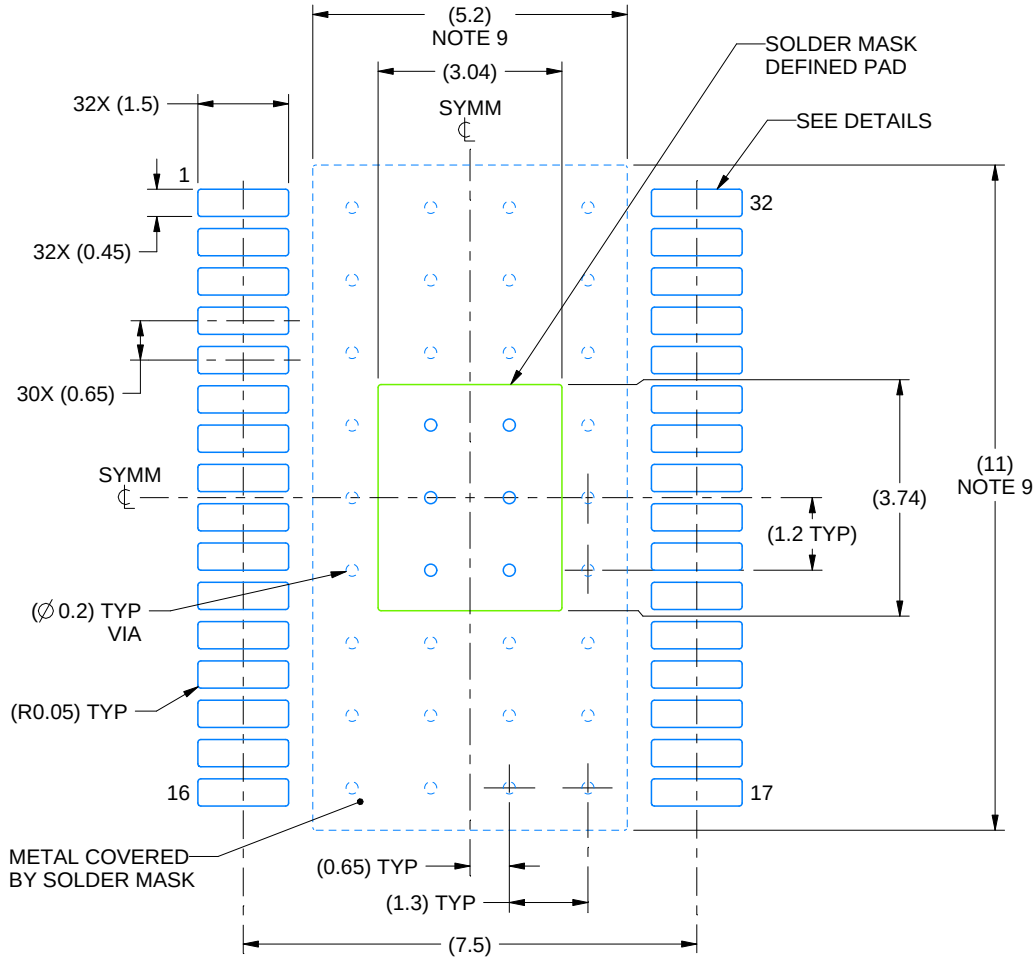
PLASTIC SMALL OUTLINE



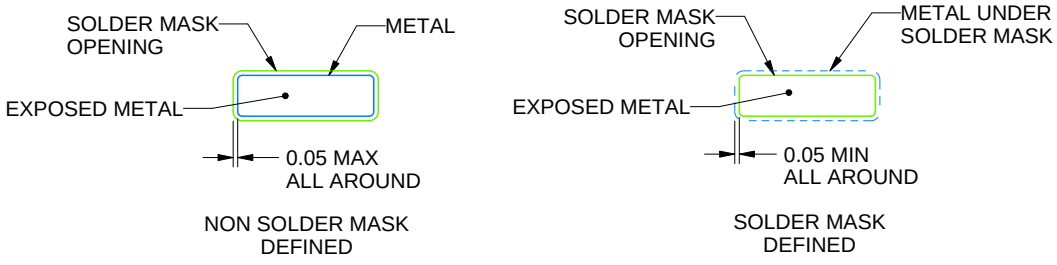
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ and may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

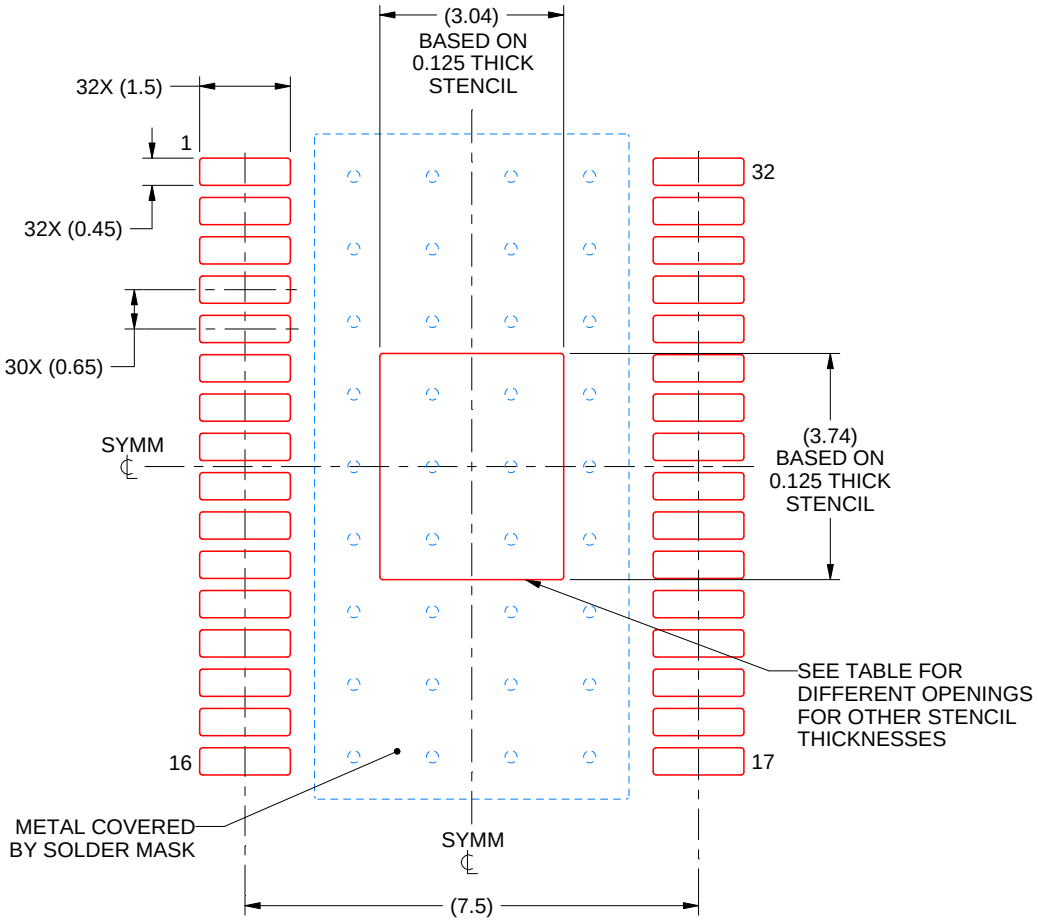


SOLDER MASK DETAILS
NOT TO SCALE

4223691/A 05/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.40 X 4.18
0.125	3.04 X 3.74 (SHOWN)
0.15	2.78 X 3.41
0.175	2.57 X 3.16

4223691/A 05/2017

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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