HIGHLY EFFICIENT PHASE SHIFT FULL BRIDGE CCFL CONTROLLER

Check for Samples: TPS68000

FEATURES

- **8-V to 30-V Input Voltage Range**
- **Full Bridge Topology With Integrated Gate Drives for 4 NMOS Switches**
- **Synchronizable Constant Frequency Operation**
- **Programmable Phase Delays of Operating Frequency for Master-Slave Operation**
- **Lamp Voltage and Lamp Current Regulation**
- **Analog and Burst Dimming**
- **Configurable Distributed Burst Dimming in Multiple Controller Applications**
- **Programmable Voltage Regulation Timeout for Startup and Fault Conditions**
- **Open-Lamp and Short-Circuit Protection**
- **Internal Over-Temperature Protection**
- **Undervoltage Lockout**
- **30-pin TSSOP Package**

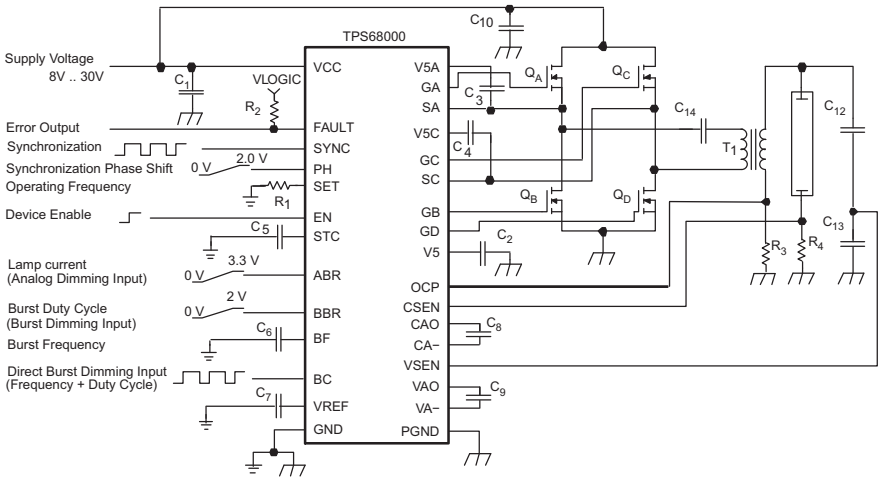
APPLICATIONS

- **CCFL Backlight Power Supplies for Desktop Monitors and LCD TVs**
- **CCFL Backlight Power Supplies for Notebook Computers**

DESCRIPTION

The TPS68000 device provides a power supply controller solution for CCFL backlight applications in a large variety of applications. The wide input voltage range of 8 V to 30 V makes it suitable to be powered directly from regulated 12-V or 24-V rails, or any other source with output voltages in this range. When using a 10% accurate regulated 5-V rail, it also can be used in notebook computers or other portable battery-powered equipment having lower minimum supply voltages. The controller is capable of driving the gates of all 4 NMOS switches directly without the need for any additional circuitry, like dedicated gate drivers or gate-drive transformers. The wide input voltage range also makes it easy to design CCFL converters with higher input voltages like 120 V or 400 V available at the output of a power factor correction unit. The TPS68000 also supports CCFL converter circuits driving multi-lamp applications, either by using higher power-rated switches and transformers, or using several TPS68000s synchronized. When synchronized, they can be operated either at the same frequency and phase, or phase shifted to minimize RMS input current. Already implemented smart dimming features, such as support of distributed dimming, also help to optimize the performance of multi-controller applications.

(Continued on next page)



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DESCRIPTION (CONTINUED)

To start the lamp, an automatic strike control is implemented. It smoothly increases the lamp voltage by sweeping the operating frequency across the self resonance frequency of the transformer-series capacitor resonant circuit. During this time the maximum lamp voltage is limited and regulated by a voltage control loop until the lamp current increases to a value allowing the current control loop to take over control. The lamp current is regulated over a wide current range. To set the lamp brightness, analog and PWM dimming circuits are implemented. Analog and PWM dimming can be used independent of each other to control lamp brightness over a wide range.

To protect the circuit during fault conditions, for example broken, disconnected, or shorted lamps, overvoltage protection and overcurrent protection circuits are implemented. To protect the TPS68000 from overheating, an internal temperature sensor is implemented that triggers controller turn-off at an excessive device temperature.

The device is packaged in a 30-pin TSSOP package measuring 6,4 mm x 7,8 mm (DBT).

AVAILABLE DEVICE OPTIONS

T_A	PACKAGE	PART NUMBER(1)
–40°C to 85°C	30-Pin TSSOP	TPS68000DBT

(1) The DBT package is available taped and reeled. Add R suffix to device type (e.g., TPS68000DBTR) to order quantities of 2000 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	TPS68000
Input voltage range on VCC, EN, FAULT	–0.3 V to 33 V
Input voltage range on SYNC, SET, PH, STC, ABR, BBR, BF, BC, VREF, VA-, VAO, CA-, CAO	–0.3 V to 6 V
Input voltage range on VSEN, CSEN, OCP	–6 V to 6 V
Input voltage range on GD, GB, V5	–0.3 V to 6 V
maximum differential voltage between GA, V5A and SA	6 V
maximum differential voltage between GC, V5C and SC	6 V
maximum differential voltage between SA and PGND	35 V
maximum differential voltage between SC and PGND	35 V
Operating virtual junction temperature range, T_J	–40°C to 150°C
Storage temperature range T_{stg}	–65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated uner "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATINGS

PACKAGE	THERMAL RESISTANCE θ_{JA}	POWER RATING $T_A \le 25°C$	DERATING FACTOR ABOVE $T_A = 25°C$	POWER RATING $T_A \le 70°C$	POWER RATING $T_A \le 85°C$
DBT	63.9°C/W	1565 mW	16 mW/°C	860 mW	626 mW

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_I	Supply voltage at VCC	8.0		30	V
T_A	Operating free air temperature range	–40		85	°C
T_J	Operating virtual junction temperature range	–40		125	°C

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ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MAIN CONTROL						
V_5	Internal control supply regulator	I_{OUT-V5}< 25 mA	4.5	5	5.5	V
I_{OUT-V5}	Control supply output current	including internal current consumption			25	mA
V_{UVLO}	Under voltage lockout threshold at V5	Voltage at V5 decreasing	4.0	4.1	4.3	V
V_{OL}	FAULT output low voltage	I_{FAULT} = 500 µA		0.2	0.4	V
V_{lkg}	FAULT output leakage current	V_{FAULT}= 5 V		0.1	1	µA
V_{IL}	EN input low voltage				0.4	V
V_{IH}	EN input high voltage		1.4			V
	EN input current	V_{CC} = 24 V		0.05	0.1	µA
I_{STC}	STC source current	during strike		6		µA
I_{STC}	STC source current	during wait		2		µA
I_{STC}	STC source and sink current	normal operation, V_{STC} = 1.25 V		10		µA
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C
	Quiescent current into VCC	VCC = 12 V, V5 = 5.5 V		30	50	µA
	Quiescent current into VCC	VCC = V5 = 5.5 V		25	40	µA
	Quiescent current into V5	VCC = V5 = 5.5 V		1000	1500	µA
	Shutdown current into VCC	VCC = V5 = 5.5 V, EN = 0V		1	2	µA
	Shutdown current into V5	VCC = V5 = 5.5 V, EN = 0V		1	2	µA
	Shutdown current into VCC	VCC = 12 V, EN = 0V		2.5	5	µA
V_{REF}	Reference Voltage	$I_{OUT-VREF}$ < 5 mA	3.27	3.3	3.33	V
$I_{OUT-VREF}$	Reference output current		5			mA
GATE DRIVE						
	High side drive sink resistance	I_D = 0.05 A		1.2	2.0	Ω
	High side drive source resistance	I_D = 0.05 A		1.5	2.5	Ω
	High side drive rise time	C_G = 4.7 nF, S_A = S_C = 0 V, V_{5A} = V_{5C} = 5 V		35	50	ns
	High side drive fall time	C_G = 4.7 nF		15	25	ns
	Time delay between high side off and low side on	C_G = 4.7 nF		100		ns
	Time delay between low side off and high side on	C_G = 4.7 nF		100		ns
	Low side drive sink resistance	I_D = 0.05 A		1.2	2.0	Ω
	Low side drive source resistance	I_D = 0.05 A		1.5	2.5	Ω
	Low side drive rise time	C_G = 4.7 nF, V_5 = 5 V		35	50	ns
	Low side drive fall time	C_G = 4.7 nF		15	25	ns
MAIN OSCILLATOR						
f	Oscillator frequency programming range		30		100	kHz
f_{SYNC}	Frequency capture range for synchronization		0.5 x f		2 x f	
V_{IL}	SYNC low voltage				0.4	V
V_{IH}	SYNC high voltage		1.4			V
I_{SYNC}	SYNC input current	V_{PH} ≤ V_5 - 1.3 V, V_{SYNC} = 3.3 V		0.5	1.5	µA
I_{SYNC}	SYNC drive current	V_{SYNC} ≥ 1.4 V, V_{PH} = 5 V	1000	1250	1500	µA

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ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SYNC}	SYNC sink current	$V_{SYNC} \le 0.4$ V, $V_{PH} = 5$ V	1000	1250	1500	µA
	Minimum pulse width for synchronization			100		ns
V_{SET}	SET output voltage			1.25		V
	Phase shift of the main oscillator clock	V_{PH} = 0.1 V .. 1.9 V		90		° / V_{PH}
I_{PH}	PH input current	$V_{PH} = 2.0$ V		0.1	1	µA
V_{PH}	Threshold for programming device as main oscillator frequency master		V_5 – 1.3 V		V_5 – 0.7 V	V
VOLTAGE AND CURRENT CONTROL						
R_{CSEN}	Current sense input impedance	$V_{CSEN} = 3.3$ V		35		kΩ
R_{CSEN}	Current sense input impedance	$V_{CSEN} = –3.3$ V		25		kΩ
R_{VSEN}	Voltage sense input impedance	$V_{VSEN} = 3.3$ V		25		kΩ
R_{VSEN}	Voltage sense input impedance	$V_{VSEN} = –3.3$ V		30		kΩ
I_{CAO}, I_{VAO}	Voltage and current amplifier output source current	V_{CAO}, $V_{VAO} = 2.5$ V		55		µA
I_{CAO}, I_{VAO}	Voltage and current amplifier output sink current	V_{CAO}, $V_{VAO} = 2.5$ V	200			µA
$VREF_{VREG}$	Voltage regulator reference voltage			(0.8 ×V_{REF}) / π		V
$VREF_{OVP}$	Overvoltage comparator threshold			V_{REF}		V
$VREF_{CREG}$	Current regulator reference voltage			V_{ABR} / π		V
I_{OCP}	Overcurrent comparator input current	$V_{OCP} = 3.3$V		0.1	1	µA
I_{OCP}	Overcurrent comparator input current	$V_{OCP} = –3.3$V		50		µA
$VREF_{OCP}$	Overcurrent comparator threshold			V_{REF}		V
DIMMING						
I_{ABR}	ABR input current	$V_{ABR} = 3.3$ V		0.01	0.1	µA
V_{ABR}	ABR input voltage range for lamp current programming	BC = V_5	0		3.3	V
I_{BBR}	BBR input current	$V_{BBR} = 2.0$ V		0.1	1	µA
	Burst duty cycle	V_{BBR} = 0 V .. 2 V		50		% / V_{BBR}
V_{BBR}	BBR input voltage threshold for selecting synchronized burst dimming		V_5 – 1.3 V		V_5 – 0.7 V	V
I_{BF}	BF source current			10		µA
f_{Burst}	Internal burst frequency range		20		1000	Hz
f_{BC}	Frequency lock / capture range for synchronized burst dimming		0.5 x f_{Burst}		1.5 x f_{Burst}	
t_r	Burst current pulse rise time			400		µs
I_{BC}	BC input current	$V_{BC} = 3.3$V		0.1	1	µA
V_{IL}	BC input low voltage				0.4	V
V_{IH}	BC input high voltage		1.4			V
	minimum pulse width at BC			100		ns
	Phase shift of the dimming burst compared to BC clock	V_{PH} = 0 V .. 2 V, distributed dimming selected		180		° / V_{PH}

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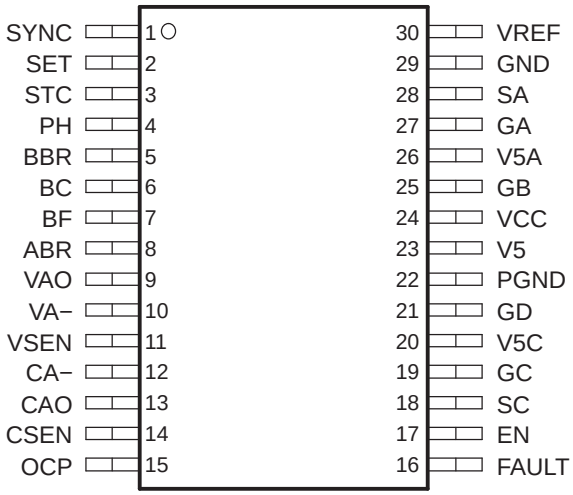
PIN ASSIGNMENTS

DBT PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ABR	8	I	Analog brightness programming input. A DC voltage applied at that pin programs the lamp current the current regulator regulates. 0 V means no current and 3.3 V means maximum current.
BBR	5	I	Burst brightness programming input. A DC voltage applied at that pin programs the duty cycle of the burst pulses generated to dimm the brightness. 0 V means zero duty cycle and 2 V means maximum duty cycle. Applying V5 (5 V) programs the device to operate in synchronized burst dimming mode.
BC	6	I	Burst control. A PWM signal applied at that pin is directly used for burst dimming. Frequency and duty cycle are used directly. This input has priority against the burst frequency programming with BBR and BF
BF	7	I	Burst frequency programming. A capacitor at that pin programs the burst frequency.
CA-	12	I	Current amplifier negative input. This input is used to connect the compensation capacitor for compensating the current loop.
CAO	13	O	Current amplifier output. This is the output for the current amplifier. It is used to connect the compensation capacitor for the current loop.
CSEN	14	I	Current sense. Measuring input for the lamp current. The applied voltage (coming from a shunt resistor) will be used for lamp current regulation. Sensed AC voltages can be applied directly. They will be rectified internally.
EN	17	I	Enable input. Logic high enables the device.
FAULT	16	O	Error output, any detected malfunctioning of the application will be reported as error on this pin. Error means the output is pulled low. The output is open drain to allow connecting multiple error outputs of similar devices together.
GA	27	O	Gate drive output of switch A
GB	25	O	Gate drive output of switch B
GC	19	O	Gate drive output of switch C
GD	21	O	Gate drive output of switch D
GND	29		Analog ground pin. Reference ground for all control signals.
OCP	15	I	Over current protection. This input is used to monitor a voltage derived from a current sensor in any part of the converter. This voltage is compared to an internal reference voltage. Exceeding the internal reference voltage causes the device logic to turn the device off and report an error signal at the fault pin.
PGND	22		Reference ground for the gate drivers and the gate drive supply.

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Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
PH	4	I	Phase delay programming input. A voltage between 0 V and 2 V applied to that pin programs the phase delay of the operating frequency compared to the synchronizing frequency. Applying V5 (5.0 V) programs the device as a master regarding the main oscillator frequency (see SYNC). The voltage applied to that pin is also used to determine the phase delay in a distributed dimming configuration
SA	28		Source connection of switch A
SC	18		Source connection of switch C
SET	2	I	Operating frequency programming input. A resistor connected to this pin programs the internal operating frequency.
STC	3	I	Startup capacitor. A capacitor connected to that pin determines the the time the device waits in voltage regulation for the lamp to strike.
SYNC	1	I/O	Synchronization input or operating frequency output. If the device is configured as master (see PH) the pin is used to provide the synchronization frequency for the slaves. Otherwise the device works as slave and uses the applied frequency at that pin for synchronizing the operating frequency.
V5	23	I/O	Input/Output of the internal 5 V regulator for gate drive supply and control supply. A capacitor must be connected to that pin to decouple switching noise caused by the gate drivers.
V5A	26	O	Supply input for the gate driver of the high-side switch A. A capacitor must be connected to that pin to supply the gate driver during switching (bootstrap).
V5C	20	O	Supply input for the gate driver of the high side switch C. A capacitor must be connected to that pin to supply the gate driver during switching (bootstrap).
VA-	10	I	Voltage amplifier negative input. This input is used to connect the compensation capacitor for compensating the voltage loop.
VAO	9	O	Voltage amplifier output. This is the output for the voltage amplifier. It is used to connect the compensation capacitor for the voltage loop.
VCC	24	I	Device supply voltage input. VCC must be connected to V5 in case the device is powered directly from a regulated 5 V rail.
VREF	30	O	Voltage reference. Output of the internal 3.3 V reference for use with all the analog control inputs.
VSEN	11	I	Voltage sense. Measuring input for the lamp voltage. This voltage is used for lamp voltage regulation (open lamp regulation) and overvoltage protection. Sensed AC voltages can be applied directly. They are rectified internally.

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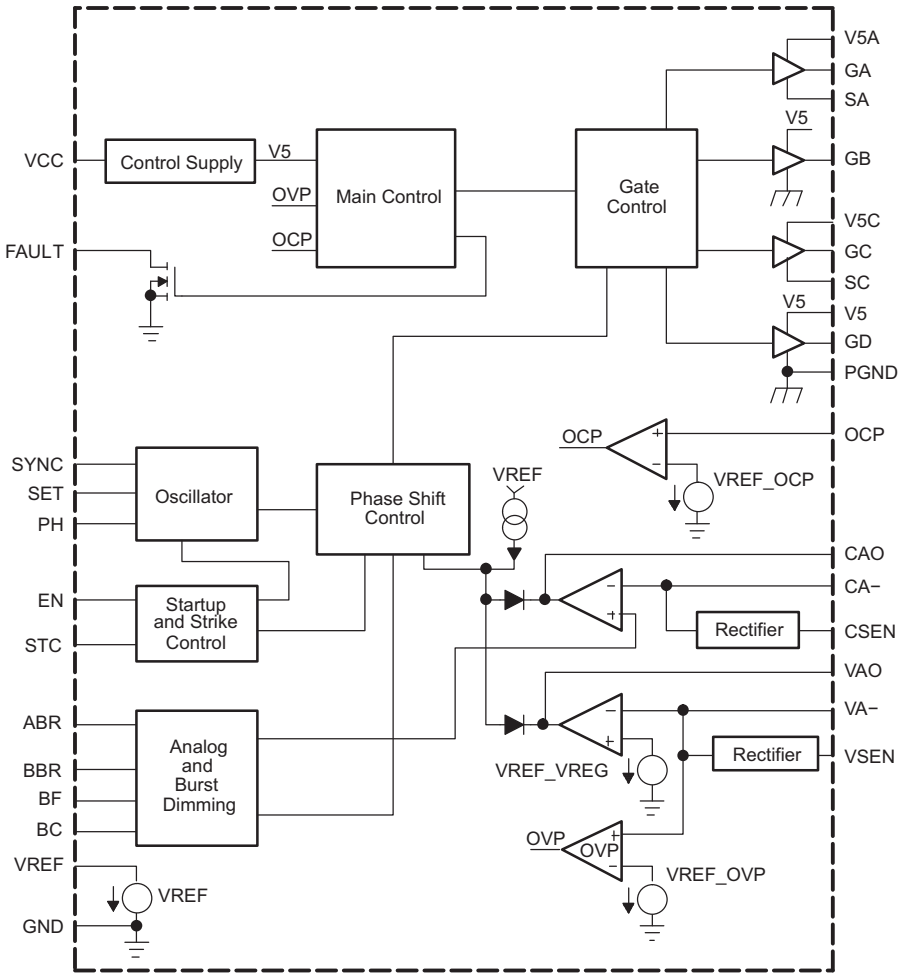
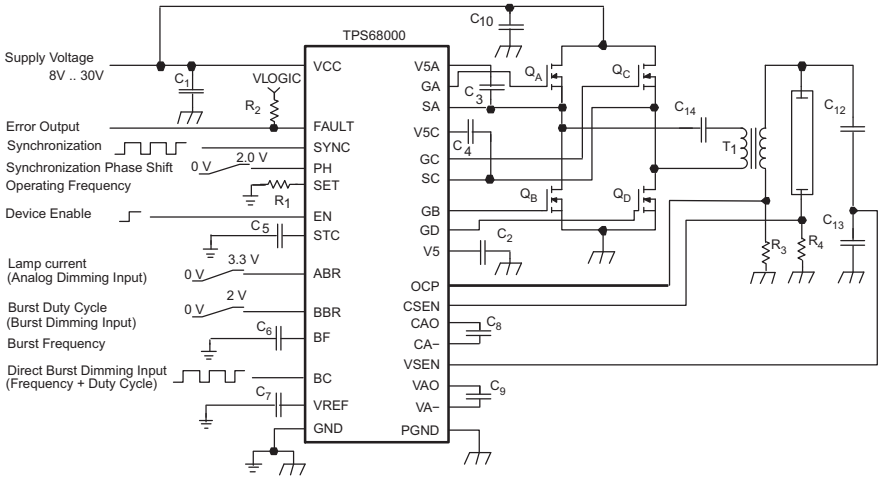
FUNCTIONAL BLOCK DIAGRAM (TPS68000)



PARAMETER MEASUREMENT INFORMATION



TYPICAL CHARACTERISTICS

Table 1. Table of Graphs

		FIGURE
Output voltage at V_5	vs output current at V_5	1
Output voltage at V_{REF}	vs output current at V_{REF}	2
Operating frequency	vs resistance at SET	3
Phase shift of operating frequency	vs voltage at PH	4
Burst dimming duty cycle	vs voltage at BBR	5
Burst dimming phase shift	vs voltage at PH	6
Waveforms	Startup of V5 (V_{CC} = 12 V)	7
	Startup of V5 (V_{CC} = 24 V)	8
	Startup of V_{REF} (V_{CC} = V5 = 5V)	9
	Lamp current and lamp voltage at startup (V_{CC} = 12 V)	10
	Lamp current and lamp voltage at startup (V_{CC} = 24 V)	11
	Lamp current softstart at burst dimming	12

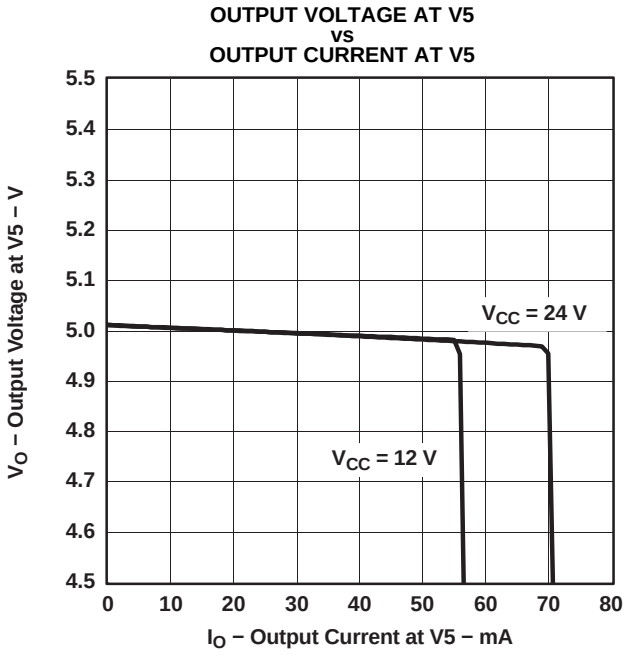


Figure 1.

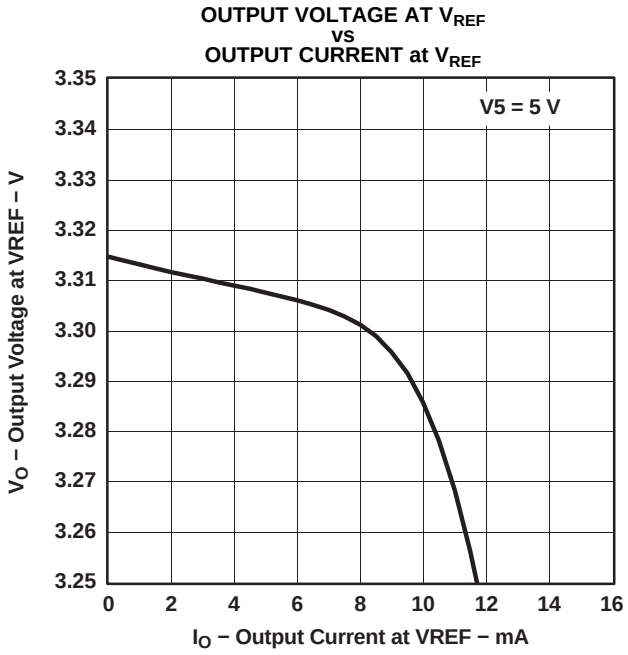


Figure 2.

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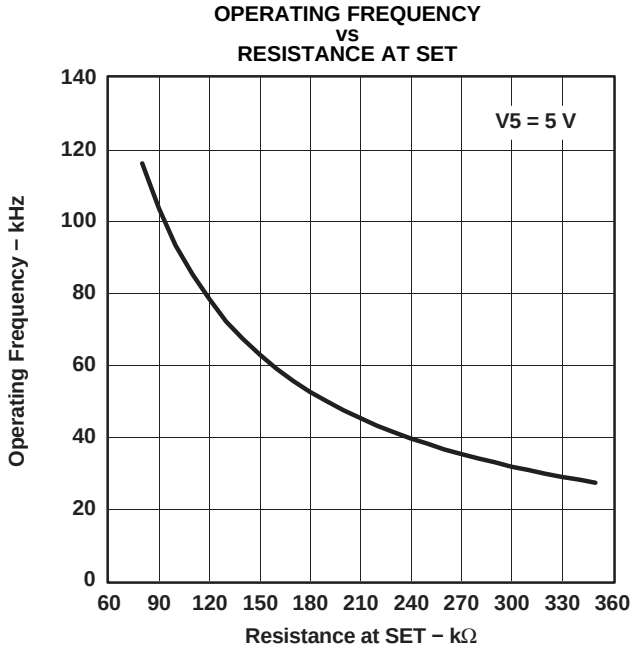

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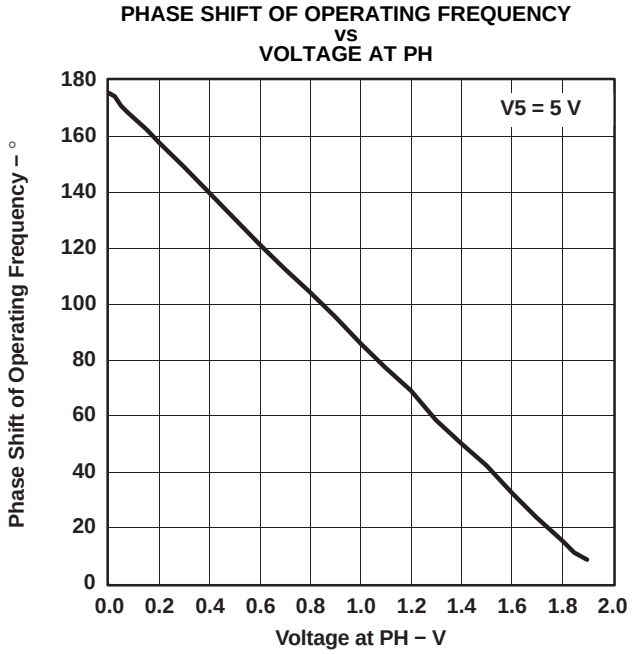

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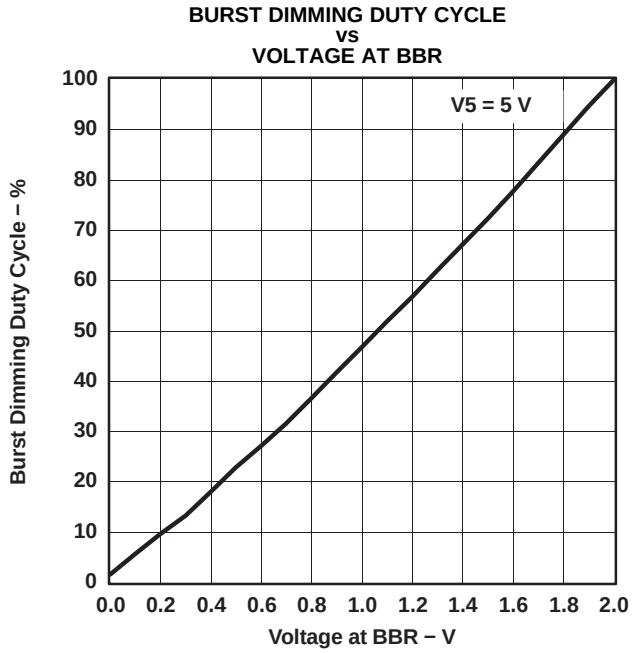

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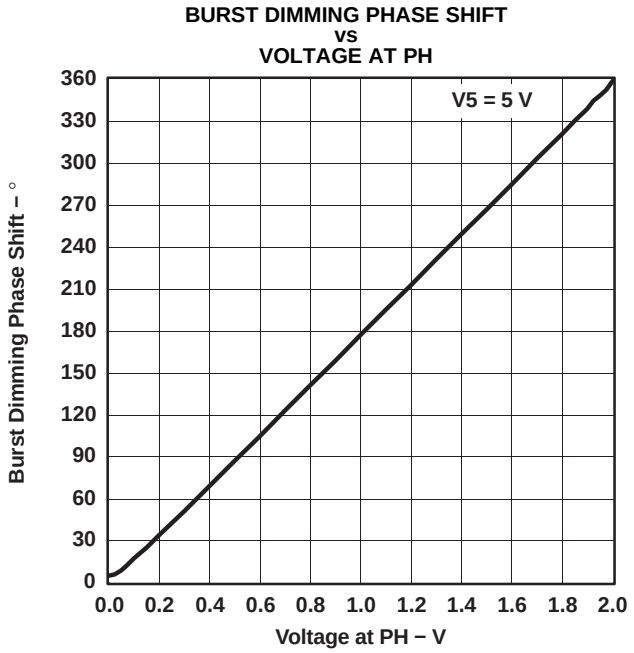

Figure 6.

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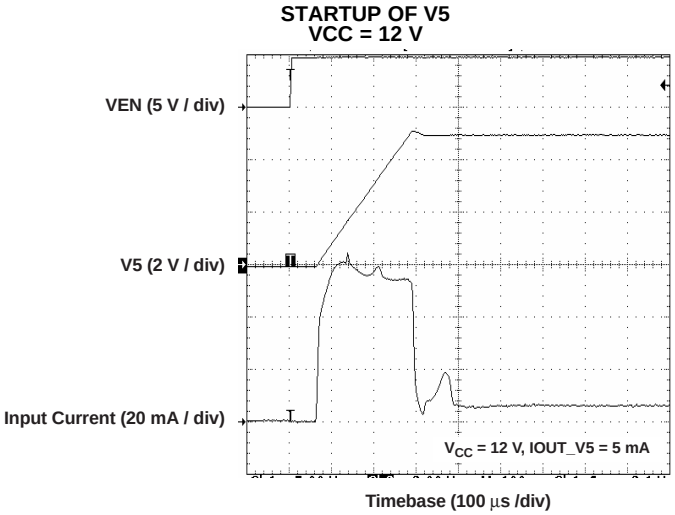

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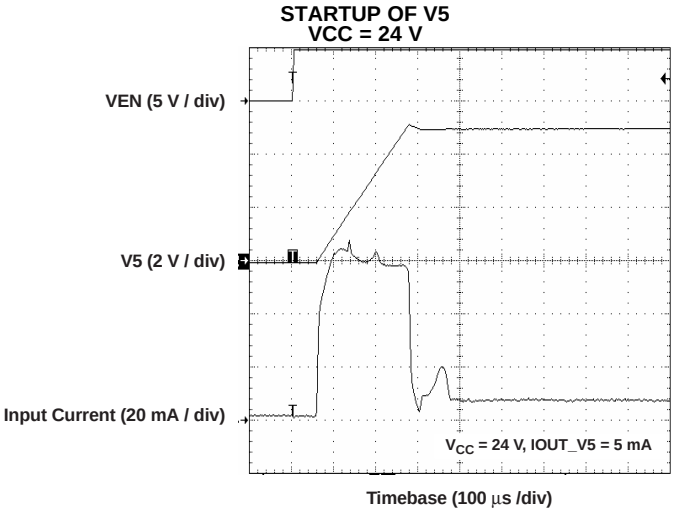

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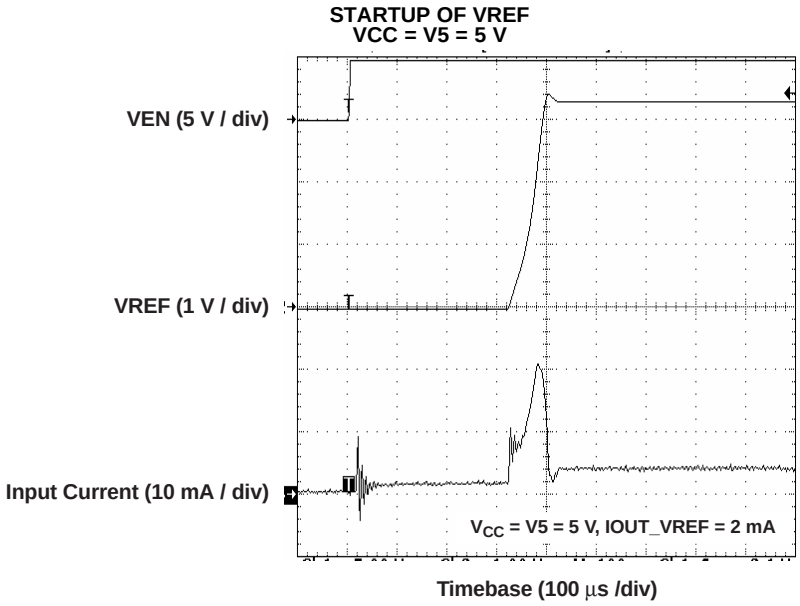

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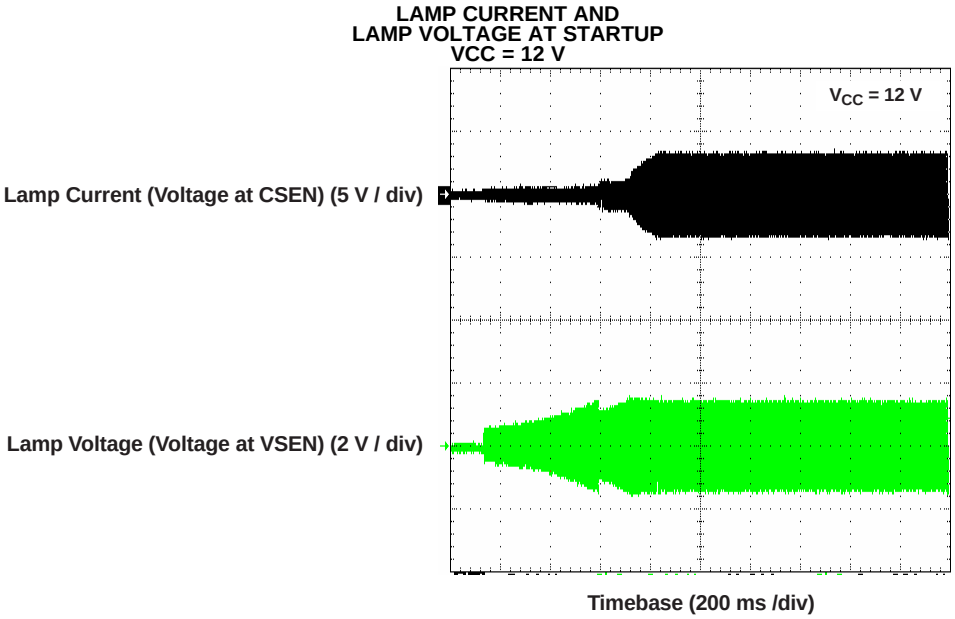

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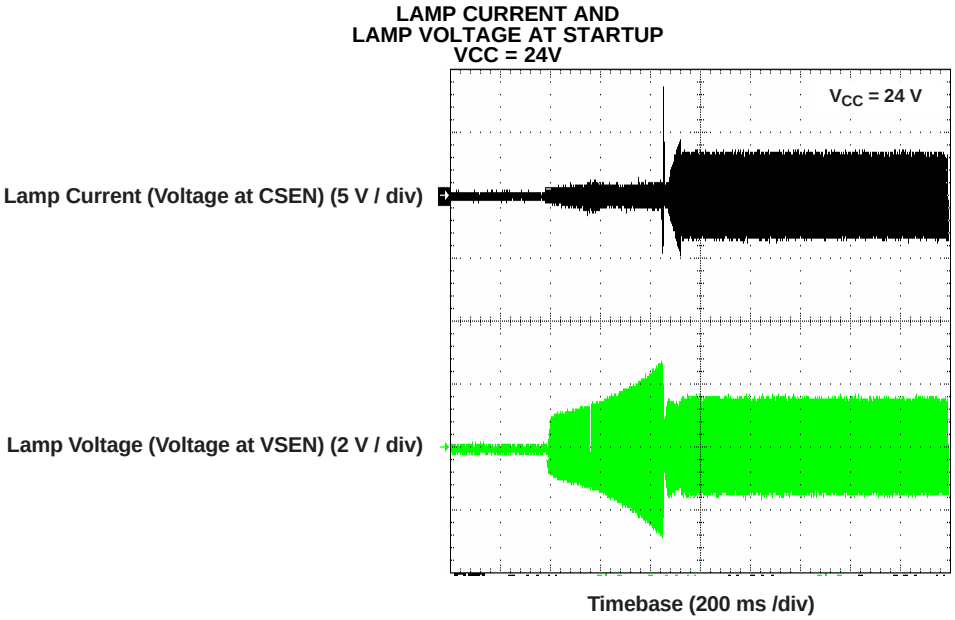

Figure 11.

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LAMP CURRENT SOFTSTART AT BURST DIMMING

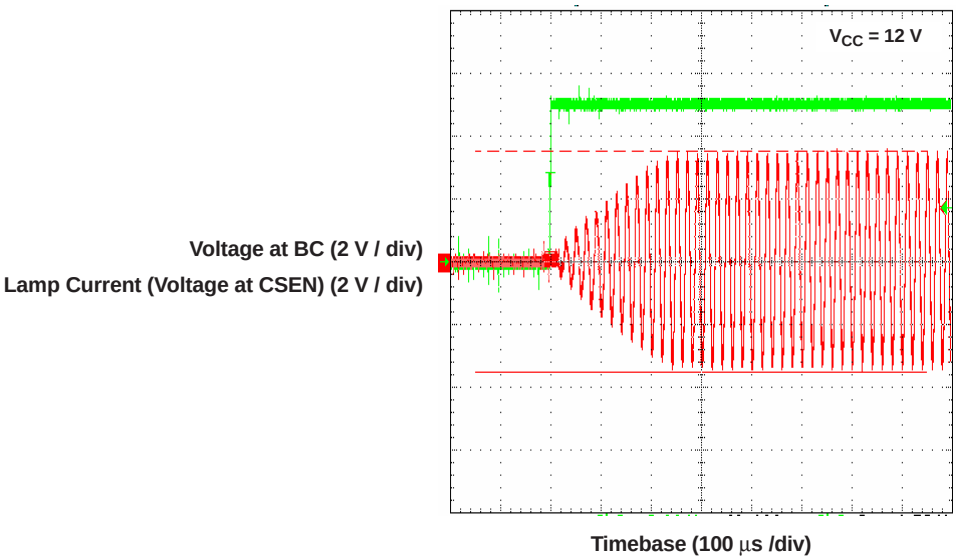

Figure 12.

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DETAILED DESCRIPTION

Supply Voltages

The TPS68000 and the connected H-bridge power stage can be completely supplied by a voltage connected to VCC. This voltage must be between 8 V to 30 V. In this configuration an internal linear regulator generates the 5 V required for control supply and gate drive supply. It is available at the V5 pin. The external capacitors for supplying the high side gate drivers during operation are charged using internal diodes during the time when the low side switches are turned on. The 3.3-V reference voltage is generated with a precise linear regulator, which is also supplied from the 5-V control supply.

Optionally, the device can be supplied using a regulated 5-V rail. This is done by connecting the external 5 V to VCC and V5. This way the internal regulator is bypassed and the internal power dissipation is reduced. It also makes it possible to use any voltage lower than 30 V to supply the H-bridge power stage. When using appropriate means of isolating the gate drive outputs of the device from their respective gates of the H-bridge switches, the device can control power stages with higher input voltages as well. An example for this configuration is using the output voltage of the PFC directly as a supply for the H-bridge power stage.

Gate Driver

The TPS68000 is a controller for converters, built with a full bridge topology. To control the output power high-side and low-side switches in each of the two half bridges are driven alternately with 50% duty cycle. By phase shifting both half-bridge parts to each other, output power is controlled. Current can only flow into the transformer if one of the high side switches is turned on the same time as the low-side switch on the other half-bridge is turned on. Maximum output power can be achieved if the turn on time of the high-side switch on one half-bridge exactly overlaps with the turn on time of the low side on the other half bridge. Zero output power will be if there is no overlap.

To properly control the 4 switches required for this phase shift full bridge topology, 4 gate drivers are implemented. To obtain maximum efficiency at lowest costs the gate drivers are designed to drive 4 N-Channel MOSFETs. The gate drive outputs can be connected directly to the gates of the FETs. There is no gate drive circuit required as long as the operating input voltage range does not exceed the isolation voltage of the high side drivers or the drive capability is not sufficient for larger FETs. The nominal gate drive voltage is 5 V. This 5-V rail is generated internally in the device and is used directly to supply the low side drivers. For the high side drivers external capacitors are used to supply the drivers. They are charged up during the on time of the low-side drivers.

Control Circuit

The device is able to control lamp current and lamp voltage directly. Lamp voltage and lamp current are sensed with an appropriate feedback divider and a shunt resistor. By suitable designing feedback divider and shunt resistor lamp current and maximum lamp voltage are programmed. Since the lamp needs to be operated with AC current, the feedback signals in simple applications usually are AC voltages. To directly support this and to save external components for rectification, internal half wave rectifiers are built in the device.

Regulating current and voltage is done by two independent error amplifiers. Both are compensated externally to be flexible to meet the demands for a wide variety of CCFL backlight applications. Both error amplifier outputs feed the phase shift modulator. Whichever error amplifier requires the lower duty cycle, takes over control of the system. The control circuit also detects whether the device operates in voltage regulation or in current regulation. If voltage regulation is detected a fault condition is assumed, for example a broken lamp. In this condition the control circuit waits for a programmed wait time. If the current regulator does not take over control again during this wait time, the device shuts down and sets the FAULT flag. The wait time is programmed with the size of the capacitance at STC.

Protection

In addition to the voltage regulator other means of protection are implemented. To ensure that the secondary voltage of the transformer does not exceed the isolation breakdown voltage of the transformer an overvoltage comparator is implemented. This comparator monitors the rectified voltage at the VSEN input. If the peak voltage level at VSEN rises 20% above the nominal regulation voltage, regulated by the voltage amplifier, the overvoltage comparator trips and the device immediately enters FAULT condition. For detailed threshold values please check the electrical characteristics table.

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For additional protection there is a standalone comparator implemented. It can be used to monitor any voltage in the system. The switching threshold is set to the V_{REF} voltage.

. This comparator monitors a voltage at its input and compares it with the internal reference voltage. As soon as the input voltage of the comparator exceeds the reference voltage the comparator asserts FAULT at its output. Negative voltages can be applied at that pin but there is no rectification. Since the input of the overcurrent comparator is directly accessible at a pin it can be connected to any part of the circuit. It must not necessarily use the shunt resistor used for current regulation. Monitoring the current in the secondary winding or any other DC voltage in the system may be a desired approach as well.

Finally the device has an internal temperature sensor to monitor the IC temperature. If the temperature gets too high FAULT is asserted as well. For detailed values for threshold and hysteresis of the thermal protection please check the electrical characteristics table.

Oscillator

The device is operating at a fixed frequency which is generated by a built in PLL circuit. The frequency is programmed with a resistor at SET. It also can be synchronized to an external frequency at SYNC. When synchronizing to an external clock two modes are possible. One is to synchronize directly to the external clock, the other is to synchronizeto the external clock but phase shifted. This helps to minimize the RMS input current of the complete power converter application in a multi controller topology. This phase shift is programmed with a DC voltage of 0 V to 2 V at PH for a phase shift of 0° to 180°.

Dimming

To dimm the lamp, two basic methods of dimming are supported. The first is to control the lamp current directly, called analog dimming. The second is to turn the lamp on and off at a low frequency with a certain duty cycle, called burst dimming. Analog dimming, is done by just providing a DC voltage at ABR. The lamp current will be regulated propotional to that voltage. The maximum lamp current in burst dimming is also programmed with this voltage at ABR.

Turning the lamp on and off, burst dimming, needs some more information. A low frequency must be generated and duty cycle information for the on time needs to be provided. The simplest burst dimming mode, independent burst dimming, is to program the low frequency with an external capacitor at BF. Applying a DC voltage at BBR sets the duty cycle of the burst pulse. The burst duty cycle will be programmed proportional to the DC voltage at BBR.

If the burst dimming frequency and duty cycle must be synchronized to an external PWM signal this external signal can be connected to BC. The bursts follow the PWM signal directly. A PWM signal detected at BC has priority to any internally generated burst signal. To force the device to take the BC PWM signal BBR can be tied high (V5).

To minimize RMS input current in a multiple controller application the burst signal can be phase shifted to the external PWM connected to BC, which is called Distributed Dimming®. Frequency and duty cycle stay the same. The phase shift information is derived from the voltage at PH. Voltages of 0 V to 2 V at PH generate burst phase shifts of 0° to 360°. For this mode of operation the internal low frequency oscillator is used. It is operated as a PLL synchronized to the PWM frequency at BC and its center frequency has to be programmed at BF. The compensation of the low frequency PLL is done with and R - C network connected at BBR.

Startup

When the device is enabled or the device is powered up with EN tied high, the device enters lamp strike mode. In this mode no dimming and synchronization is possible. During the strike procedure the lamp current which should flow when the lamp has turned on is programmed at ABR.

The device starts operating at double the programmed operating frequency and sweeps down to half of the nominal frequency. During this sweep it can cross the self resonance frequency of the system with its maximum voltage gain. As soon as the lamp current has reached its programmed value the device stops sweeping and switches to the nominal operating frequency. The device will continue to regulate the lamp current and all other control features like synchronization and burst dimming are enabled and will be used. If during this sweep the

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lamp voltage, which is programmed at the voltage regulator is reached, frequency sweeping is stopped and the voltage regulator regulates the voltage at the programmed level. At that time a timer is started. If during this waiting, the lamp current reaches its programmed value, the device will continue operating as described above. If for any reason the timer reaches its programmed end, programmed by a capacitor at STC, the device stops working and enters FAULT condition.

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APPLICATION INFORMATION

DESIGN PROCEDURE

This section describes the basic configuration and calculations which need to be done for getting the component values necessary for configuring the device properly. Backlight inverters can be significantly more complex especially when driving multiple lamps with one or more controllers. This will be described in seperate application notes and documentation for reference designs and EVM's which are also available.

Decoupling and Filtering

For decoupling and filtering it is recommended to use capacitors with a low series resistance and inductance to achieve optimum performance. Surface mount ceramic capacitors are a good choice. It is also recommended to use short and wide traces to connect those decoupling capacitors to the controller.

For the high side gate drivers in typical applications at least a 1-µF supply capacitor is recommended. It should be connected between SA to V5A and SC to V5C with connectio placed as close as possible to the respective pins to make sure that the gate drive outputs have a low impedance power source.

The V5 control supply requires a decoupling capacitor as well. It should be similar in capacitance as used for both of the high side gate drivers. Example if a typical 1uF capacitor is used at the high side drivers therefore 2.2 µF is recommended at V5.

If V5 is used as an input, which means the controller is supplied with regulated 5 V directly, V5 must be connected to VCC to avoid reverse current flowing and malfunctioning of the control circuits directly powered from VCC.

In case the V5 regulator is supplied via the VCC input it is recommended to use a decoupling capacitor at the VCC pin. The capacitor should be at least 0.1 µF. For additional filtering a resistor in series can be used.

For all those capacitors the PGND pin at the IC should be the reference ground.

Connecting the Gates of the MOSFETs

The gates of the MOSFETs of the power stage should be connected with short and wide traces having a low impedance. The respective ground connection should be similar in width and length. Special care should be taken on the loop area formed by the gate drive trace and the respective ground return trace, that it is as small as possible. Any vias in this traces should be avoided.

If there is a need to slow down the switching speed of the FETs to reduce EMI caused by switching transients, gate resistors at the gate drive outputs can be used.

Voltage Reference

The internal reference voltage is available at the VREF pin. It is recommended to decouple it at this pin using a minimum 0.22 µF capacitor to the analog ground reference pin GND. Short direct connections are recommended.

Enabling the Controller

A logic high at the EN pin enables the controller. The enable thresholds are designed to meet requirements of 3.3 V and 1.8 V logic standards. Nevertheless it is also possible to connect EN directly to VCC to enable the controller at power up, since the EN pin can withstand voltages as high as allowed at VCC.

If the device detects a fault it is automatically disabled. To allow the device to automatically restart after a fault, FAULT and EN pins can be directly connected together using a common pull up resistor to VCC.

Fault Output

The fault output is open drain. It is low impedance to GND if the controller detected a fault. In normal operation it is always high impedance. To make sure that a logic low at the FAULT pin has a lower voltage than 0.4 V the pullup resistor should limit the current into the FAULT pin to a value lower than 0.5 mA. Equation 1 shows the calculation:

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$$R_{FAULT} = \frac{V_{LOGIC}}{0.5\ mA} \quad (1)$$

R_{FAULT} is the minimum resistance value of the pullup resistor, V_{LOGIC} is the maximum supply voltage of the logic connected to FAULT.

Main Oscillator

In normal operation the controller operates at the frequency of the main oscillator. It is programmed with a resistor connecting the SET pin to GND. The resistor value is calculated using Equation 2:

$$R_{SET} = \frac{9720 \times k\Omega \times kHz}{f_N} \quad (2)$$

If the controller should be synchronized to an external clock the main oscillator frequency should be programmed close to the synchronizing frequency. This avoids large variations in case external clock pulses are missing. It also speeds up the locking to the external clock. The SET pin should never be left open.

Synchronization of the Main Oscillator

The main oscillator can be used in different modes of operation. The first and most important mode is using it as a reference clock. This is also the mode of choice in a single controller application which is not synchronized to an external clock. In this mode the SYNC pin is used as an output and should be left open if no circuit needs to be synchronized to the device main oscillator clock. To force the device operating in this mode 5 V (V5) must be connected to the PH pin.

Lower voltages applied at the PH pin configure the SYNC pin as an input. Detailed voltage levels for this can be found in the electrical characteristics table. If the SYNC pin is configured as an input the device automatically synchronizes the main oscillator to the frequency which must be applied at the SYNC pin. The compensation for this main oscilator PLL circuit is done with a capacitor connected at the STC pin. Since this capacitor is used for defining sweep and wait timing during startup and voltage regulation, synchronization is only possible when the device has started and is regulating lamp current. Any capacitance value which makes sense for defining sweep and wait time should offer a reasonable compensation for the main oscillator PLL. How to calculate the value for the capacitor at STC to program the startup and wait timing is shown in the following paragraph. Typical values are in a µF range.

Also a phase shifted synchronization can be programmed. For this a voltage in the range between 0 V and 2 V must be applied at the PH pin. For calculating the phase shift of the main oscillator clock to the clock applied at the SYNC pin Equation 3 can be used:

$$\phi_N = V_{PH} \times 90\frac{^{o}}{V} \quad (3)$$

In this equation φ_N is the main oscillator clock phase shift and V_{PH} is the voltage applied at the PH pin.

Startup and Wait Timing

After enabling the device the device is starting at double the programmed main oscillator frequency and is sweeping down to half the programmed main oscillator frequency. The timing for the sweep is programmed with a capacitor connected between STC and GND. It can be calculated using Equation 4:

$$t_{SW} = C_{STC} \times 0.42 \times \frac{s}{\mu F} \quad (4)$$

t_{SW} is the sweep time and C_{STC} is the capacitance connected between the pins STC and GND.

If at any time the voltage regulator becomes active a wait timer is started. The timing is also programmed with a capacitor connecting STC and GND. Open lamp condition will lead to shutdown after timeout. Equation 5 shows how to calculate the wait time, t_W:

$$t_W = C_{STC} \times 0.63 \times \frac{s}{\mu F} \quad (5)$$

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Programming the Lamp Current

The lamp current which is an AC signal is sensed at the CSEN input. The AC signal is half-wave rectified through internal circuits eliminating the need for external parts except for a current sense resistor. The error amplifier will generate an average voltage from the half wave rectified input signal. This average voltage is compared to the steering signal for the lamp current. This steering signal is always provided at the ABR input. It is recommended to use the reference voltage as a maximum input voltage. For a sinusoidal feedback voltage at CSEN the peak voltage matches the voltage applied at ABR. With this information the shunt resistor for a given RMS lamp current can be calculated using Equation 6:

$$R_{Shunt} = \frac{V_{ABR}}{I_{Lamp}\sqrt{2}} \quad (6)$$

Assuming that the reference voltage is connected to ABR the lamp current is calculated as shown in the following Equation 7:

$$R_{Shunt} = \frac{3.3\ V}{I_{Lamp}\sqrt{2}} \quad (7)$$

R_{Shunt} is the value of the shunt resistor used for current sensing, V_{ABR} is the voltage applied at ABR and I_{Lamp} is the RMS value of the lamp current which should be programmed.

Analog Dimming

By modifiying the voltage at ABR the lamp current steering signal is changed. With this the lamp current is changed. The resulting lamp current for a certain voltage at ABR can be calculated as shown in Equation 8:

$$I_{Lamp} = \frac{V_{ABR}}{R_{Shunt}\sqrt{2}} \quad (8)$$

I_{Lamp} is the RMS lamp current, V_{ABR} is the voltage at ABR and R_{Shunt} is the value of the resistor used for lamp current sensing.

Programming the Voltage Regulation and Overvoltage Protection

The lamp voltage and the transformer secondary voltage are AC signals as is the lamp current. They are sensed at the VSEN input. Circuits similar to the current amplifier (CSEN) half wave rectified input are eliminating the requirement for rectification on VSEN. The error amplifier will generate an average voltage from the half wave rectified input signal. This average voltage is compared to the steering signal for the voltage. This steering signal is derived from the internal reference voltage V_{REF}. The overvoltage comparator is monitoring the peak voltage at VSEN. Its threshold is the internal reference voltage. The voltage divider ratio can be calculated using Equation 9:

$$r_V = \frac{V_{REG}}{1.87\ V} \quad (9)$$

r_V is the ratio of the voltage feedback divider and V_{REG} is the maximum RMS voltage the regulator should regulate at the lamp or transformer secondary.

The corresponding RMS voltage where the overvoltage protection comparator turns off can be calculated using Equation 10:

$$V_{OVP} = 2.33\ V \times r_V \quad (10)$$

To build the voltage feedback divider, resistive and capacitive dividers can be used. In case of a resistive divider the ratio of the feedback divider is defined as shown in Equation 11:

$$r_V = \frac{R_H + R_L}{R_L} \quad (11)$$

R_H is the upper resistor in the divider at the high voltage side, R_L is the resistor to GND.

In case of a capacitive divider the ratio can be calculated as shown in Equation 12:

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$$r_V = \frac{C_H + C_L}{C_H} \quad (12)$$

In this case C_H is the upper capacitor in the divider at the high voltage side, C_L is the capacitor to GND.

Protection

The overcurrent protection comparator (OCP) is typically used to monitor output current but can be configured to monitor any voltage. The comparator uses the internal reference voltage V_{REF} as a fixed threshold. Any voltage above the internal reference voltage at OCP for more than 4 clock cycles of the main oscillator causes the comparator to trip and generate a fault. The comparator only will trip with positive voltages above the internal reference voltage at applied to OCP. Although the input can withstand higher negative voltages there is no rectification implemented.

Compensating the Current and Voltage Regulators

The compensation networks for current and voltage regulators are connected between the negative inputs and the outputs of the respecive amplifier. At the current amplifier the pins are CAM (input) and CAO (output). At the voltage amplifier VAM (input) and VAO (output) are used. The compensation network must have a dominating capacitive characteristic, since the error amplifiers are also used for smoothing the half wave rectified feedback input signal. capacitors in parallel with resistor and capacitor in series or just capacitors are recommended. In typical applications a 2200 pF capacitor at the current amplifier and a 0.022 µF capacitor at the voltage amplifier can be used.

Synchronized Burst Dimming

To configure the device for synchronized burst dimming the dimming PWM signal must be connected directly to the BC logic input pin. The controller will turn the lamp on and off, following directly the PWM pulses applied at BC regarding frequency, phase and duty cycle. The slopes of the lamp current are controlled internally. The other pins used for configuring burst dimming, BBR and BF should have a defined state as well. It is recommended to connect BBR to 5 V (V5) and to connect BF to GND.

Independent Burst Dimming

In this configuration the device generates the low dimming frequency and the duty cycle internally. To use this feature the BC pin should be connected to GND. A capacitor connected to BF is used to program the frequency of the low frequency oscillator. The capacitance necessary to program a given burst dimming frequency can be calculated using Equation 13:

$$C_{BF} = \frac{4.7}{f_D} \times \mu F \times Hz \quad (13)$$

C_{BF} is the capacitor required to be connected between BF and GND and f_D is the low frequency oscillator frequency which should be programmed. For example a 0.047 µF capacitor is needed to program a burst frequency of 100 Hz.

To program the burst duty cycle a voltage at BBR is used. The duty cycle can be calculated using Equation 14:

$$D_B = V_{BBR} \times 50 \times \frac{\%}{V} \quad (14)$$

D_B is the resulting burst duty cycle and V_{BBR} is the voltage applied at the BBR pin. The operating voltage range for duty cycle programming is 0 V to 2 V. 0 V at BBR will program 0% burst duty cycle and 2 V will program 100% burst duty cycle.

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Phase Shifted Burst Dimming

The device also supports phase shifted burst dimming. In this configuration a direct PWM burst signal is used which must be connected to BC. The internal low frequency oscillator must be programmed as described in the independent burst dimming section and in Equation 13. Since the internal low frequency oscillator will be synchronized to the frequency connected to BC it is recommended to program the internal low frequency close to the frequency at BC. The synchronization is done using a PLL circuit. This PLL circuit needs an external compensation network connected at BBR. For a typical burst frequency in the 100 Hz range using a 0.68 µF capacitor in series with a 100 kΩ resistor is recommended. This R - C network should be connected between BBR and GND.

The phase shift of the dimming burst compared to the input signal at BC is programmed with a voltage applied at PH. The resulting phase shift can be calculated using Equation 15:

$$\phi_B = V_{PH} \times 180 \times \frac{^{o}}{V} \tag{15}$$

φ_B is the phase shift of the dimming burst and V_{PH} is the voltage applied at the PH pin.

Layout Considerations

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

To layout the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

The maximum recommended junction temperature (T_J) of the TPS68000 device is 125°C. The thermal resistance of the 30-pin TSSOP package (PW) is $R_{\theta JA}$ = 63.9°C/W. Specified regulator operation is assured to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 626 mW. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{125^{o}C - 85^{o}C}{63.9 \frac{^{o}C}{W}} = 626 \text{ mW} \tag{16}$$

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS68000DBT	NRND	TSSOP	DBT	30	60	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS68000	
TPS68000DBTR	NRND	TSSOP	DBT	30	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TPS68000	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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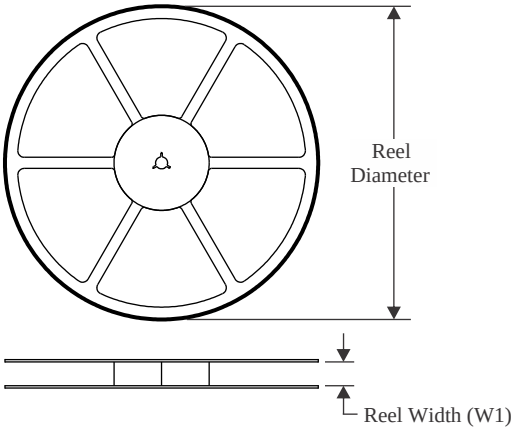
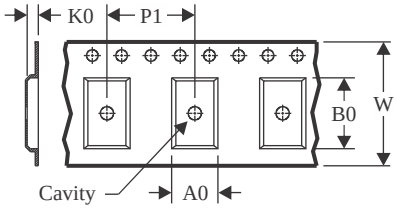
TAPE AND REEL INFORMATION

REEL DIMENSIONS

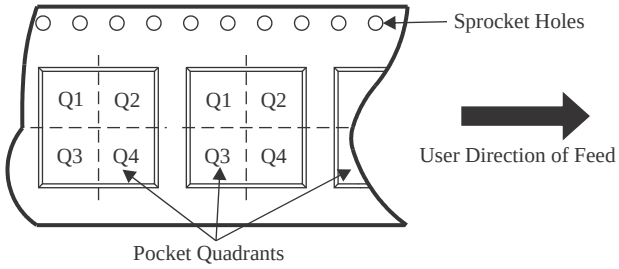


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

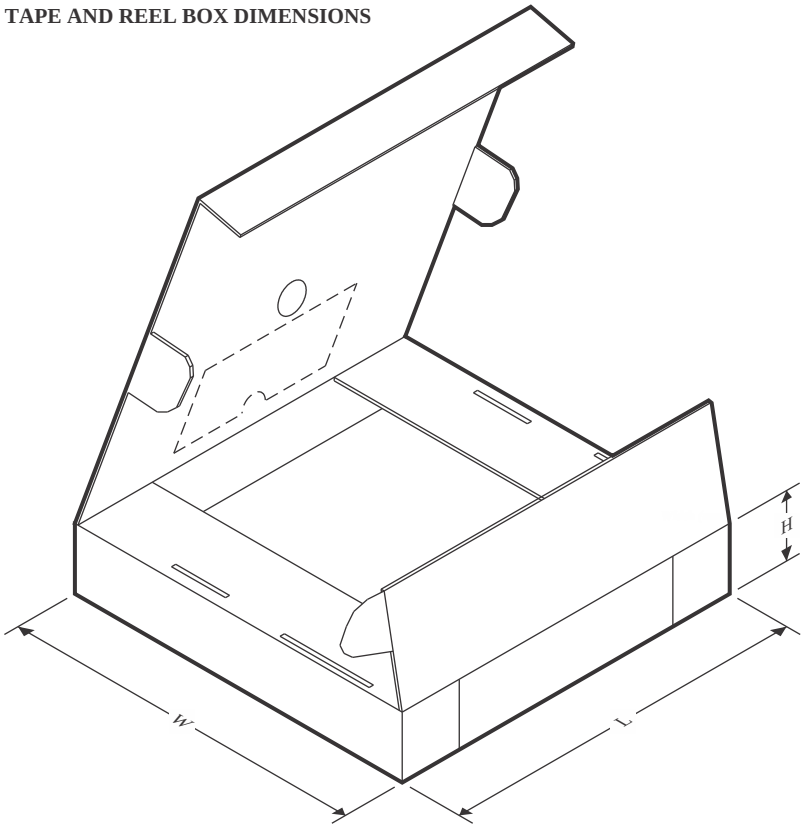
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS68000DBTR	TSSOP	DBT	30	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

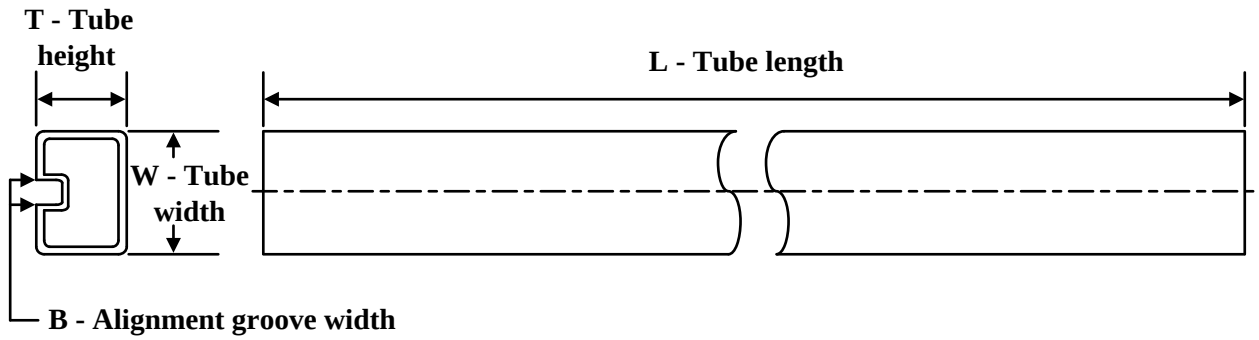
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS68000DBTR	TSSOP	DBT	30	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

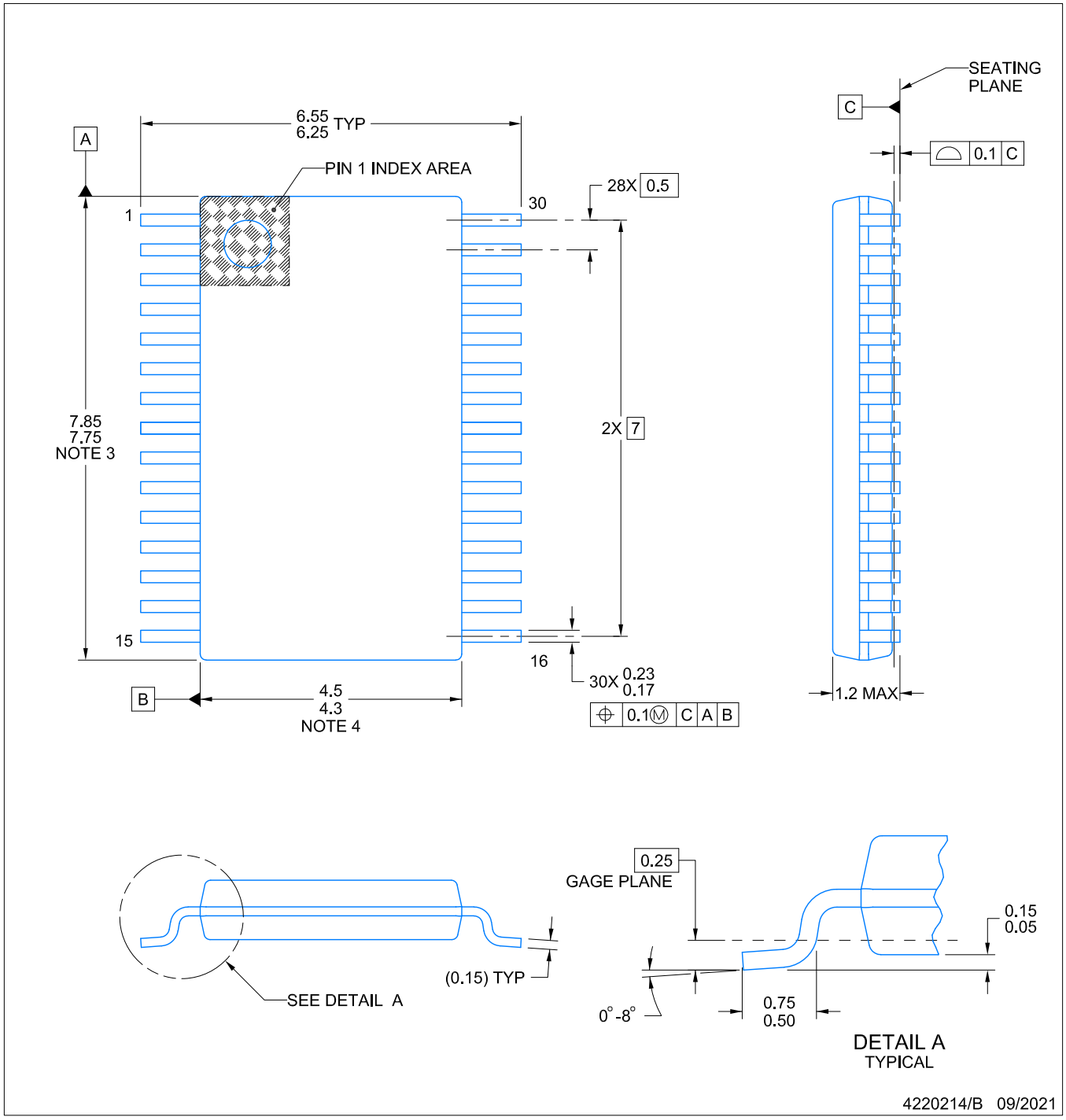
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS68000DBT	DBT	TSSOP	30	60	530	10.2	3600	3.5

PACKAGE OUTLINE

DBT0030A

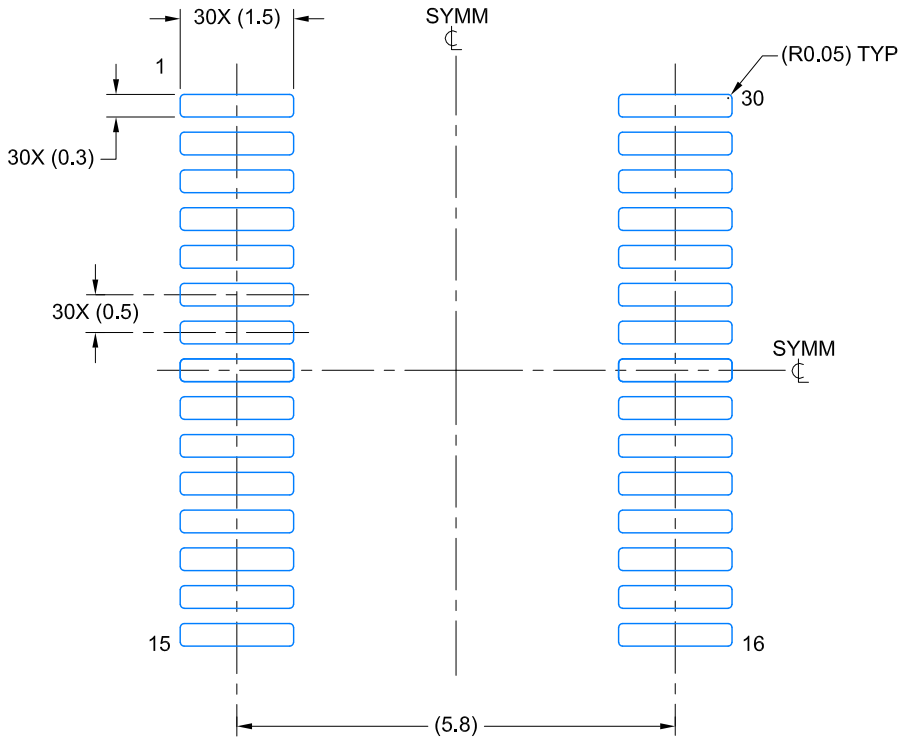
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

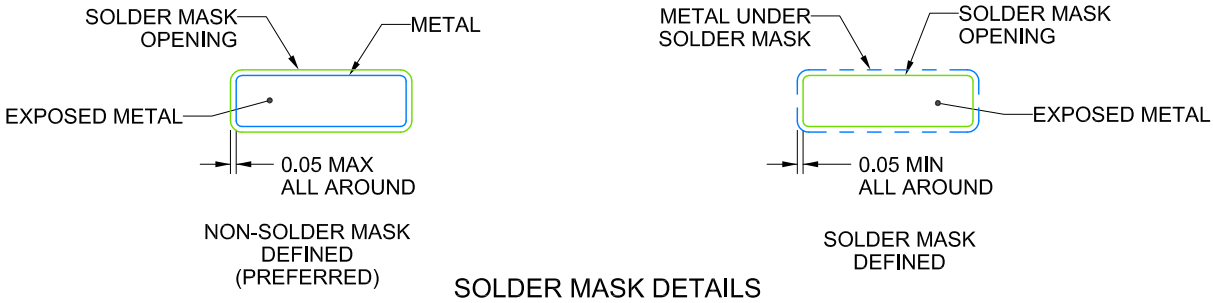


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

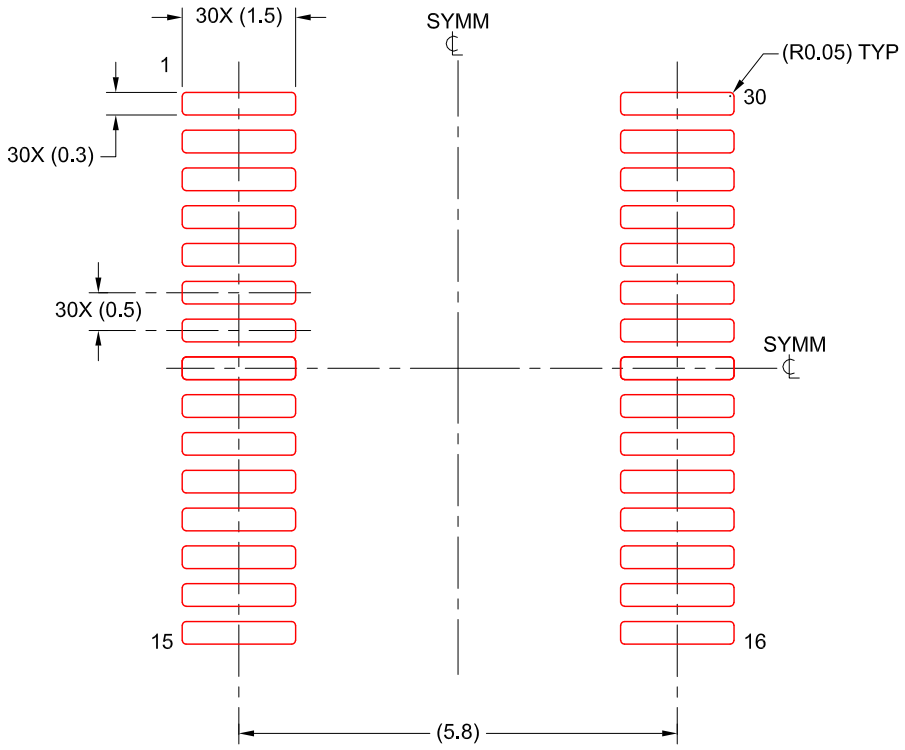


SOLDER MASK DETAILS

4220214/B 09/2021

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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