

CSD17579Q3A 30V N 通道 NexFET™ 功率 MOSFET

1 特性

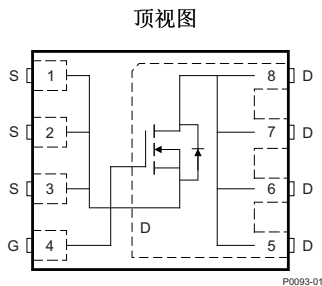
- 低 Q_g 和 Q_{gd}
- 低 $R_{DS(on)}$
- 低热阻
- 雪崩级
- 无铅
- 符合 RoHS 标准
- 无卤素
- 小外形尺寸无引线 (SON) 3.3mm x 3.3mm 塑料封装

2 应用

- 用于网络、电信和计算系统中的 负载点 同步降压转换器
- 针对控制场效应晶体管 (FET) 应用进行了优化

3 说明

这款 30V, 8.7mΩ, SON 3.3mm x 3.3mm NexFET™ 功率 MOSFET 旨在最大限度地降低功率转换应用中的损耗提供了灵活性和便利性。



产品概要

$T_A = 25^\circ\text{C}$		典型值		单位
V_{DS}	漏源电压	30		V
Q_g	总栅极电荷 (4.5V)	5.3		nC
Q_{gd}	栅极电荷 (栅极到漏极)	1.2		nC
$R_{DS(on)}$	漏源导通电阻	$V_{GS} = 4.5\text{V}$	11.8	mΩ
		$V_{GS} = 10\text{V}$	8.7	mΩ
$V_{GS(th)}$	阈值电压	1.5		V

订购信息⁽¹⁾

器件	包装介质	数量	封装	发货
CSD17579Q3A	13 英寸卷带	2500	SON 3.3mm x 3.3mm 塑料封装	卷带封装
CSD17579Q3AT	7 英寸卷带	250		

(1) 如需了解所有可用封装, 请参阅产品说明书末尾的可订购产品附录。

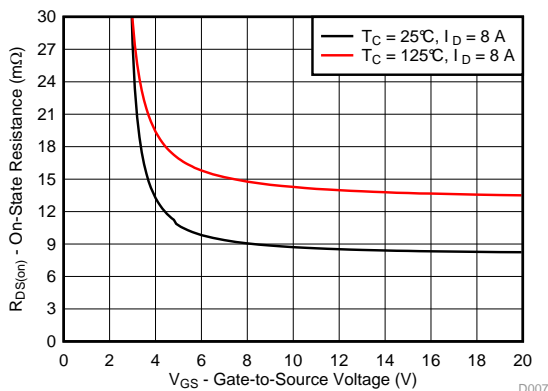
绝对最大额定值

$T_A = 25^\circ\text{C}$		值	单位
V_{DS}	漏源电压	30	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流 (受封装限制)	20	A
	持续漏极电流 (受芯片限制), $T_C = 25^\circ\text{C}$ 时测得	39	
	持续漏极电流 ⁽¹⁾	11	
I_{DM}	脉冲漏极电流 ⁽²⁾	106	A
P_D	功率耗散 ⁽¹⁾	2.5	W
	功率耗散, $T_C = 25^\circ\text{C}$	29	
T_J, T_{stg}	工作结温, 储存温度	-55 至 150	°C
E_{AS}	雪崩能量, 单一脉冲 $I_D = 17\text{A}, L = 0.1\text{mH}, R_G = 25\Omega$	14	mJ

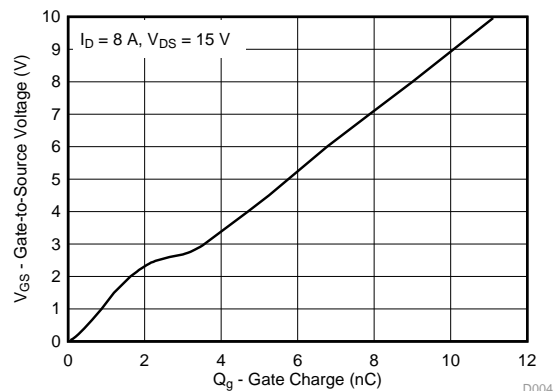
(1) $R_{\theta JA} = 50^\circ\text{C/W}$, 这是在厚度为 0.06 英寸的环氧板 (FR4) 印刷电路板 (PCB) 上的 1 英寸² 2 盎司的铜过渡垫片上测得的典型值。

(2) 最大 $R_{\theta JC} = 5.4^\circ\text{C/W}$, 脉冲持续时间 $\leq 100\mu\text{s}$, 占空比 $\leq 1\%$

$R_{DS(on)}$ 与 V_{GS} 对比



栅极电荷



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (September 2014) to Revision A	Page
• 在绝对最大额定值表中更新了功率耗散值	1
• 已添加 添加了 社区资源 部分	7
• 更新了封装尺寸图	8
• 更新了 PCB 图	9
• 更新了模版布局图	9

5 Specifications

5.1 Electrical Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
V_{DSS}	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
I_{DSS}	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$			1	μA
I_{GSS}	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.1	1.5	1.9	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 4.5\text{ V}, I_D = 8\text{ A}$		11.8	14.2	m Ω
		$V_{GS} = 10\text{ V}, I_D = 8\text{ A}$		8.7	10.2	m Ω
g_{fs}	Transconductance	$V_{DS} = 3\text{ V}, I_D = 8\text{ A}$		37		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$		768	998	pF
C_{oss}	Output capacitance			93	121	pF
C_{rss}	Reverse transfer capacitance			38	49	pF
R_G	Series gate resistance			1.9	3.8	Ω
Q_g	Gate charge total (4.5 V)	$V_{DS} = 15\text{ V}, I_D = 8\text{ A}$		5.3	6.9	nC
Q_g	Gate charge total (10 V)			11.5	15.0	nC
Q_{gd}	Gate charge gate-to-drain			1.2		nC
Q_{gs}	Gate charge gate-to-source			2.2		nC
$Q_{g(th)}$	Gate charge at V_{th}			1.1		nC
Q_{oss}	Output charge		$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}$		3.0	
$t_{d(on)}$	Turn on delay time	$V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 8\text{ A}, R_G = 0\ \Omega$		2		ns
t_r	Rise time			5		ns
$t_{d(off)}$	Turn off delay time			11		ns
t_f	Fall time			1		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	$I_{SD} = 8\text{ A}, V_{GS} = 0\text{ V}$		0.8	1.0	V
Q_{rr}	Reverse recovery charge	$V_{DS} = 15\text{ V}, I_F = 8\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		3.4		nC
t_{rr}	Reverse recovery time			5		ns

5.2 Thermal Information

($T_A = 25^\circ\text{C}$ unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance ⁽¹⁾			5.4	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance ⁽¹⁾⁽²⁾			60	$^\circ\text{C}/\text{W}$

- $R_{\theta JC}$ is determined with the device mounted on a 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.

CSD17579Q3A

ZHCST3A – SEPTEMBER 2014 – REVISED JANUARY 2016

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Max $R_{\theta JA} = 60^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2 oz. (0.071 mm thick)
Cu.

M0161-01

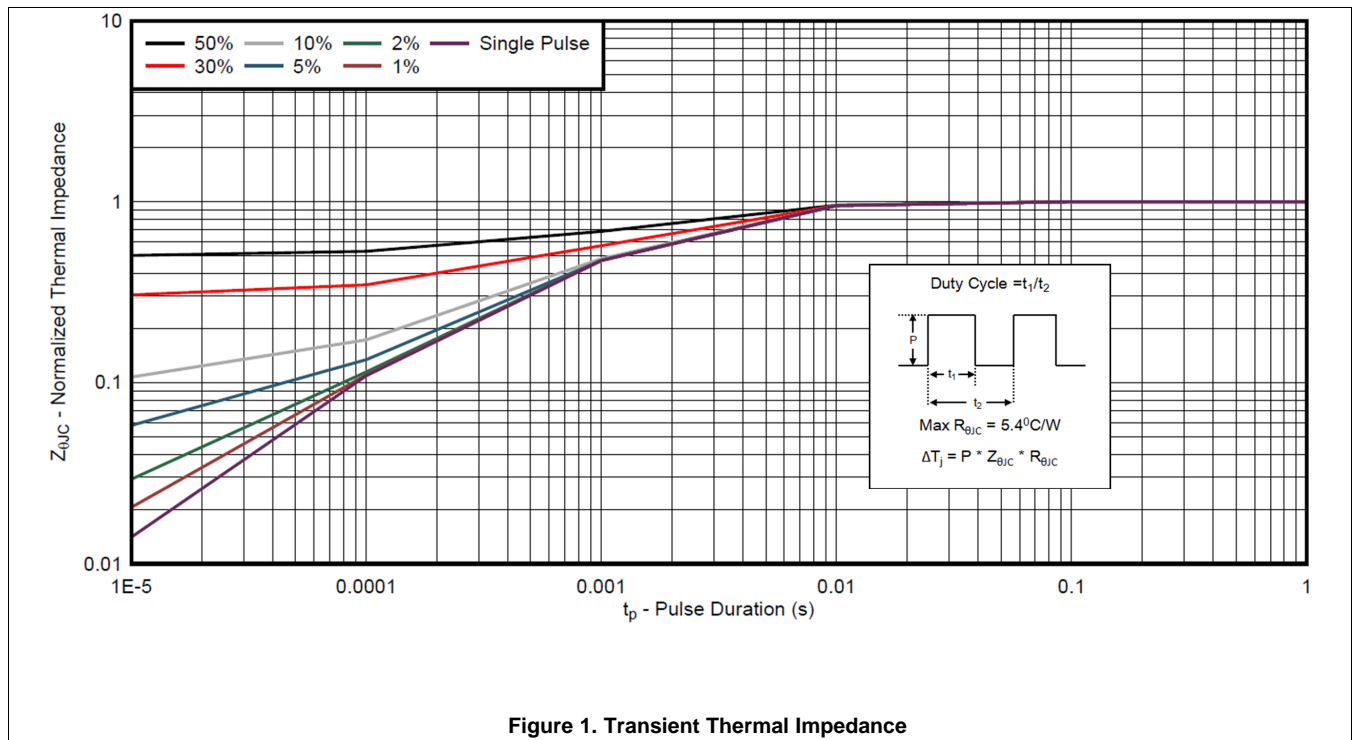


Max $R_{\theta JA} = 145^{\circ}\text{C/W}$
when mounted on a
minimum pad area of 2
oz. (0.071 mm thick)
Cu.

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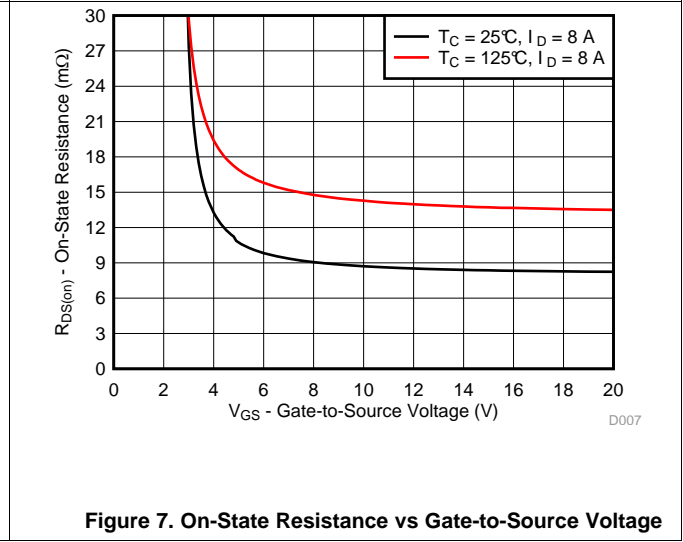
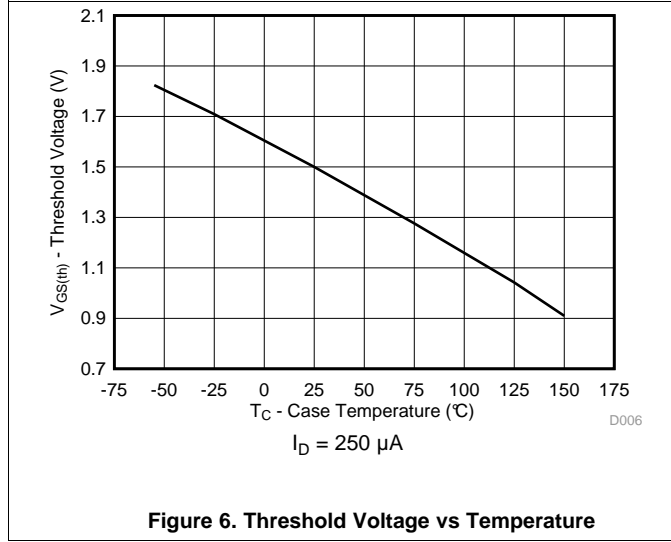
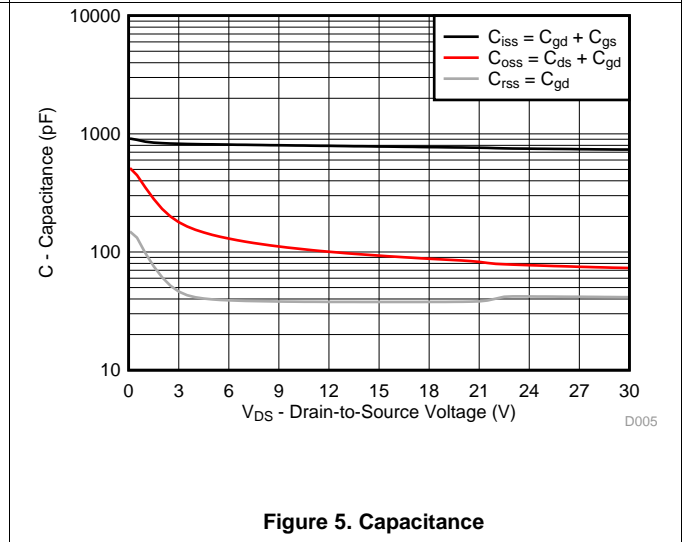
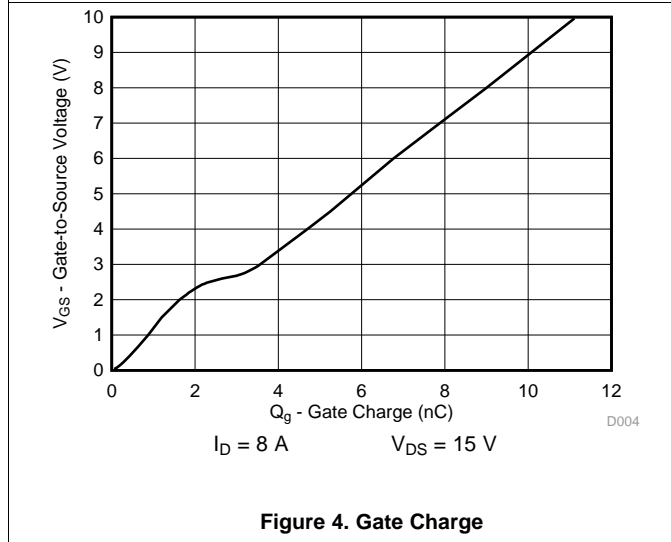
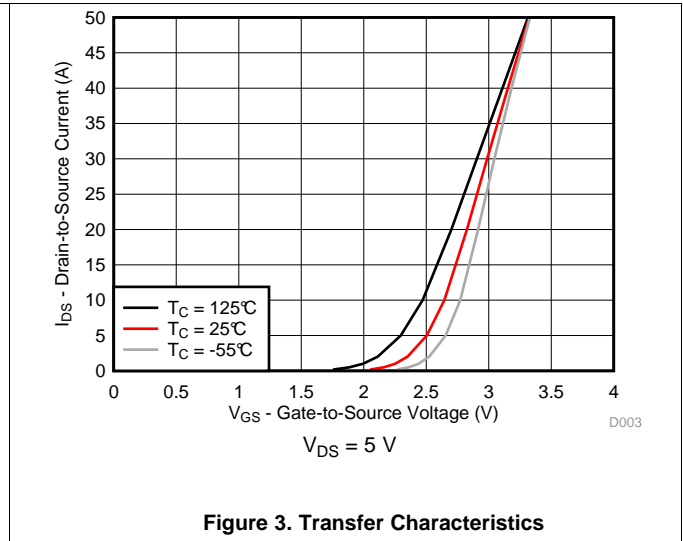
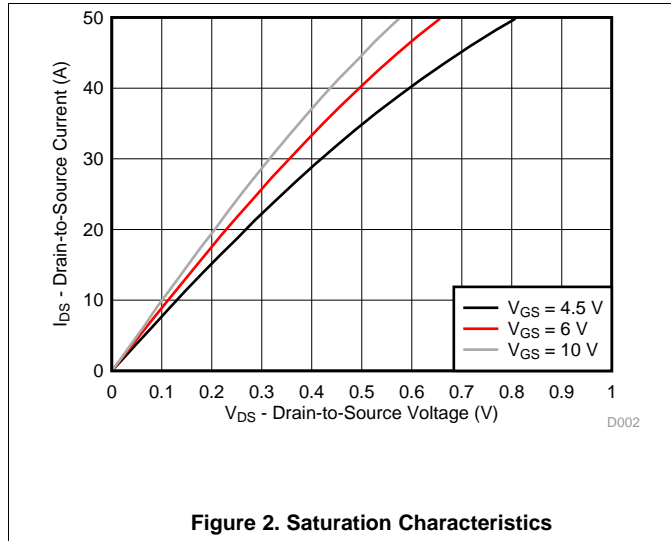
5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

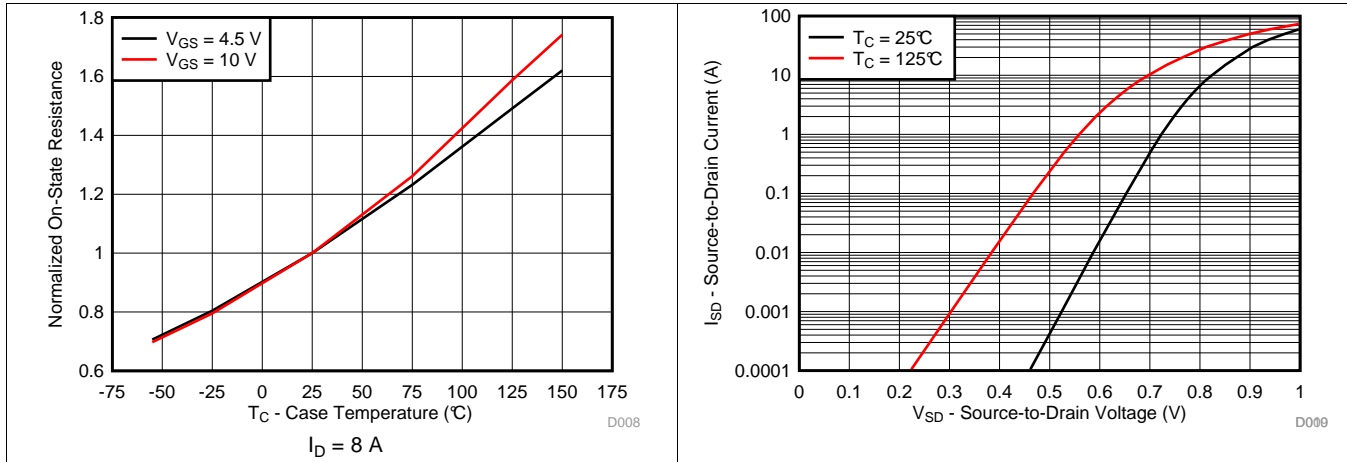


Figure 8. Normalized On-State Resistance vs Temperature

Figure 9. Typical Diode Forward Voltage

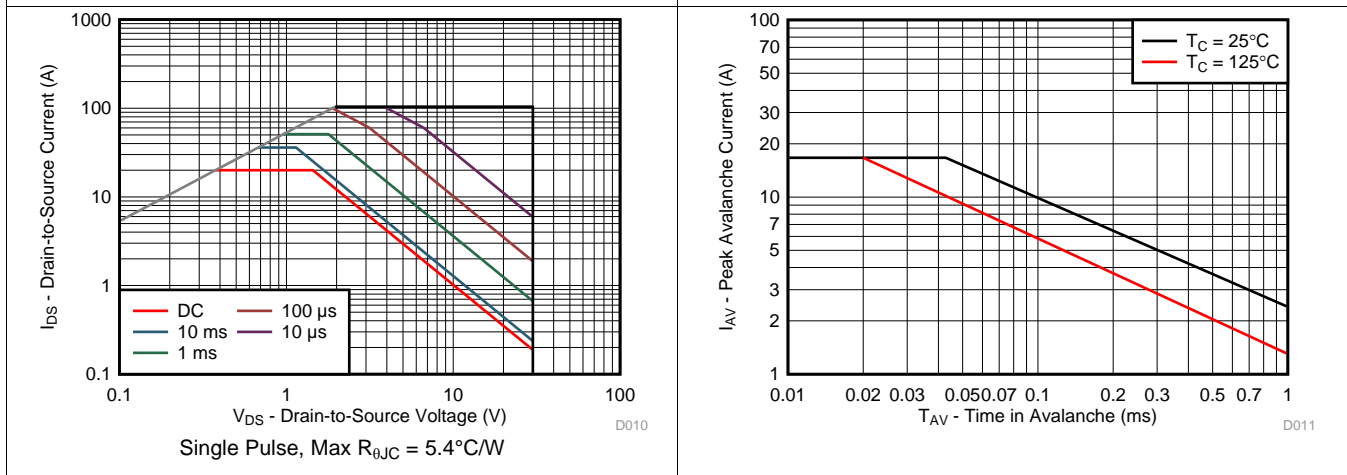


Figure 10. Maximum Safe Operating Area

Figure 11. Single Pulse Unclamped Inductive Switching

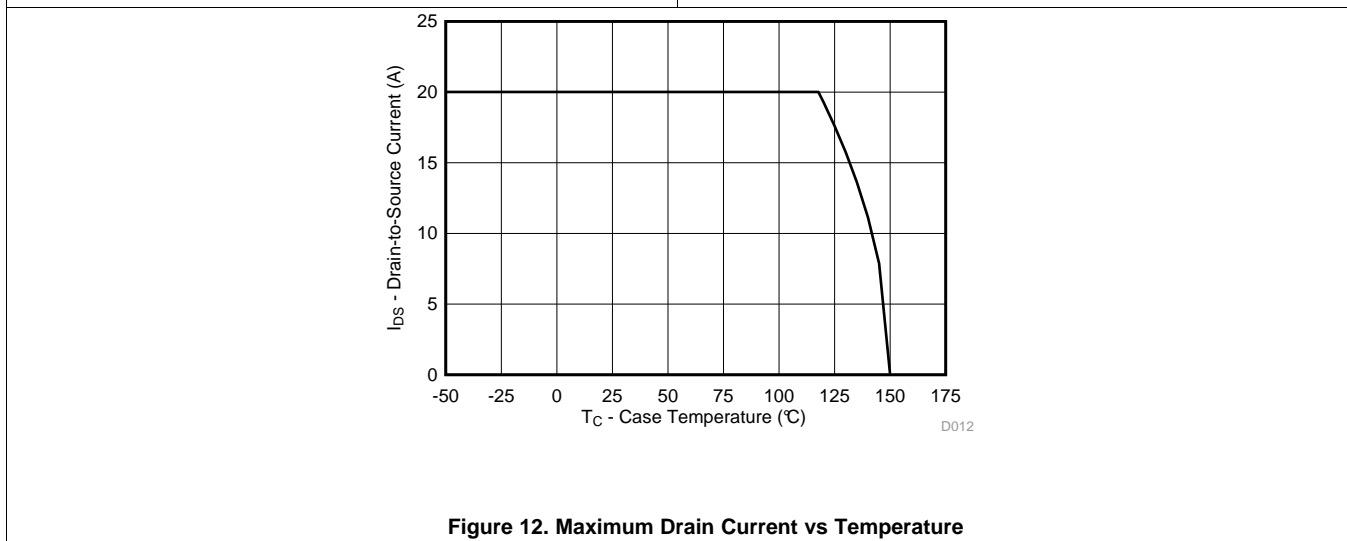


Figure 12. Maximum Drain Current vs Temperature

6 器件和文档支持

6.1 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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6.2 商标

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6.3 静电放电警告



这些装置包含有限的内置 ESD 保护。存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.4 Glossary

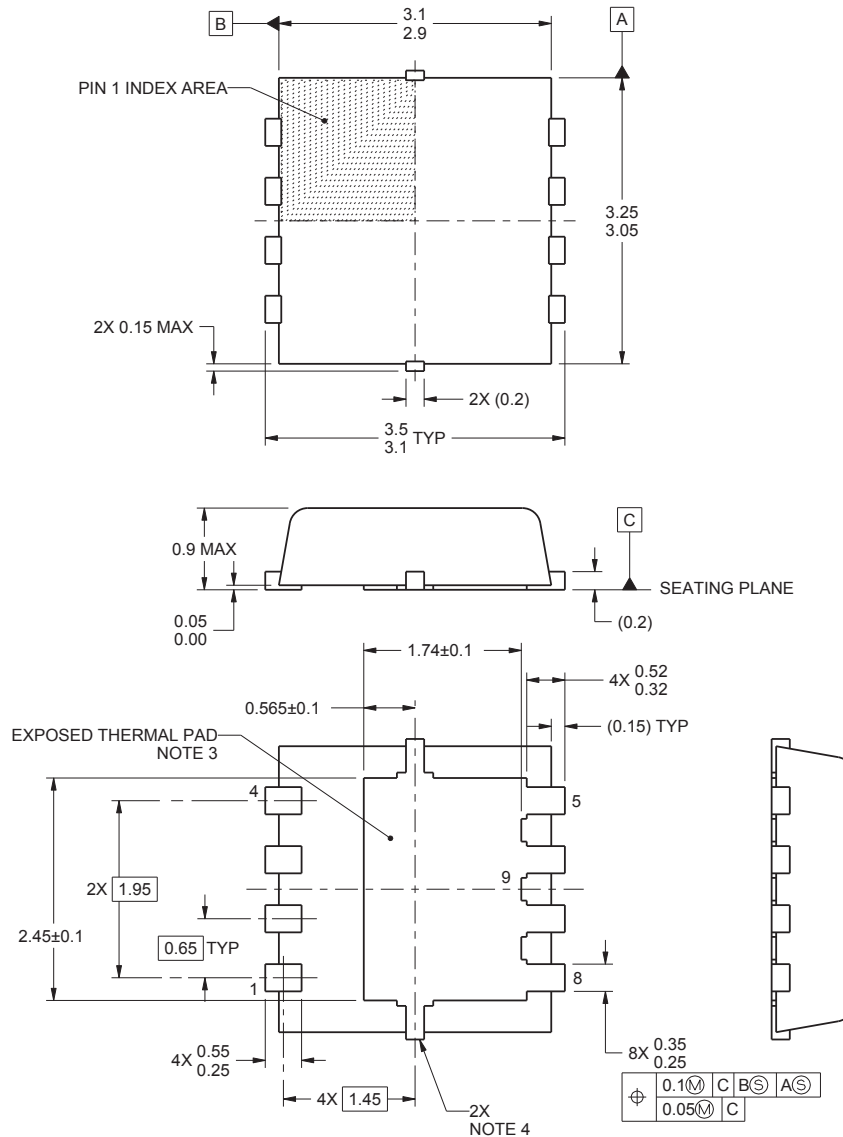
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此产品说明书的浏览器版本，请参阅左侧的导航。

7.1 Q3A 封装尺寸



1. 所有线性尺寸的单位均为毫米。括号中的任何尺寸仅供参考。尺寸和公差值符合 ASME Y14.5M 标准。
2. 本图如有变更，恕不另行通知。
3. 必须在印刷电路板上焊接封装散热焊盘，以获得良好的散热和机械性能。
4. 金属化 特性 为供应商选配特性，因此封装上可能不具备。
5. 所有尺寸不包括模具毛边或突出部分。

7.4 Q3A 卷带信息


- Notes:
1. 10 链轮孔距累积容差 ± 0.2
 2. 每 100mm 长度的翘曲不能超过 1mm, 在 250mm 长度上不累积
 3. 材料: 黑色抗静电聚苯乙烯
 4. 全部尺寸单位为 mm, 除非另外注明。
 5. 厚度: 0.30 ± 0.05 mm
 6. MSL1 260°C (红外 (IR) 和传导) PbF 回流焊兼容

M0144-01

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17579Q3A	ACTIVE	VSONP	DNH	8	2500	RoHS & Green	SN	Level-1-260C-UNLIM		17579	Samples
CSD17579Q3AT	ACTIVE	VSONP	DNH	8	250	RoHS & Green	SN	Level-1-260C-UNLIM	-55 to 150	17579	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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