

## SNx4AHCT541 具有三态输出的八路缓冲器/驱动器

### 1 特性

- 输入兼容 TTL 电压
- 闩锁性能超过 250mA，符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 1000V 充电器件模型 (C101)
- 对于符合 MIL-PRF-38535 标准的产品，所有参数均经过测试，除非另有说明。对于所有其他产品，生产流程不一定包含对所有参数的测试。

### 2 说明

'AHCT541 八通道缓冲器/驱动器非常适合用于驱动总线或缓冲存储器地址寄存器。该类器件在封装的相对两侧具有输入端和输出端，有助于印刷电路板布局布线。

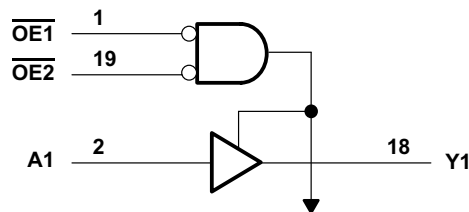
#### 器件信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>	本体尺寸 <sup>(3)</sup>
SNx4AHCT541	N ( PDIP , 20 )	24.33mm x 9.4mm	25.40mm x 6.35mm
	DB ( SSOP , 20 )	7.2mm x 7.8mm	7.50mm x 5.30mm
	PW ( TSSOP , 20 )	6.50mm x 6.4mm	6.50mm x 4.40mm
	DGV ( TVSOP , 20 )	5.00mm x 6.4mm	5.00mm x 4.40mm
	DW ( SOIC , 20 )	12.80mm x 10.3mm	12.80mm x 7.50mm
	J ( CDIP , 20 )	24.2mm x 7.62mm	24.2mm x 6.92mm
	W ( CFP , 20 )	13.09mm x 8.13mm	13.09mm x 6.92mm

(1) 有关更多信息，请参阅节 10。

(2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。

(3) 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



To Seven Other Channels

展示各触发器的逻辑图 (正逻辑)



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### 3 Pin Configuration and Functions

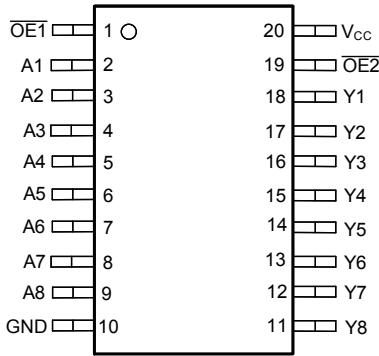


图 3-1. SN54AHCT541 J or W Package;  
 SN74AHCT541 DB, DW, N, NS, or PW Package; 20-  
 Pin SSOP, SOIC, PDIP, SOP, or TSSOP (Top View)

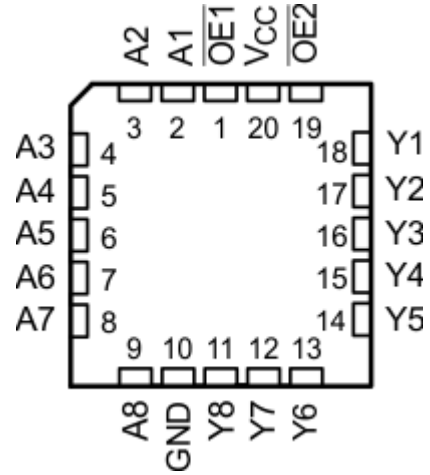


图 3-2. SN54AHCT541 FK Package, 20-Pin LCCC  
 (Top View)

表 3-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{OE1}$	I	Output Enable 1
2	A1	I	A1 Input
3	A2	I	A2 Input
4	A3	I	A3 Input
5	A4	I	A4 Input
6	A5	I	A5 Input
7	A6	I	A6 Input
8	A7	I	A7 Input
9	A8	I	A8 Input
10	GND	—	Ground
11	Y8	O	Y8 Output
12	Y7	O	Y7 Output
13	Y6	O	Y6 Output
14	Y5	O	Y5 Output
15	Y4	O	Y4 Output
16	Y3	O	Y3 Output
17	Y2	O	Y2 Output
18	Y1	O	Y1 Output
19	$\overline{OE2}$	I	Output Enable 2
20	V <sub>CC</sub>	—	Power Pin

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	7	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	7	V
V <sub>O</sub>	Output voltage range <sup>(2)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-20	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>CC</sub>	±20	mA
I <sub>O</sub>	Continuous output current	V <sub>O</sub> = 0 to V <sub>CC</sub>	±25	mA
	Continuous current through V <sub>CC</sub> or GND		±75	mA

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 4.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±1000
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±2000

- (1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54AHCT541		SN74AHCT541		UNIT
		MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		V
V <sub>IL</sub>	Low-level Input voltage		0.8		0.8	V
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-8		-8	mA
I <sub>OL</sub>	Low-level output current		8		8	mA
Δt/Δv	Input transition rise or fall rate		20		20	ns/V
T <sub>A</sub>	Operating free-air temperature	-55	125	-40	125	°C

- (1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

### 4.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74AHCT541						UNIT	
	DB (SSOP)	DGV (TVSOP)	DW (SOIC)	N (PDIP)	NS (SO)	PW (TSSOP)		
	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS	20 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	87.2	92	81.1	69	60	116.8	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report ([SPRA953](#)).

## 4.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		T <sub>A</sub> = -40°C TO 125°C		UNIT
					Recommended		SN54AHCT541	SN74AHCT541	SN74AHCT541		
			MIN	TYP	MAX	MIN			MAX	MIN	
V <sub>OH</sub>	I <sub>OH</sub> = -50μA	4.5V	4.4	4.5	4.4		4.4		4.4		V
	I <sub>OH</sub> = -8mA		3.94		3.8		3.8		3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50μA	4.5V	0.1		0.1		0.1		0.1		V
	I <sub>OH</sub> = 8mA		0.36		0.44		0.44		0.44		
I <sub>I</sub>	V <sub>I</sub> = 5.5V or GND	0V to 5.5V	±0.1		±1 <sup>(1)</sup>		±1		±1		μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.5 V	±0.25		±2.5		±2.5		±2.5		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5V	4		40		20		40		μA
Δ I <sub>CC</sub> <sup>(2)</sup>	One input at 3.4V, Other inputs at V <sub>CC</sub> or GND	5.5V	1.35		1.5		1.5		1.5		mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5V	2 10				10				pF
C <sub>O</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5V	4								pF

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested at V<sub>CC</sub> = 0V.

(2) This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0V or V<sub>CC</sub>.

## 4.6 Switching Characteristics

over recommended operating free-air temperature range, V<sub>CC</sub> = 5V ± 0.5V (unless otherwise noted) (see [图 5-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C		T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		T <sub>A</sub> = -40°C TO 125°C		UNIT
						Recommended		SN54AHCT541	SN74AHCT541	SN74AHCT541		
				TYP	MAX	MIN	MAX			MIN	MAX	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 15pF	4.1 <sup>(1)</sup>	6.0 <sup>(1)</sup>	1 <sup>(1)</sup>	6.5 <sup>(1)</sup>	1	6.5	1	6.5	ns
t <sub>PHL</sub>				4.1 <sup>(1)</sup>	6.0 <sup>(1)</sup>	1 <sup>(1)</sup>	6.5 <sup>(1)</sup>	1	6.5	1	6.5	
t <sub>PZH</sub>	OE	Y	C <sub>L</sub> = 15pF	5.0 <sup>(1)</sup>	7.0 <sup>(1)</sup>	1 <sup>(1)</sup>	8.0 <sup>(1)</sup>	1	8.0	1	8.0	ns
t <sub>PZL</sub>				5.0 <sup>(1)</sup>	7.0 <sup>(1)</sup>	1 <sup>(1)</sup>	8.0 <sup>(1)</sup>	1	8.0	1	8.0	
t <sub>PHZ</sub>	OE	Y	C <sub>L</sub> = 15pF	4.5 <sup>(1)</sup>	7.0 <sup>(1)</sup>	1 <sup>(1)</sup>	8.0 <sup>(1)</sup>	1	8.0	1	8.0	ns
t <sub>PLZ</sub>				4.5 <sup>(1)</sup>	7.0 <sup>(1)</sup>	1 <sup>(1)</sup>	8.0 <sup>(1)</sup>	1	8.0	1	8.0	
t <sub>PLH</sub>	A	Y	C <sub>L</sub> = 50pF	6.2	8.5	1	9.5	1	9.5	1	9.5	ns
t <sub>PHL</sub>				6.2	8.5	1	9.5	1	9.5	1	9.5	
t <sub>PZH</sub>	OE	Y	C <sub>L</sub> = 50pF	7.5	10.0	1	12	1	12	1	12	ns
t <sub>PZL</sub>				7.5	10.0	1	12	1	12	1	12	
t <sub>PHZ</sub>	OE	Y	C <sub>L</sub> = 50pF	7.0	10.0	1	12	1	12	1	12	ns
t <sub>PLZ</sub>				7.0	10.0	1	12	1	12	1	12	
t <sub>sk(o)</sub>			C <sub>L</sub> = 50pF	1 <sup>(2)</sup>				1		1		ns

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

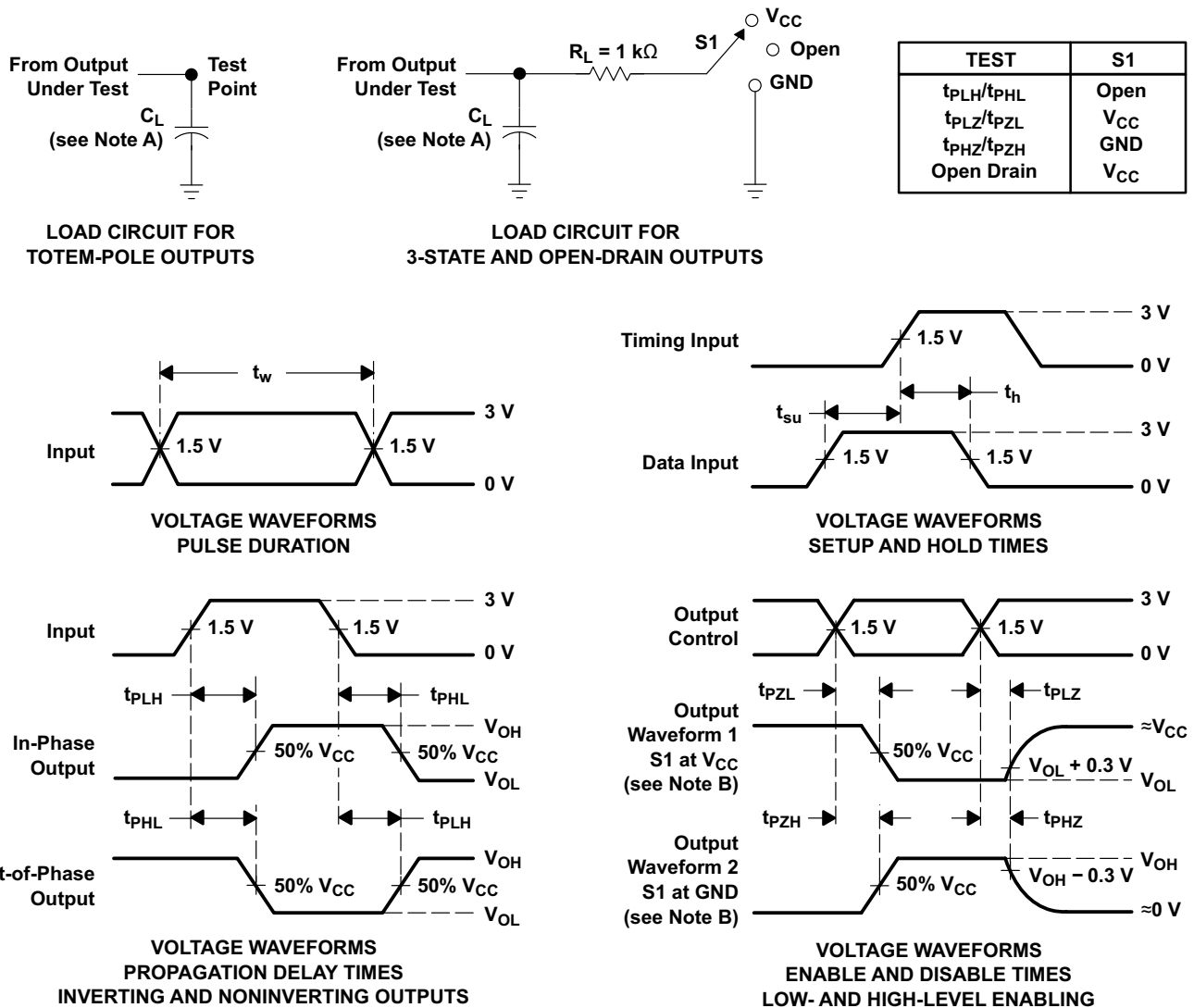
(2) On products compliant to MIL-PRF-38535, this parameter does not apply.

## 4.7 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	12	pF

## 5 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

图 5-1. Load Circuit and Voltage Waveforms

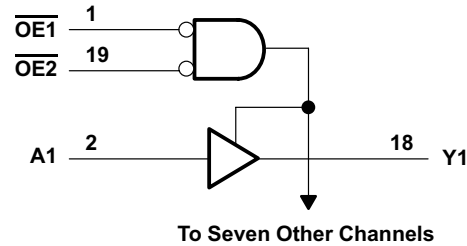
## 6 Detailed Description

### 6.1 Overview

The 3-state control gate is a 2-input AND gate with active-low inputs so that if either output-enable ( $\overline{OE1}$  or  $\overline{OE2}$ ) input is high, all corresponding outputs are in the high-impedance state. The outputs provide non-inverted data when they are not in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

### 6.2 Functional Block Diagram



### 6.3 Device Functional Modes

表 6-1 lists the functional modes for the SNx4AHCT541 devices.

**表 6-1. Function Table  
(Each Buffer/Driver)**

INPUTS			OUTPUT Y
OE1	OE2	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z



## 7 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 7.1 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the [节 4.3](#) table. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply,  $0.1 \mu F$  is recommended. If there are multiple  $V_{CC}$  terminals then  $0.01 \mu F$  or  $0.022 \mu F$  is recommended for each power terminal. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A  $0.1 \mu F$  and  $1 \mu F$  are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in the [图 7-1](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

#### 7.2.2 Layout Example

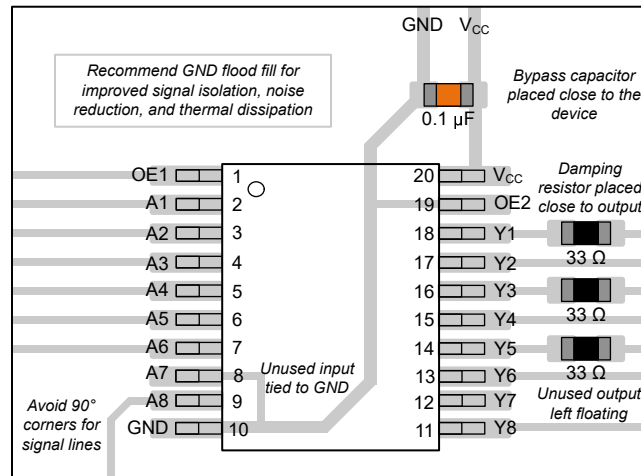


图 7-1. Example Layout for the SN74AHCT541

## 8 Device and Documentation Support

### 8.1 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

#### 8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

#### Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54AHCT541	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74AHCT541	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 8.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 8.6 Glossary

[SLYZ022](#) — TI Glossary.

This glossary lists and explains terms, acronyms and definitions.

## 9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision P (June 2013) to Revision Q (August 2024)	Page
• 删除了整个数据表中对机器放电模型的引用.....	1
• 向“特性”列表中添加了“军用免责声明”.....	1
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 添加了 <a href="#">器件信息表</a> 、 <a href="#">引脚功能表</a> 、 <a href="#">ESD 等级表</a> 、 <a href="#">热性能信息表</a> 、 <a href="#">器件功能模式</a> 、“应用和实施”部分、 <a href="#">器件和文档支持</a> 部分以及 <a href="#">机械、封装和可订购信息</a> 部分.....	1

- Updated  $R_{\theta JA}$  values: PW = 83 to 116.8, DB = 70 to 87.2, DW = 58 to 81.1; Updated PW, DB, and DW packages for  $R_{\theta JC(top)}$ ,  $R_{\theta JB}$ ,  $\Psi_{JT}$ ,  $\Psi_{JB}$ , and  $R_{\theta JC(bot)}$ , all values in  $^{\circ}C/W$  ..... 4

**Changes from Revision O (July 2003) to Revision P (June 2013) Page**

- Extended operating temperature range to 125 $^{\circ}C$ .....4
- Updated  $R_{\theta JA}$  values: PW = 83 to 116.8, all values in  $^{\circ}C/W$  ..... 4

**10 Mechanical, Packaging, and Orderable Information**

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9685801Q2A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9685801Q2A SNJ54AHCT 541FK	<a href="#">Samples</a>
5962-9685801QRA	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685801QR A SNJ54AHCT541J	<a href="#">Samples</a>
5962-9685801QSA	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685801QS A SNJ54AHCT541W	<a href="#">Samples</a>
SN74AHCT541DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(AHCT541, HB541)	<a href="#">Samples</a>
SN74AHCT541DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	-40 to 125	AHCT541	
SN74AHCT541DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT541	<a href="#">Samples</a>
SN74AHCT541N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 125	SN74AHCT541N	<a href="#">Samples</a>
SN74AHCT541NSR	ACTIVE	SOP	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHCT541	<a href="#">Samples</a>
SN74AHCT541PW	OBSOLETE	TSSOP	PW	20		TBD	Call TI	Call TI	-40 to 125	HB541	
SN74AHCT541PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(AHCT541, HB541)	<a href="#">Samples</a>
SN74AHCT541PWRE4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541	<a href="#">Samples</a>
SN74AHCT541PWRG3	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	HB541	<a href="#">Samples</a>
SN74AHCT541PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HB541	<a href="#">Samples</a>
SNJ54AHCT541FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962- 9685801Q2A SNJ54AHCT 541FK	<a href="#">Samples</a>
SNJ54AHCT541J	ACTIVE	CDIP	J	20	20	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685801QR A SNJ54AHCT541J	<a href="#">Samples</a>
SNJ54AHCT541W	ACTIVE	CFP	W	20	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9685801QS A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
										SNJ54AHCT541W	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54AHCT541, SN74AHCT541 :**

- Catalog : [SN74AHCT541](#)

- Enhanced Product : [SN74AHCT541-EP](#), [SN74AHCT541-EP](#)
- Military : [SN54AHCT541](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHCT541DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT541DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74AHCT541DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74AHCT541DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHCT541NSR	SOP	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74AHCT541PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHCT541PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74AHCT541PWRG3	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74AHCT541PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHCT541DBR	SSOP	DB	20	2000	353.0	353.0	32.0
SN74AHCT541DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74AHCT541DWR	SOIC	DW	20	2000	356.0	356.0	45.0
SN74AHCT541DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHCT541NSR	SOP	NS	20	2000	367.0	367.0	45.0
SN74AHCT541PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74AHCT541PWR	TSSOP	PW	20	2000	353.0	353.0	32.0
SN74AHCT541PWRG3	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74AHCT541PWRG4	TSSOP	PW	20	2000	356.0	356.0	35.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-9685801Q2A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-9685801QSA	W	CFP	20	25	506.98	26.16	6220	NA
SN74AHCT541N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54AHCT541FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54AHCT541W	W	CFP	20	25	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20

PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



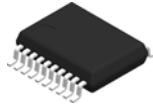
SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

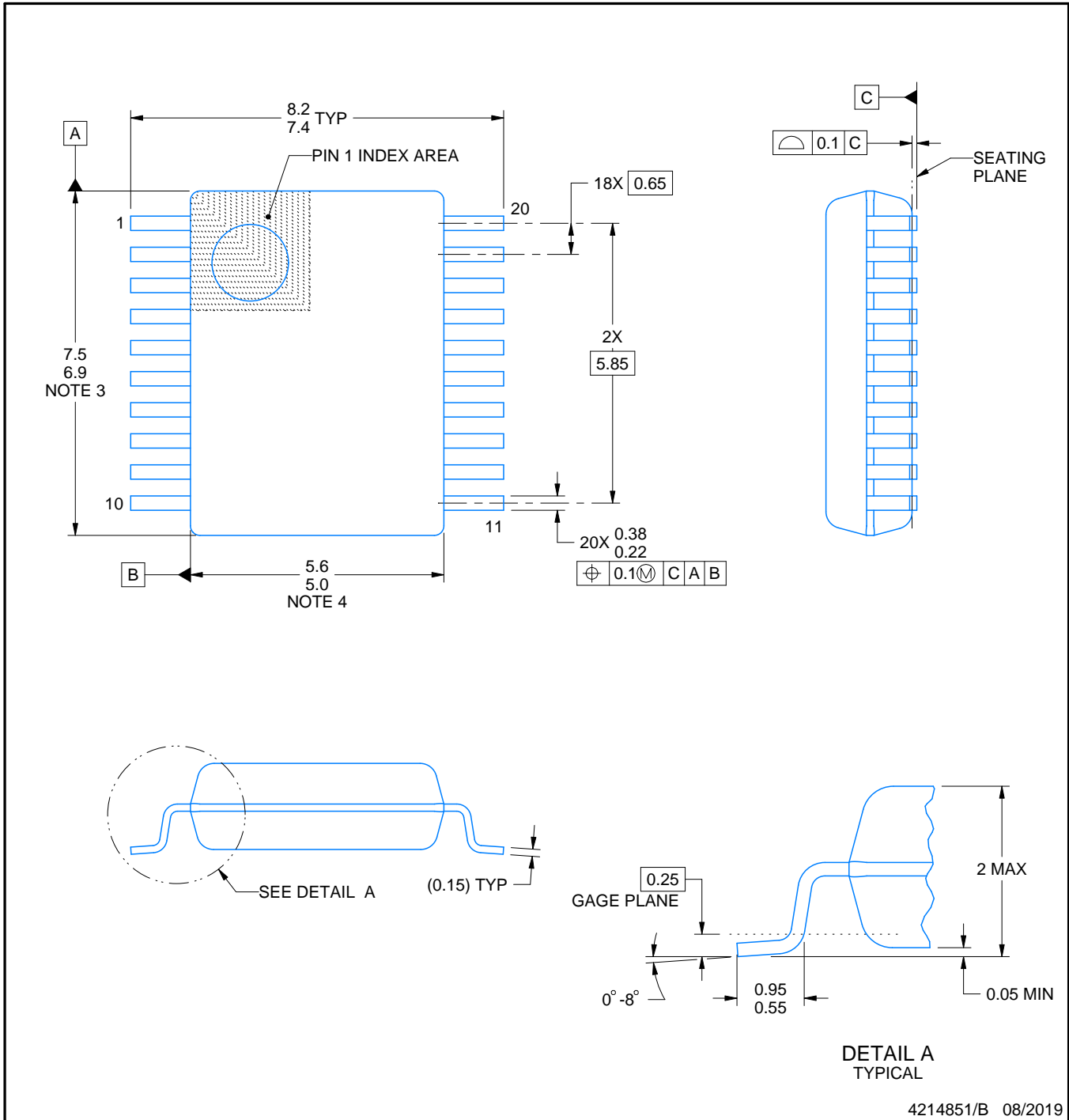
# DB0020A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214851/B 08/2019

# EXAMPLE BOARD LAYOUT

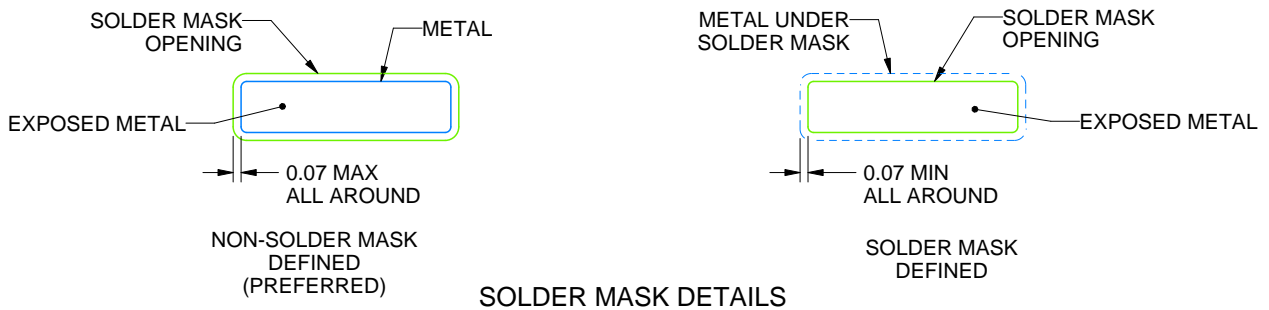
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4214851/B 08/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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