bq50002A 适用于 WPC v1.2 A11 发送器的低成本 5V 无线电源发送器模拟前端

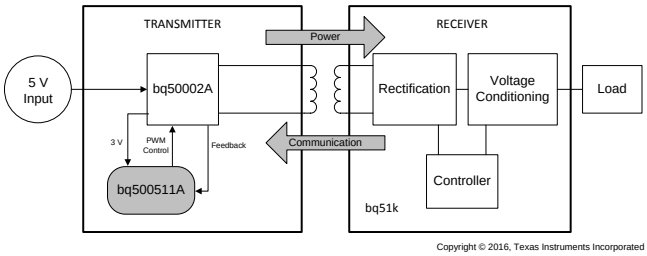
1 特性

- 符合无线充电联盟 (WPC) v1.2 A11 低功耗发送器规范的 5V 发送器模拟前端 (AFE)
- 专为与 bq500511A WPC 控制器搭配使用而设计
  - 注：如果需要进行外来物体检测，则 bq50002A 与 bq500511 器件不兼容。
- 适用于 WPC 和 5V 专用无线电源发送器
- 支持 5W 的接收器输出功率
- 在无线电源发送器中集成了所需的全部模拟功能
  - 金属氧化物半导体场效应晶体管 (MOSFET) 驱动器和同步 N 沟道功率场效应晶体管 (FET)
  - 精确的电流感测
  - 变频振荡器
  - 高效稳压器
  - 用于对接收器信号进行解码的高灵敏度解调器
- 双芯片解决方案实现了效率超过 75% 的高效发送器设计
- 超低待机功耗，即使在数字 Ping 过程中也可实现 (< 30mW)
- 动态电源限制 (DPL)™通过功率受限的输入源实现正常运行
- 系统发光二极管 (LED) 指示充电状态和故障状态
- 精准的外来物体检测 (FOD) 方法

2 应用

- 适用于智能手机和可穿戴应用且符合 WPC 标准的无线 发送器
- 专用无线充电器和发射器
- 医疗和可穿戴 应用

简化电路原理图



3 说明

bq50002A 器件是一款高度集成的无线电源发送器模拟前端 (AFE)，其中包含实现符合无线充电联盟 (WPC) 标准的 5V 发送器所需的全部模拟组件。bq50002A 器件将全桥电源驱动器与 MOSFET、变频振荡器、双通道通信解调器、线性稳压器以及保护电路相集成。bq50002A 器件必须与数字控制器 bq500511A 一起搭配使用，以实现紧凑型双芯片无线电源发送器解决方案。bq500511A 可安全接合 Rx 器件、接收充电器件传输的通信数据包以及根据 WPC v1.2 规范管理功率传输。

该系统支持外来物体检测 (FOD)，具体方法是通过持续监视传输功率并将功率值与接收器报告的接收功率相比较。该功能可防止因在无线电源传输场中错误放置金属物体而产生功率损耗。为此，bq50002A 使用电流感测放大器对输入直流电流进行精确测量。如果在功率传输过程中出现任何异常情况，bq500511A 会对其进行处理并提供指示输出。综合状态和故障监视 特性 可实现一个经 WPC 认证的低成本、稳健耐用的无线电源系统设计。

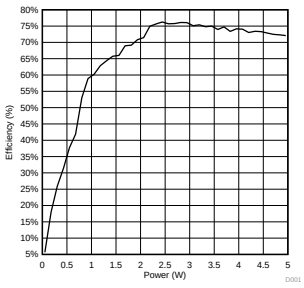
bq50002A 采用 5.00mm × 5.00mm 32 引脚散热增强型四方扁平无引线 (QFN) 封装。

器件信息 (1)

部件号	封装	封装尺寸（标称值）
bq50002A	QFN (32)	5.00mm x 5.00mm

(1) 要了解所有可用封装，请见数据表末尾的可订购产品附录。

效率与功率间的关系



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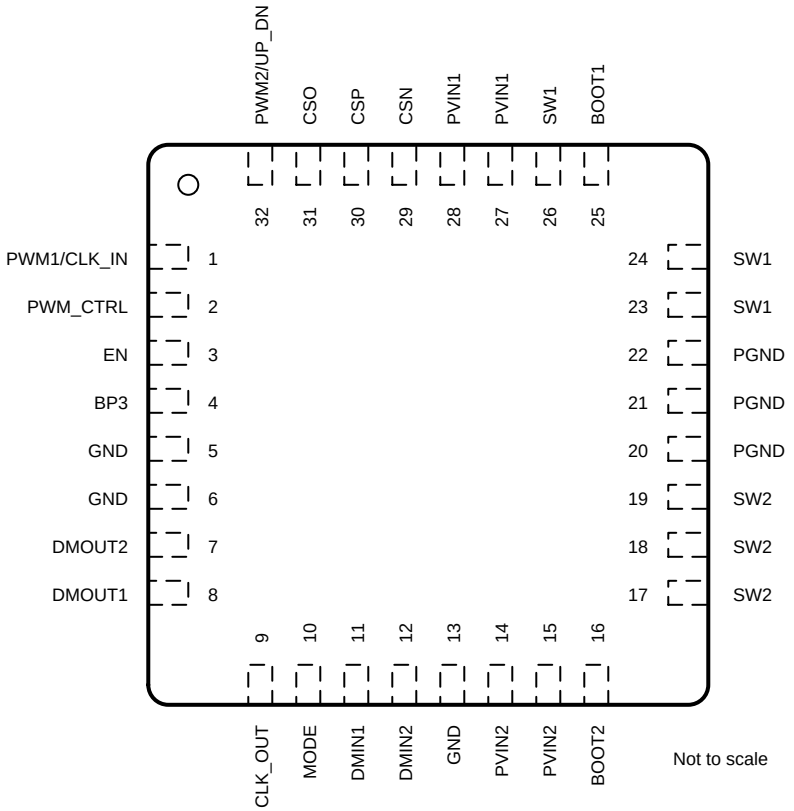
4 修订历史记录

日期	修订版本	注释
2016 年 8 月	A	最初发布。

5 Pin Configuration and Functions

RHB Package
32-Pin QFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
BOOT1	25	I/O	Positive supply rail for the high-side gate driver. Connect a 0.1-µF ceramic capacitor between the BOOT1 and SW1 pins.
BOOT2	16	I/O	Positive supply rail for the high-side gate driver. Connect a 0.1-µF ceramic capacitor between the BOOT2 and SW2 pins.
BP3	4	O	LDO output. Tie with 2.2-µF capacitor to GND. For use by bq500511A only.
CLK_OUT	9	O	Internal oscillator clock out signal.
CSN	29	I	Current sense amplifier negative input.
CSO	31	O	Current sense amplifier output. For use by bq500511A only.
CSP	30	I	Current sense amplifier positive input. Connect current sense resistor as close as possible to this pin. This also serves as the quiet node for power supply input.
DMIN1	11	I	Modulated signal from coil for DEMOD CHAN1.
DMIN2	12	I	Modulated signal from coil for DEMOD CHAN2.
DMOUT1	8	O	Demodulated 2-kHz signal from CHAN1. For use by bq500511A only.
DMOUT2	7	O	Demodulated 2-kHz signal from CHAN2. For use by bq500511A only.
EN	3	I	Enable pin with a weak internal pull-down. Float or pull below 1.5 V to disable gate driver, demodulation and current sense. Pull above 2.2 V to enable gate driver. Used by bq500511A to enter and leave standby mode for the transmitter.
GND	5	–	Signal ground for the ground-referenced logic. All signal level circuits should be referenced to this pin unless otherwise noted.
GND	6	–	Signal ground for the ground-referenced logic. All signal level circuits should be referenced to this pin unless otherwise noted.
GND	13	–	Signal ground for the ground-referenced logic. All signal level circuits should be referenced to this pin unless otherwise noted.
MODE	10	I	MODE pin with a weak internal pull-down. Float, or pull below 1.5 V to enable frequency control of the internally generated PWM signal. Pull above 2.2 V to enable pulse width control of the internally generated PWM signal. Used by bq500511A to select the control method for power control
PGND	20	–	Power ground for the ground-referenced power stage. Connect to GND.
PGND	21	–	Power ground for the ground-referenced power stage. Connect to GND.
PGND	22	–	Power ground for the ground-referenced power stage. Connect to GND.
PVIN1	27	I	DC input voltage for half-bridge MOSFET. Bypass with 22-µF ceramic capacitor to GND.
PVIN1	28	I	DC input voltage for half-bridge MOSFET. Bypass with 22-µF ceramic capacitor to GND.
PVIN2	14	I	DC input voltage for half-bridge MOSFET. Bypass with 22-µF ceramic capacitor to GND.
PVIN2	15	I	DC input voltage for half-bridge MOSFET. Bypass with 22-µF ceramic capacitor to GND.
PWM_CTRL	2	I	PWM_CTRL pin with a weak internal pull-down. Controlled by bq500511A (SLUSCN3) for system power delivery control.
PWM1/CLK_IN	1	I	PWM1/CLK_IN pin with a weak internal pull-down. Controlled by bq500511A (SLUSCN3) for system power delivery control.
PWM2/UP_DN	32	I	PWM2/UP_DN pin with a weak internal pull-down. Controlled by bq500511A (SLUSCN3) for system power delivery control.
SW1	23	O	Switch node of the half-bridge MOSFETs. Connect to TX coil.
SW1	24	O	Switch node of the half-bridge MOSFETs. Connect to TX coil.
SW1	26	O	Switch node of the half-bridge MOSFETs. Connect to TX coil.
SW2	17	O	Switch node of the half-bridge MOSFETs. Connect to resonant capacitor.
SW2	18	O	Switch node of the half-bridge MOSFETs. Connect to resonant capacitor.
SW2	19	O	Switch node of the half-bridge MOSFETs. Connect to resonant capacitor.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
PVIN1, PVIN2	–0.3	7	V
BOOT1 (2)	–0.3	14	V
VBOOT1 – VSW1	–0.3	7	V
BOOT2 (2)	–0.3	14	V
VBOOT2 – VSW2	–0.3	7	V
PWM1, PWM2, EN, CLK_OUT, MODE, PWM_CTRL	–0.3	3.6	V
DMIN1	–5	7	V
DMIN2	–0.3	7	V
CSN, CSP	–0.3	7	V
CSN to CSP	-0.5	0.5	V
Operating junction temperature, T_J	–40	125	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) In normal use, BOOT1, BOOT2 voltage internally regulated.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
	PVIN1, PVIN2	4.5	5	5.5	V
	PWM1, PWM2, EN, CLK_OUT, MODE, PWM_CTRL	0	3	3.3	V
	DMIN1	–0.3		5	V
	DMIN2	–0.3		5	V
C_{BP3}	BP3 ceramic capacitor		2.2		µF
C_{PVIN1}, C_{PVIN2}	PVIN1, PVIN2 ceramic capacitor		0.1		µF
C_{PVIN1}, C_{PVIN2}	PVIN1, PVIN2 electrolytic capacitor		22		µF
C_{BOOT1}, C_{BOOT2}	SW1-BOOT1, SW2-BOOT2 capacitor		0.1		µF

6.4 Thermal Information

THERMAL METRIC (1)		bq50002A RHB (QFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	13.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	13	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	5.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

–40°C ≤ T_J ≤ +125°C, V_{PVIN1} = 5 V, V_{PVIN2} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE (VIN)					
UVLO rising threshold	V_{IN} rising	3.75	3.9	4.2	V
UVLO falling threshold	V_{IN} falling	3.6	3.85	4.08	V
REGULATOR VOLTAGE (BP3)					
BP3 output voltage	I_{BP3} = –5 mA, V_{PVIN1} = V_{PVIN2} = 5 V	2.9	3	3.1	V
BP3 output voltage	I_{BP3} = –10 mA, V_{PVIN1} = V_{PVIN2} = 5 V	2.9	3	3.1	V
BP3 load current max	V_{BP3} = 2.7 V, V_{PVIN1} = V_{PVIN2} = 5 V	7.7	14	21	mA
CURRENT SENSE AMPLIFIER (CSP, CSN)					
Current sense amplifier gain	0°C < T_J < 85°C		50		V/V
Input current (CSP)	V_{CSP} = 5 V, V_{PVIN1} = V_{PVIN2} = 5 V		1.5		mA
Input current (CSN)	V_{CSN} = 5 V, V_{PVIN1} = V_{PVIN2} = 5 V	8.5	10	11.3	µA
EN					
High-level input voltage	Input rising	1.7	1.8	1.9	V
Low-level input voltage	Input falling	0.8	1	1.1	V
EN pull-down resistance	EN = 3 V	40	50	60	kΩ
PWM_CTRL					
High-level input voltage	Input rising	1.4	1.6	1.8	V
Low-level input voltage	Input falling	0.9	1	1.1	V
PWM_CTRL pull-down resistance	PWM_CTRL = 3 V	40	50	60	kΩ

Electrical Characteristics (continued)

–40°C ≤ T_J ≤ +125°C, V_{PVIN1} = 5 V, V_{PVIN2} = 5 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PWM1					
High-level input voltage	Input rising	1.6	1.8	1.9	V
Low-level input voltage	Input falling	0.9	1	1.1	V
PWM1 pull-down resistance	PWM1 = 3 V	40	50	60	kΩ
PWM2					
High-level input voltage	Input rising	1.6	1.7	1.8	V
Low-level input voltage	Input falling	1	1.1	1.2	V
PWM2 pull-down resistance	PWM2 = 3 V	40	50	60	kΩ
MODE					
High-level input voltage	Input rising	1.7	1.8	1.9	V
Low-level input voltage	Input falling	0.9	1	1.1	V
MODE pull-down resistance	MODE = 3 V	40	50	60	kΩ
BOOTSTRAP DIODE (BOOT1 AND BOOT2)					
Regulation voltage (BOOT1)	V_{PVIN1} = V_{PVIN2} = 5 V, I_{BOOT} = 0 mA	4.2	4.4	4.7	V
Regulation voltage (BOOT2)	V_{PVIN1} = V_{PVIN2} = 5 V, I_{BOOT} = 0 mA	4.9	5	5.1	V
UVLO (BOOT1)	V_{PVIN1} = V_{PVIN2} = 5 V	1.8	2.3	2.7	V
UVLO (BOOT2)	V_{PVIN1} = V_{PVIN2} = 5 V	1.8	2.2	2.6	V
MOSFETS (SW1 AND SW2)					
SW1 high-side $R_{DS(on)}$	V_{PVIN1} = V_{PVIN2} = 5 V	59	76	107	mΩ
SW1 low-side $R_{DS(on)}$	V_{PVIN1} = V_{PVIN2} = 5 V	48	61	86	mΩ
SW2 high-side $R_{DS(on)}$	V_{PVIN1} = V_{PVIN2} = 5 V	42	49	64	mΩ
SW2 low-side $R_{DS(on)}$	V_{PVIN1} = V_{PVIN2} = 5 V, I_{SW} = 500 mA	39	46	58	mΩ

6.6 Typical Characteristics

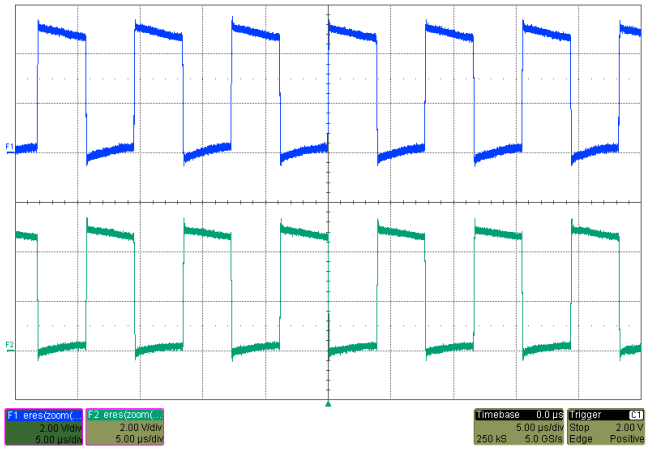


Figure 1. bq50002A SW1, SW2

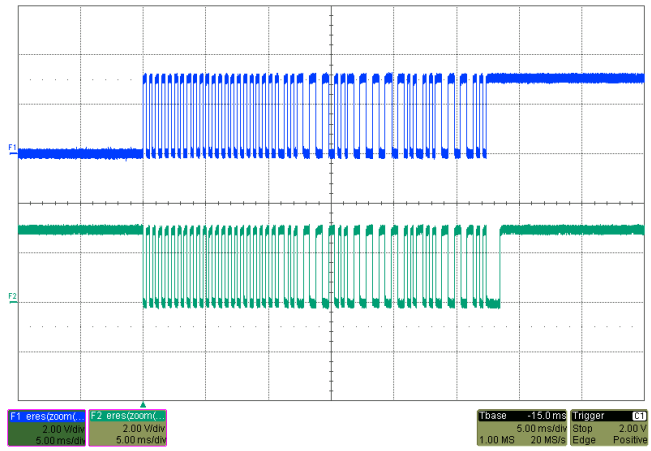


Figure 2. DMOUT1, DMOUT2

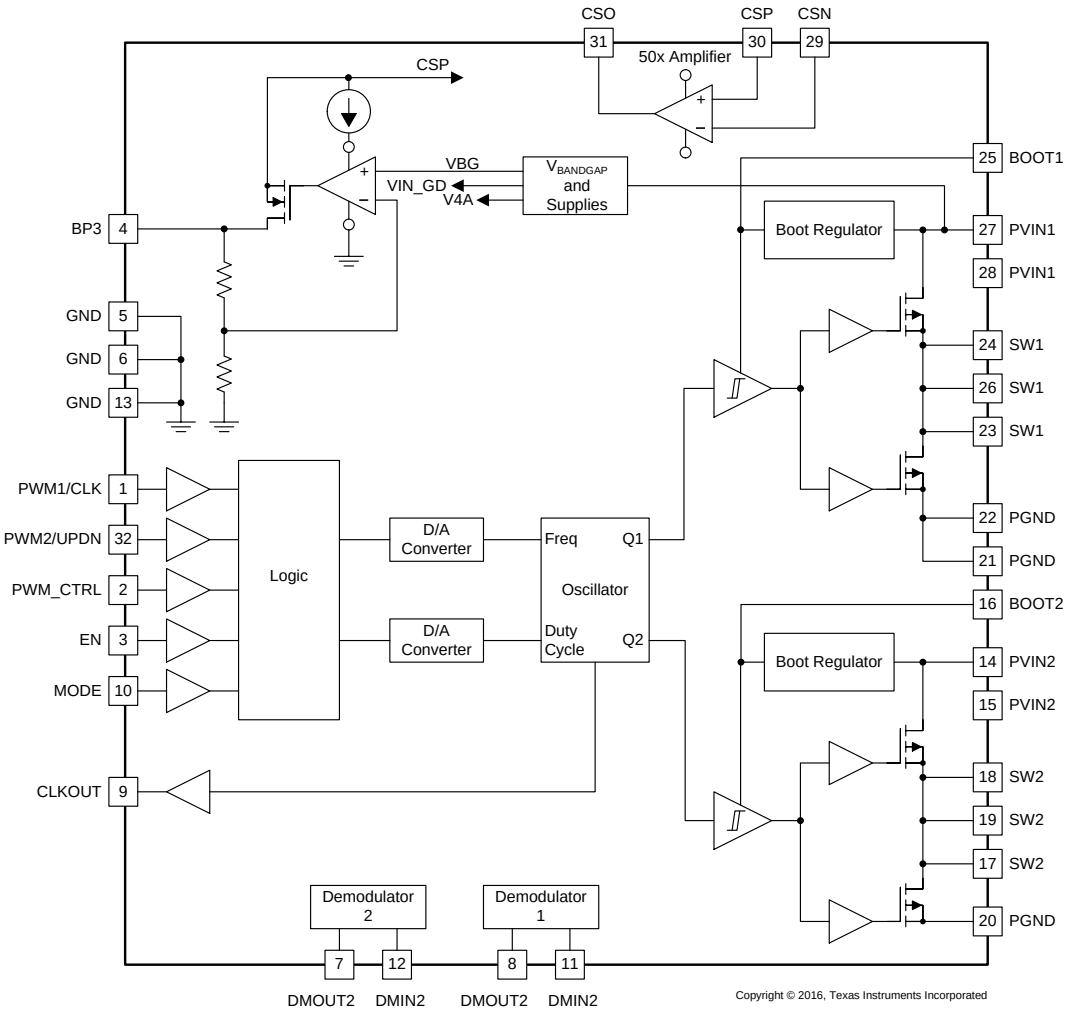
7 Detailed Description

7.1 Overview

The principle of wireless power transfer is simply an open-cored transformer consisting of transmitter and receiver coils. The transmitter coil and electronics are typically built into a charger pad and the receiver coil and electronics are typically built into a portable device, such as a smart phone. When the receiver coil is positioned on the transmitter coil, magnetic coupling occurs when the transmitter coil is driven. The flux is coupled into the secondary coil, which induces a voltage and current flows. The secondary voltage is rectified, and power can be transferred effectively to a load, wirelessly. Power transfer can be managed through various closed loop control schemes.

After power is applied and the transmitter device comes out of reset, the process of detecting and powering a receiver automatically begins. The bq500511A sends a ping to detect the presence of a receiver on the pad. After a receiver is detected, the bq500511A attempts to establish communication and begin power transfer. The bq500511A is designed to operate with the bq50002A Wireless Power Transmitter Analog Front End to control a full-bridge power stage to drive the primary coil. Through a simple interface the bq500511A instructs the bq50002A how much to increase or decrease power. The full bridge power stage allows for higher power delivery for a given supply voltage.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Demodulator

The embedded demodulator outputs at least one valid bit stream under all modulation conditions that can be used by the accompanied bq500511A controller in order to comply with WPC specification.

More specifically, the WPC worst case condition is defined as the transmitter operating at the minimum modulation level, and the receiver coil is measured by certain x, y and z axis distance to the center of the transmitter coil.

Analog demodulation channel function diagram:

- The diagram below from the WPC spec document explains the concept of Minimum Modulation. The peak-to-peak amplitude difference in TX coil waveform between HI and LO states is 400 mV. With 20-V_{pp} carrier waveform, and 400-mV_{pp} modulation, with a typical divider it translates to 1 V_{pp} ±20 mV_{pp} at the input of the demodulator channel.
- The difference of the amplitude of the primary cell voltage in the HI and LO state is at least 200 mV.

During a transition the primary cell current and primary cell voltages are undefined. See Figure 3.

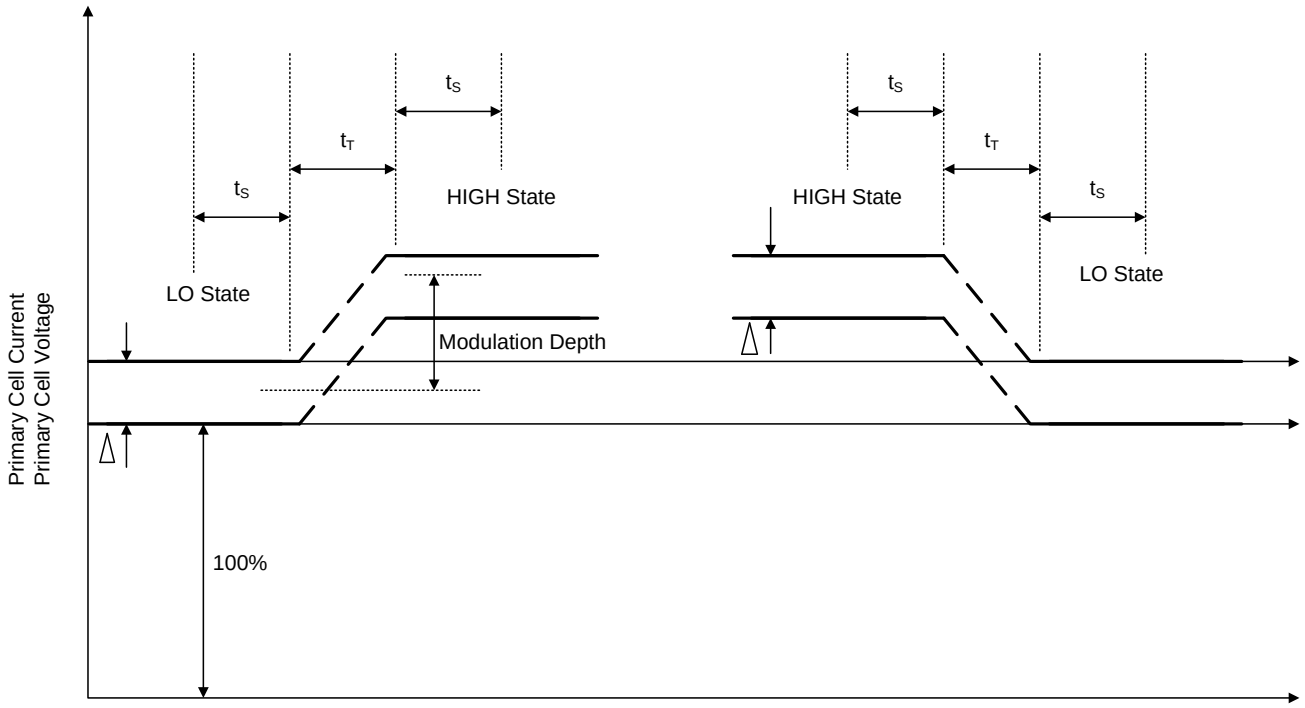


Figure 3. Amplitude Modulation of the Power Signal

Feature Description (continued)

7.3.2 PWM Control

7.3.2.1 PWM_CTRL Input

The bq50002A device operates in two modes:

Direct PWM Control Mode and Self Switching. The mode of operation is set by the state of PWM_CTRL input when EN=HIGH. This is intended for control by bq500511A.

7.3.2.2 PWM1, PWM2

bq50002A passes external PWM inputs to drive gate drivers when the following conditions hold:

- EN pin is HIGH
- PWM_CTRL pin is HIGH
- Typical Dead Time shall be better than 20 ns. Minimum PWM input pulse duration that changes SW output should be less than 50 ns.

7.3.2.3 Self-Switching

bq50002A follows the commands from the controller to adjust the internal oscillator frequency up or down to adjust output power levels when the following conditions apply:

- PWM_CTRL pin is LOW
- PWM1/CLK_IN behaves as CLK_IN pin. The CLK_IN rising edge triggers frequency increase or decrease by one step based on the state of PWM2/UP_DN pin.
- Self-switching starts at F=175 kHz when PWM_CTRL state changes from HIGH to LOW. Operating frequency changes are based on the inputs of UP_DN, CLK_IN and MODE.
- The CLK_OUT pin outputs 3.3V logic level with frequency equal in value to the current switching frequency. The rising edge of this signal coincides with the rising edge of the SW1 waveform. The duty factor of the signal on CLK_OUT pin is 50%.
- bq50002A increases the frequency (reduces delivered power) if:
  - PWM_CTRL pin is LOW
  - MODE pin is LOW
  - UP_DN pin is LOW
  - CLK_IN pin changes its state from LOW to HIGH (rising edge)
- bq50002A decreases the frequency (increases delivered power) if:
  - PWM_CTRL pin is LOW
  - MODE pin is LOW
  - UP_DN pin is HIGH
  - CLK_IN pin changes its state from LOW to HIGH (rising edge)

Feature Description (continued)

7.3.2.4 Duty Cycle Adjustment

bq50002A follows the commands from the controller to adjust the internal oscillator duty cycle up or down to adjust power output levels when the following conditions hold:

- The internal clock is set to the highest frequency tap, 205 kHz
- PWM_CTRL pin is LOW
- MODE pin is HIGH
- bq50002A decreases the duty cycle (reduces delivered power) if:
  - The internal clock is set to the highest frequency tap, 205 kHz or at frequency at which MCU commands MODE = 1
  - PWM_CTRL pin is LOW
  - MODE pin is HIGH
  - UP_DN is LOW
  - CLK_IN pin changes state from LOW to HIGH (rising edge)
  - bq50002A ignores CLK_IN signals when minimum duty factor position of 10% is reached
- bq50002A increases the duty cycle (increases delivered power) if:
  - The internal clock is set to the highest frequency tap, 205 kHz at frequency at which MCU commands MODE = 1
  - PWM_CTRL pin is LOW
  - MODE pin is HIGH
  - UP_DN is HIGH
  - CLK_IN pin changes state from LOW to HIGH (rising edge)
  - bq50002A ignores CLK_IN signals when maximum duty factor position of 50% is reached. bq50002A will resume clock frequency adjustment mode only when the duty cycle adjustment has reached the 50% state and MODE=0.

7.3.3 Current Sense Amplifier

To support foreign object detection (FOD), the bq50002A senses the average input current to the device. The integrated current sense amplifier has voltage gain of 50. When paired with the bq500511A the offset in the bq50002A current sense amplifier is dynamically compensated, which allows accurate FOD performance.

7.3.4 Voltage Regulator

The bq50002A device has an integrated low-dropout (LDO) voltage regulator which supplies power to the companion bq500511A controller. The BP3 pin supplies a regulated 3-V voltage supply and should have a 2.2-µF capacitor tied to GND.

7.4 Device Functional Modes

7.4.1 Power Transfer

Power transfer efficiency and robustness depends on coil coupling. Coupling depends on the distance between coils, alignment, coil dimensions, coil materials, number of turns, magnetic shielding, impedance matching, frequency. Most importantly, the receiver and transmitter coils must be aligned for best coupling and efficient power transfer. The smaller the space between the coils is, the better the coupling. Shielding is added as a backing to both the transmitter and receiver coils to direct the magnetic field to the coupled zone. Magnetic fields outside the coupled zone do not transfer power. Thus, shielding also serves to contain the fields to avoid coupling to other adjacent system components.

Regulation can be achieved by controlling any one of the coil coupling parameters. However, for WPC compatibility, the transmitter-side coils and capacitance are specified and the resonant frequency point is fixed. In the bq500511A or bq50002A system power transfer is regulated by changing the operating frequency between 110 kHz to 205 kHz. The higher the frequency, the further from resonance and the lower the power. Duty cycle remains constant at 50% throughout the power band and is reduced only once 205 kHz is reached.

7.4.1.1 Dynamic Power Limiting™

Dynamic Power Limiting™ (DPL) allows operation from a 5-V supply with limited current capability (such as a USB port). When the input voltage is observed drooping, the output power is dynamically limited to reduce the load and provides margin relative to the supply's capability.

Anytime the DPL control loop is regulating the operating point of the transmitter, the LED will indicate that DPL is active. The LED color and flashing pattern are determined by the LED Table. If the receiver sends a Control Error Packet (CEP) with a negative value, (for example, to reduce power to the load), the bq500511A in DPL mode will return to normal operation and respond to this CEP through the standard WPC control loop behavior.

Device Functional Modes (continued)

7.4.2 Communication

Communication within the WPC v1.2 specification is from the receiver to the transmitter. For example, in order to regulate the output of the transmitter, the receiver sends messages requesting the transmitter to increase or decrease power. The receiver communicates by modulating the rectifier voltage and using amplitude modulation (AM) sends packets of information to the transmitter. A packet is comprised of a preamble, a header, the actual message, and a checksum, as defined by the WPC standard.

The receiver sends a packet by modulating an impedance network. This AM signal reflects back as a change in the voltage amplitude on the transmitter coil. In the bq500511A or bq50002A system, the bq50002A performs the demodulation function and passes a digitized version of the message to the bq500511 where the message is decoded and processed. For example in response to a Control Error Packet, the bq500511A calculates the required change in output power and in turn controls the bq50002A through the CLK_OUT, UP_DOWN, and MODE pins to adjust the operating point and thus its output power.

The modulation impedance network on the receiver can either be resistive or capacitive. Figure 4 shows the resistive modulation approach, where a resistor is periodically added to the load, resulting in an amplitude change in the transmitter voltage. Figure 5 shows the corresponding capacitive modulation approach.

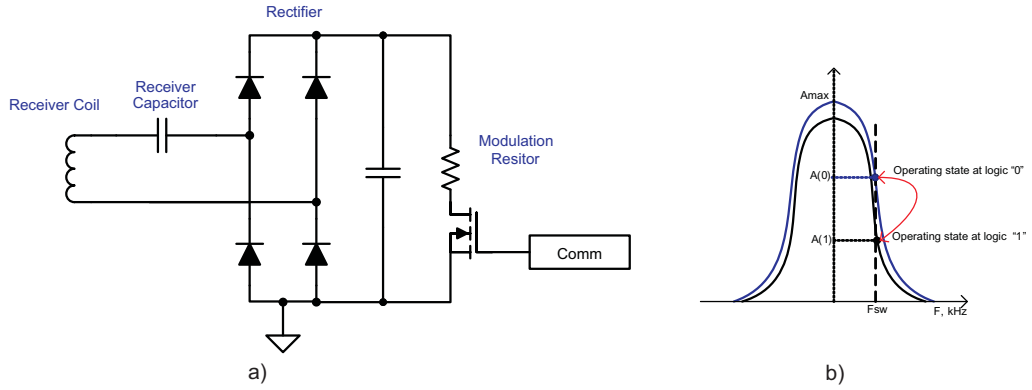


Figure 4. Receiver Resistive Modulation Circuit

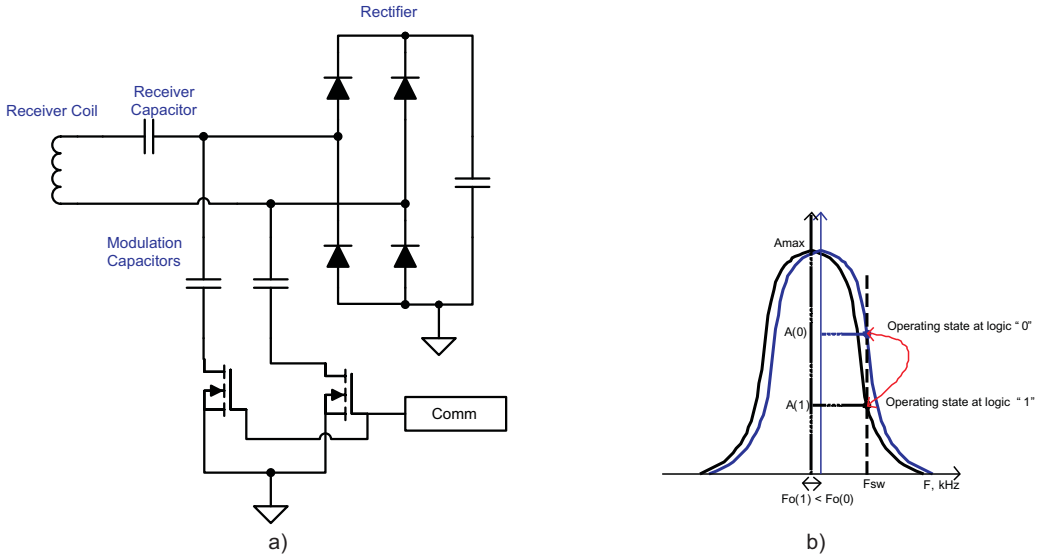


Figure 5. Receiver Capacitive Modulation Circuit

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The bq50002A device is a wireless power transmitter AFE designed for 5-W WPC compliant applications when paired with the bq500511A. The pair integrates all functions required to control wireless power transfer to a WPC v1.2 compliant receiver. Several tools are available for the design of the system. See the product folder on www.ti.com for more details. The following sections highlight some of the system design considerations.

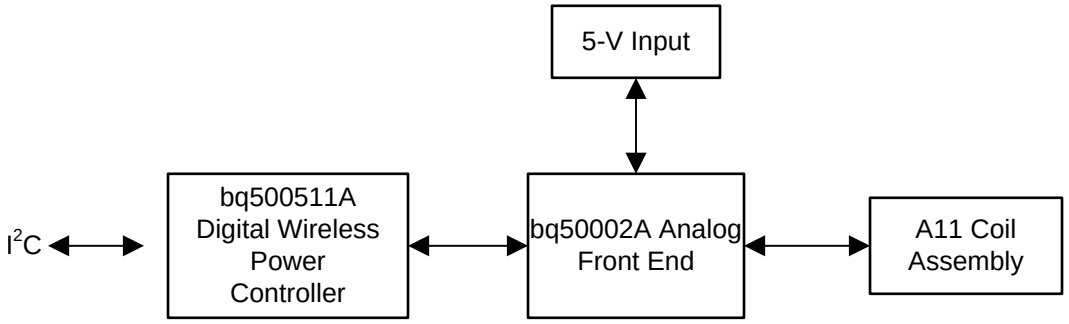


Figure 6. System Block Diagram

The I^2C port is accessed by the FOD tuning tool and can provide a level of system monitoring and evaluation.

The SDA and SCL lines of the I^2C bus must be pulled up (as shown in the) if the I^2C port is utilized. They may be left floating if no I^2C function is required. The logic reference generated by the bq50002A Analog Front End is 3 V, so care should be taken to ensure that if the Master I^2C device also has pull-up resistors to a higher reference, that the the 3-V reference to the bq500511A is not affected. Specifically, only one set of pull-up resistors should be populated, either on the I^2C Master bus or on the bq500511A system board, but not both.

8.2 Typical Application

The bq50002A is a highly integrated analog front end device which, when paired with the bq500511A controller, requires a minimum of external components to implement a WPC V 1.2 Wireless Power Transmitter system.

As shown in the application schematic, external components are used to implement the following functions:

- Resonant Tank Circuit
- Demodulator Input Signal Conditioning
- Human Interface (LED and Buzzer)
- Current Sensing
- Voltage Sensing
- Temperature Sensing
- System Configuration
  - Foreign Objection Detection (FOD) Threshold and Calibration
  - LED Mode

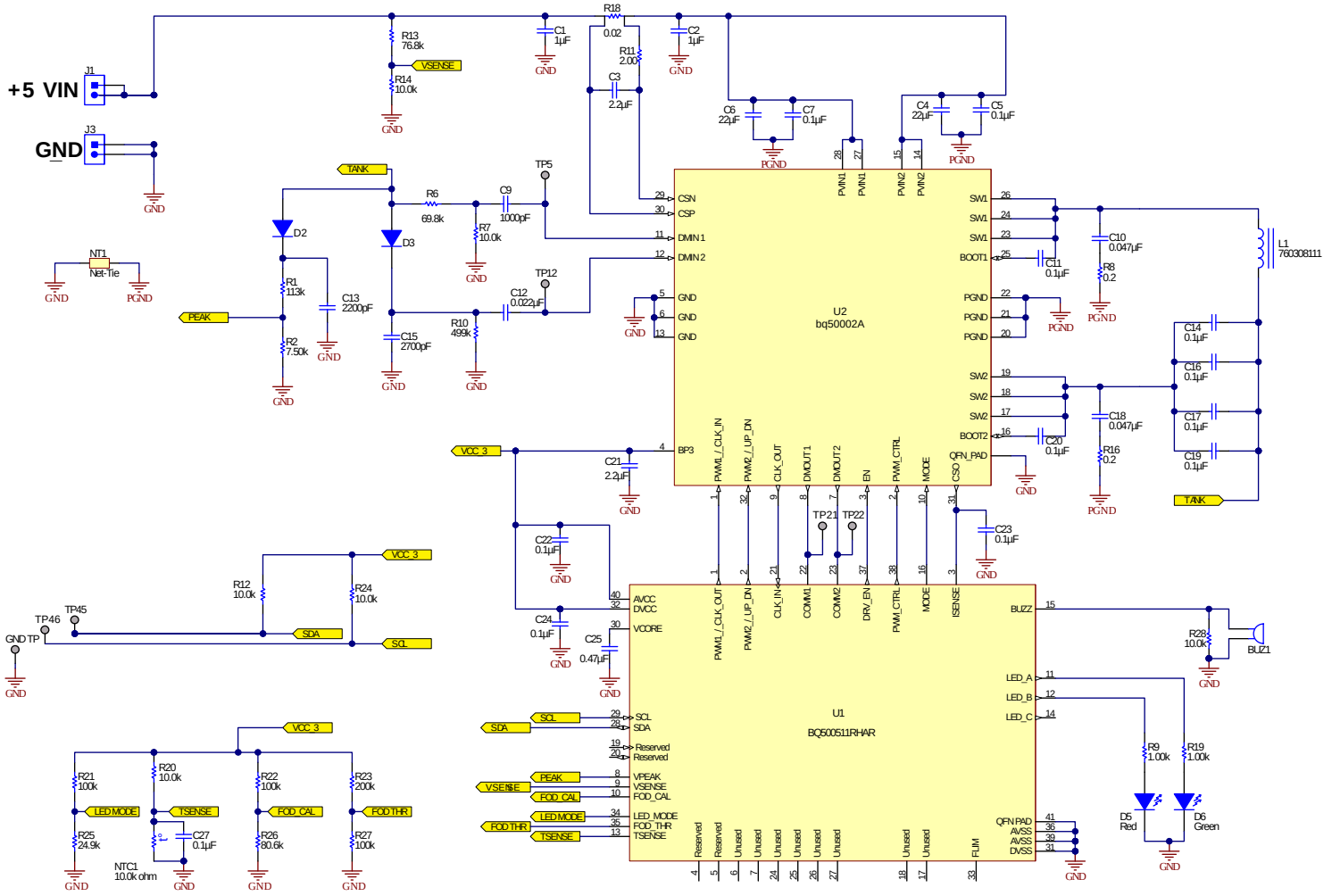


Figure 7. bq500511A Application Schematic

8.2.1 Design Requirements

For this design example, use the parameter listed in Table 1 as the input parameter.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
WPC coil type	A11

8.2.2 Detailed Design Procedure

8.2.2.1 Capacitor Selection

Capacitor selection is critical to proper system operation. The total capacitance value of 4 nF × 100 nF is required in the resonant tank. This is the WPC system compatibility requirement, not a guideline.

NOTE

A total capacitance value of 4 nF × 100 nF (C0G dielectric type, 50-V rating) is required in the resonant tank to achieve the correct resonance frequency. The capacitors chosen must be rated for at least 50 V and must be of a high-quality C0G dielectric (sometimes also called NP0). These are typically available in a 5% tolerance, which is adequate. TI does **not** recommend the use of X7R types or below if WPC compliance is required because critical WPC Certification Testing, such as the minimum modulation or guaranteed power test, might fail. The designer can combine capacitors to achieve the desired capacitance value. Various combinations can work depending on market availability. All capacitors must be of C0G types (not mixed with any other dielectric types).

8.2.2.2 Current Monitoring Requirements

The bq50002A is WPC v1.2 ready. To enable the FOD feature, current monitoring is provided in the bq50002A Analog Front End. For proper scaling of the current monitor signal, the current sense resistor should be 20 mΩ. For FOD accuracy, the current sense resistor must be a quality component with 0.5% tolerance, at least 1/4-W rating, and a temperature stability of ±200 PPM.

8.2.2.3 Input Regulation

The bq500511A requires 3 VDC to operate. The regulator in the bq50002A provides this voltage rail eliminating the need for any external regulation.

8.2.2.4 System Input Power Requirements

The design works with 5-V input voltage to the bq50002A. The WPC defined A11 TX type requires 5-V system voltage in order to deliver 5 W of output power from the receiver.

8.2.3 Application Curves

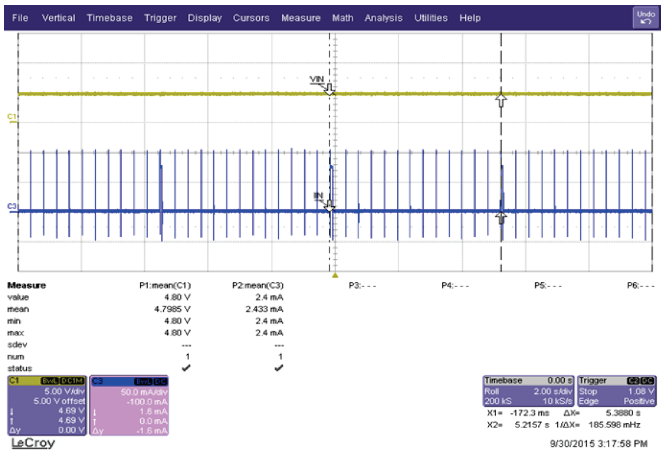


Figure 8. Standby Power

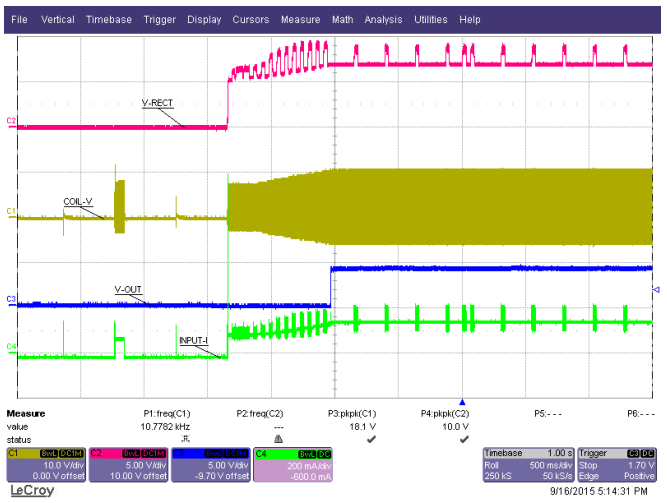


Figure 9. Start-Up with bq51013B

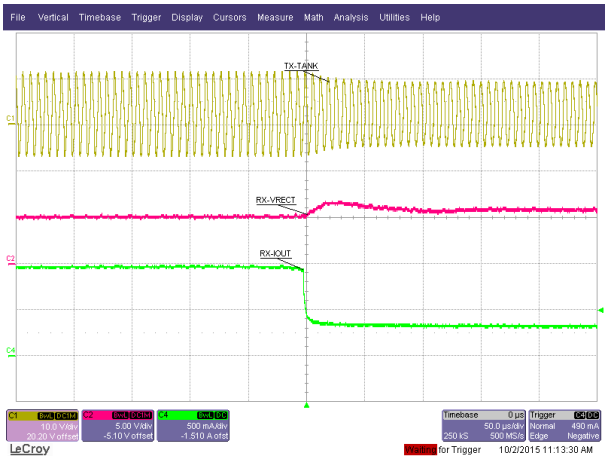


Figure 10. Load-Transient Response

9 Power Supply Recommendations

The A11 TX type requires a 5-V system voltage.

10 Layout

10.1 Layout Guidelines

Careful PCB layout practice is critical to proper system operation. Many references are available on proper PCB layout techniques. A few good tips are as follows.

The TX layout requires a 4-layer PCB layout for best ground plane technique. A 2-layer PCB layout can be achieved though not as easily. Ideally, the approach to the layer stack-up is:

- Layer 1 component placement and as much ground plane as possible
- Layer 2 clean ground
- Layer 3 finish routing
- Layer 4 clean ground

Thus, the circuitry is virtually sandwiched between grounds. This minimizes EMI noise emissions and also provides a noise-free voltage reference plane for device operation.

Keep as much copper as possible. Make sure the bq500511A GND pins have a continuous flood connection to the ground plane. The power pad of the bq50002A should also be stitched to the ground plane, which also acts as a heat sink. A good GND reference is necessary for proper system operation, such as analog-digital conversion, clock stability, and best overall EMI performance. Separate the analog ground plane from the power ground plane and use only **one** tie point to connect grounds. Having several tie points defeats the purpose of separating the grounds. See the bq50002 EVM, SLVUAJ7, for an example of a good layout technique.

10.1.1 Layout Notes

Make sure the bypass capacitors intended for the bq500511A 3.3-V supply are actually bypassing these supply pins (pin 32, DVCC, and pin 40, AVCC) to solid ground plane (see Figure 11). This means they need to be placed as close to the device as possible and the traces must be as wide as possible.

Make sure the bq500511A has a continuous flood connection to the ground plane (see Figure 12).

The full-bridge power stage that drives the TX coil is composed of two half-bridge power stages (integrated in bq50002A) and resonant capacitors. Inputs bypass capacitors should be placed as close as possible to the bq50002A PVIN1 pins (pin 27, 28) and PVIN2 pins (pin 14, 15). The input and ground pours and traces should be made as wide as possible for better current flow. The trace to the coil and resonant capacitors should also be made as wide as possible (see Figure 13).

To ensure proper operation, grounds conducting a large amount of current and switching noise must be isolated from low current, quiet grounds. Separate the ground pours for the power stages and the bq500511A IC. Connect all grounds to a single point at the main ground terminal (see Figure 13).

Proper current sensing layout technique is very important, as it directly affects the FOD and PMOD performance. When sampling the very-low voltages generated across a current sense resistor, be sure to use the so called 4-wire or Kelvin-connection technique. This is important to avoid introducing false voltage drops from adjacent pads and copper power routes. It is a common power-supply layout technique. Some high-accuracy sense resistors have dedicated sense pins (see Figure 15).

The trace from bq50002A CSP pin to sense resistor must be minimized to avoid unwanted offset in the application. This trace should be limited to less than 20 mΩ resistance.

10.2 Layout Examples

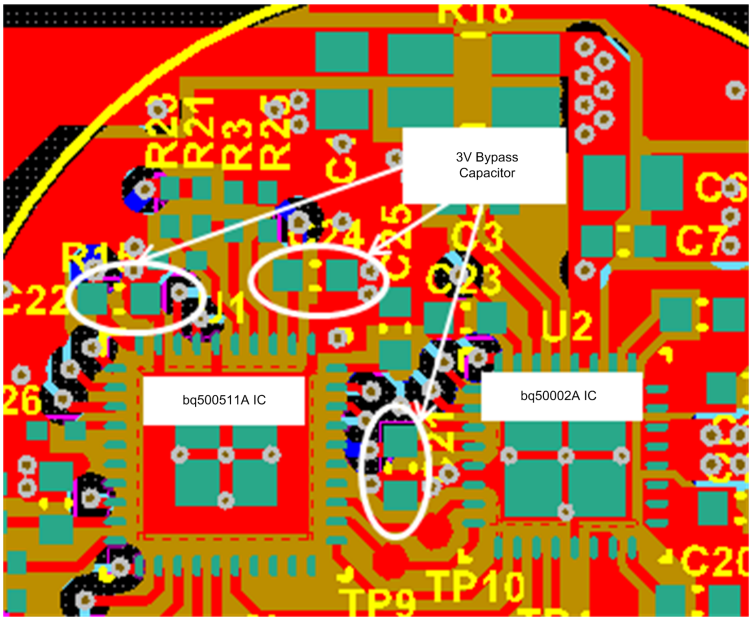


Figure 11. Bypass Capacitors Layout

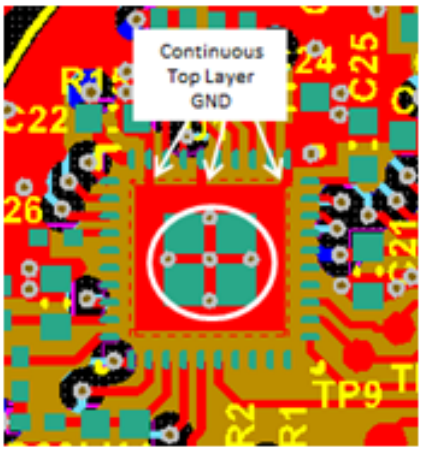


Figure 12. Continuous GND Layout

Layout Examples (continued)

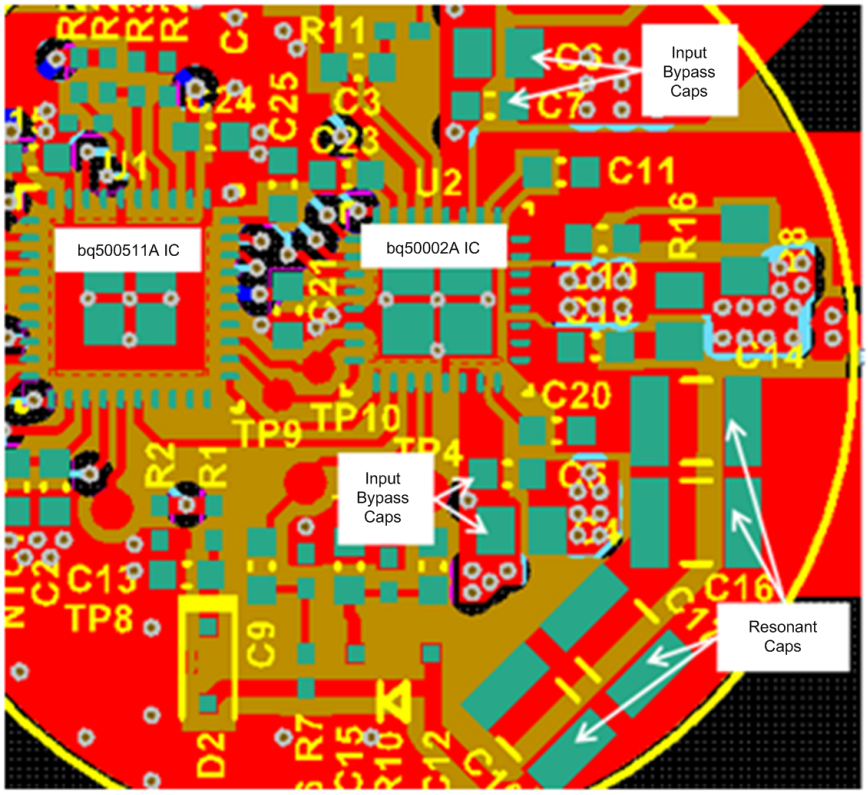


Figure 13. Ground Layout

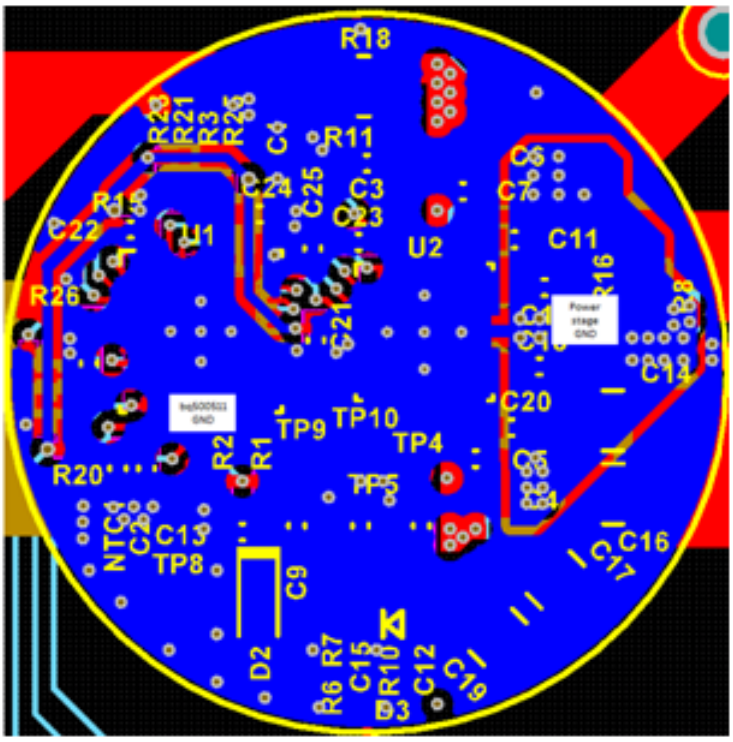


Figure 14. Ground Layout

Layout Examples (continued)

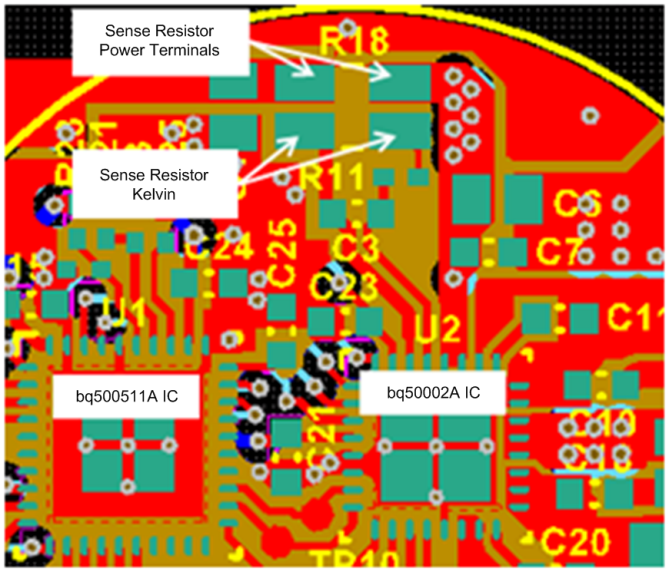


Figure 15. Current Sensing Layout

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

1. 数据表《*bq500511A 无线电源发送器控制器*》（文献编号：SLUSCN3）
2. 评估模块《*bq50002 无线电源 Tx EVM*》（文献编号：SLVUAJ7）

11.2 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.3 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 商标

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11.5 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ50002ARHBR	NRND	VQFN	RHB	32	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Q50002A	
BQ50002ARHBT	NRND	VQFN	RHB	32	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	Q50002A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

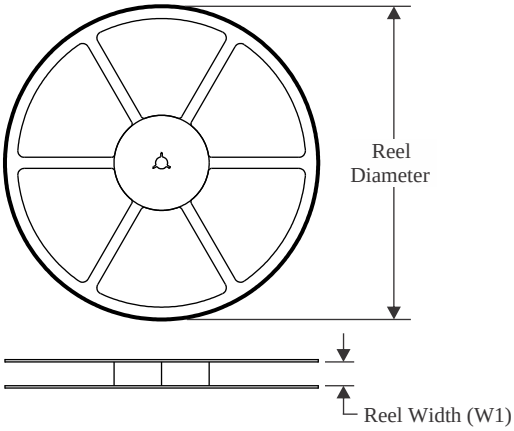
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

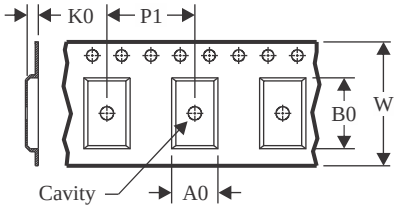
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

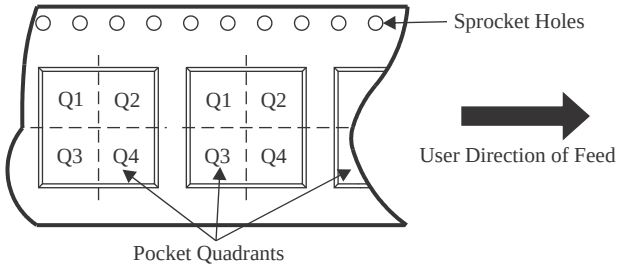


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

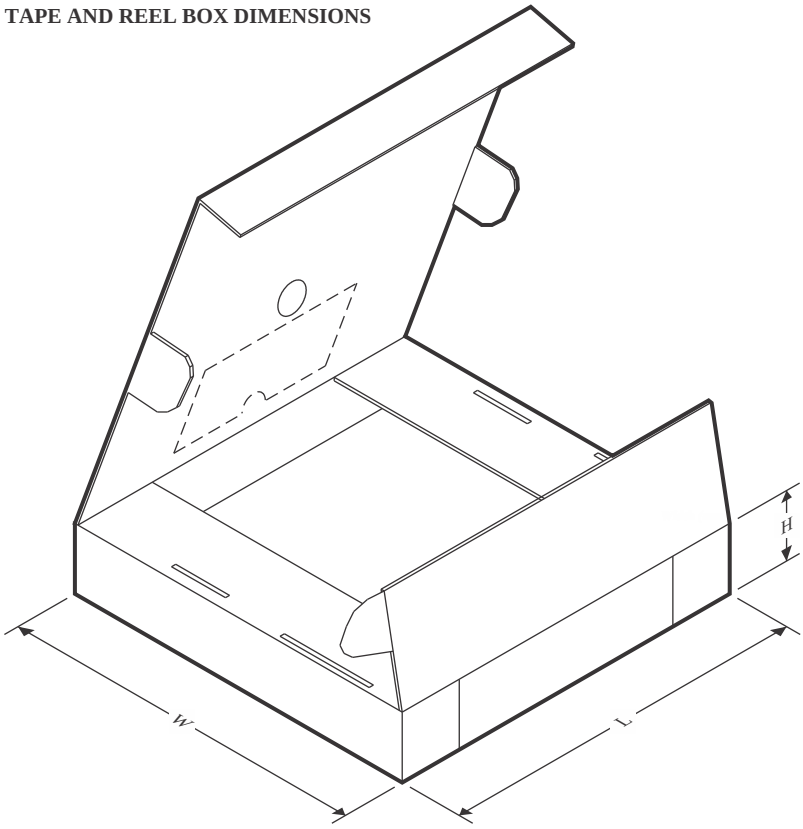
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ50002ARHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
BQ50002ARHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ50002ARHBR	VQFN	RHB	32	3000	346.0	346.0	33.0
BQ50002ARHBT	VQFN	RHB	32	250	182.0	182.0	20.0

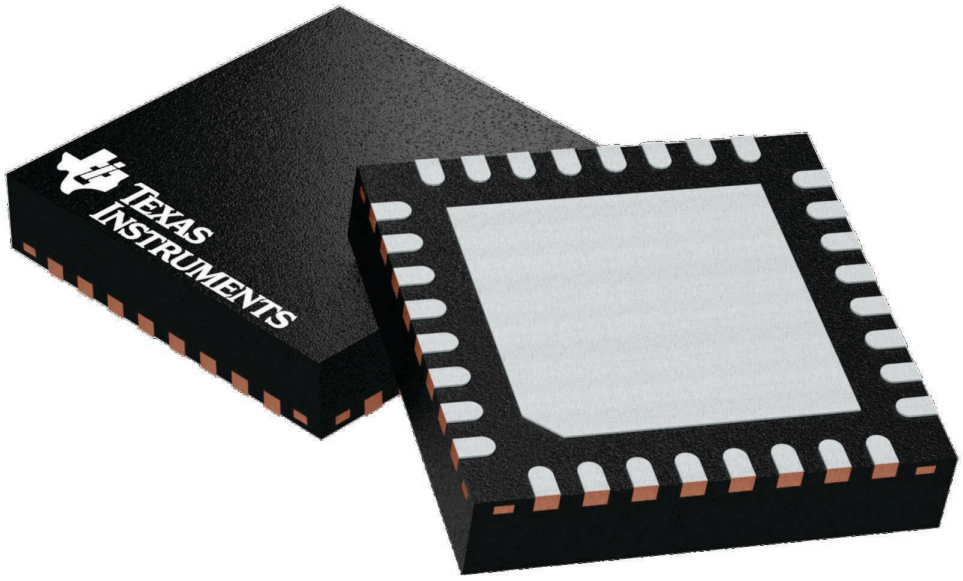
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

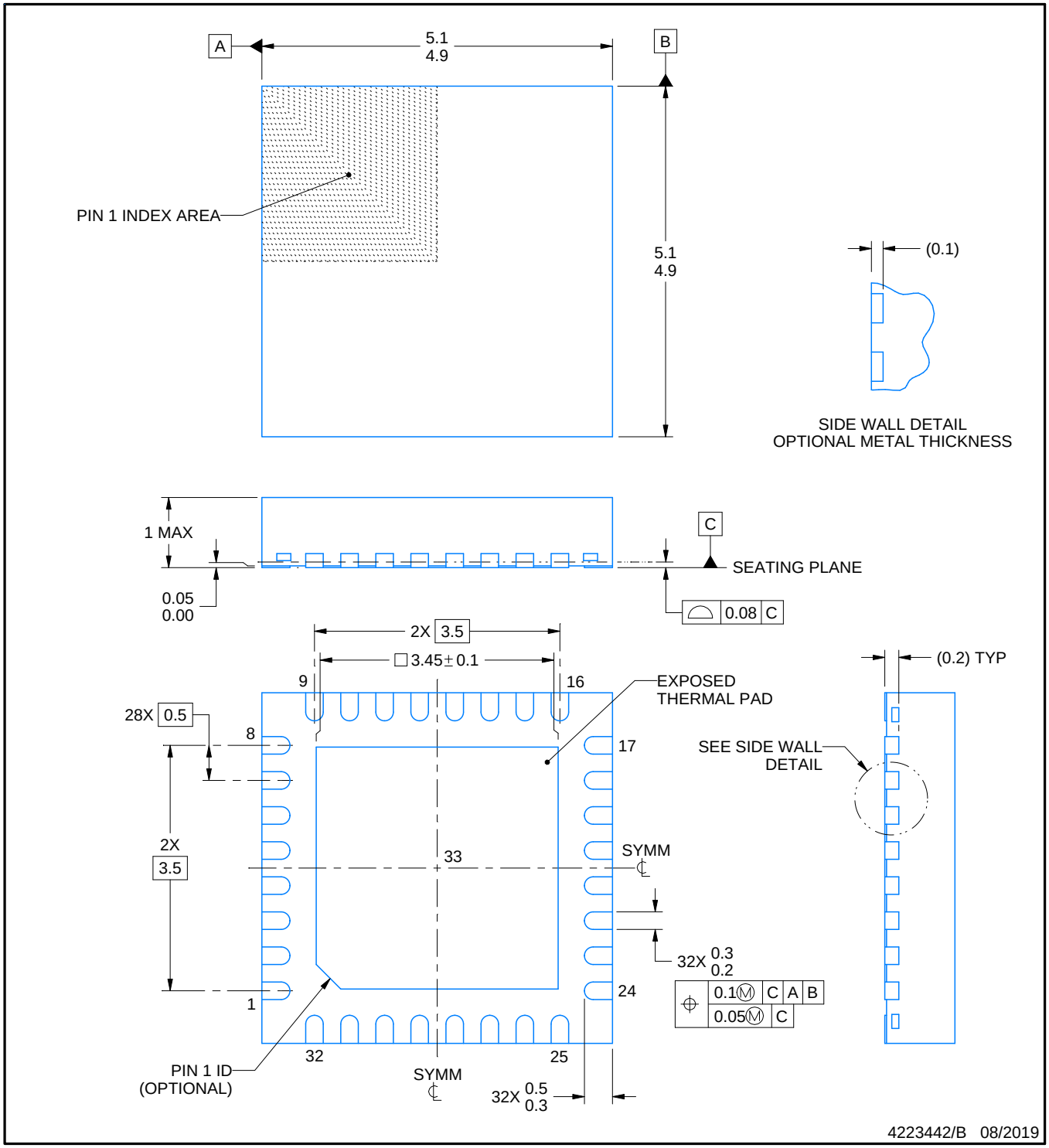
4224745/A

RHB0032E

PACKAGE OUTLINE

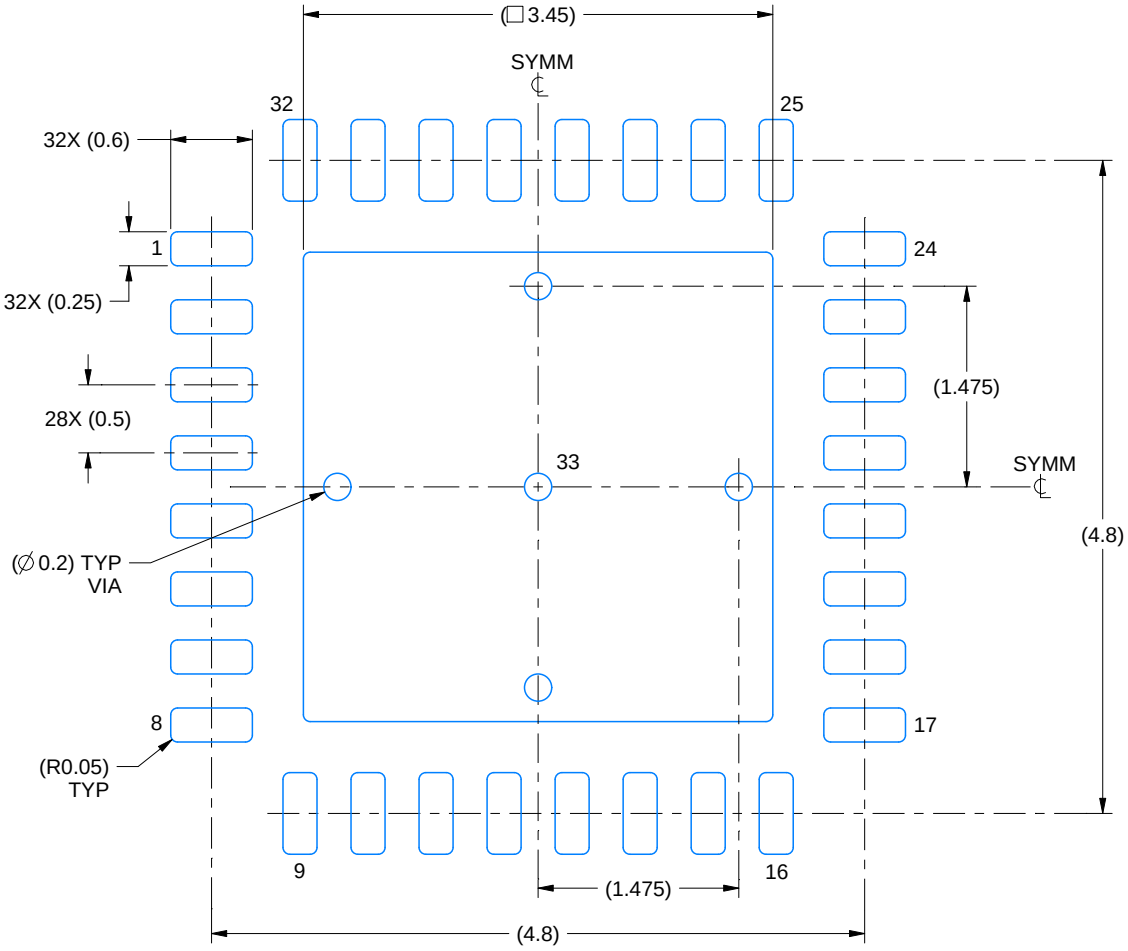
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

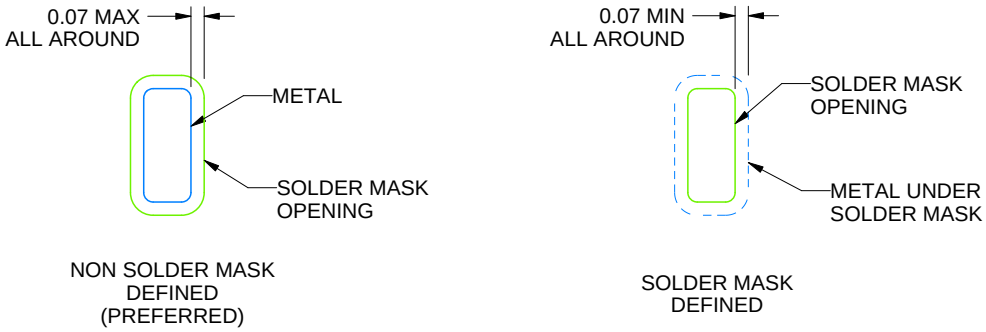


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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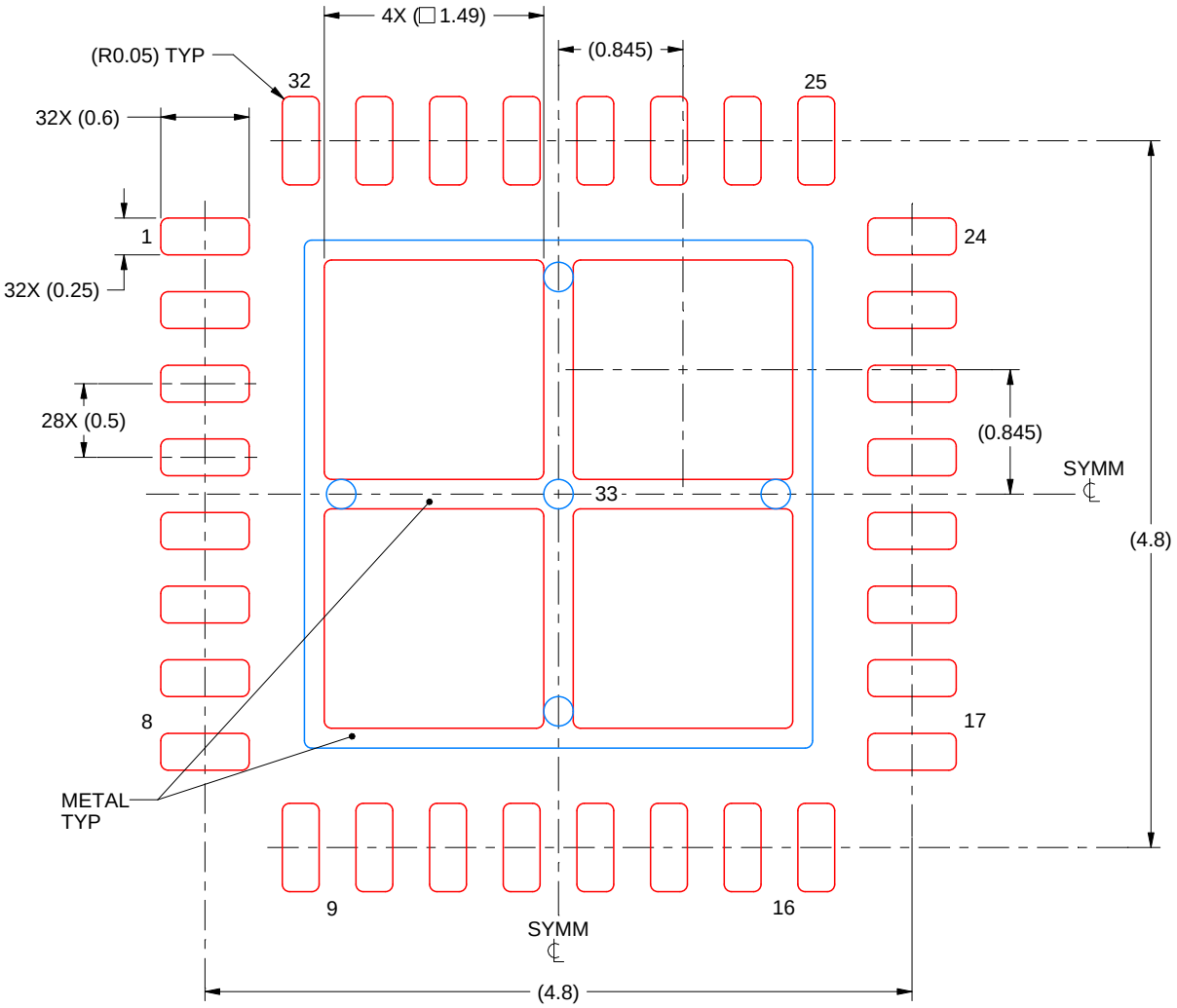
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/B 08/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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