具有内部延迟计时器的 2 节至 5 节串联锂离子电池 BQ7718 过压保护器

1 特性

- 2、3、4 和 5 节串联电池过压保护
- 内部延迟计时器
- 固定的 OVP 阈值
- 高精度过压保护：
  ±10mV
- 低功耗 I_{CC} ≈ 1μA
  ($V_{CELL(ALL)}$ < $V_{PROTECT}$)
- 每节电池输入具有小于 100nA 的低泄漏电流
- 提供功能安全
  - 可帮助进行功能安全系统设计的文档
- 封装尺寸选项：
  - 小型 8 引脚 QFN (3.00mm × 4.00mm) 封装
  - 引线式 8 引脚 MSOP（3.00mm × 5.00mm，含引线）

2 应用

- 锂离子电池组保护，可应用于：
  - 手持园艺工具
  - 手持电动工具
  - 无线真空吸尘器
  - UPS 备用电池
  - 轻型电动车辆（电动自行车、电动踏板车、踏板辅助自行车）

3 说明

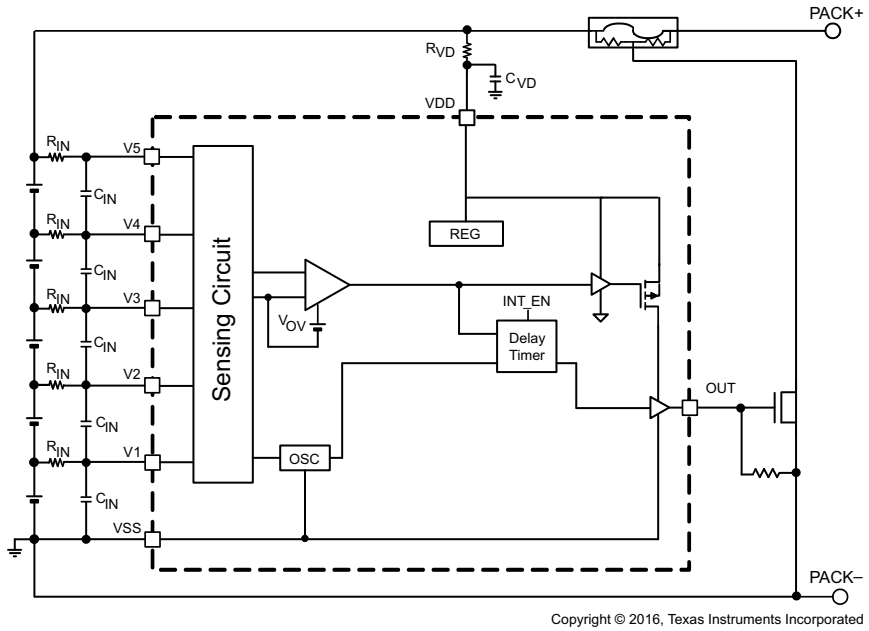
BQ7718xy 系列产品可提供适用于锂离子电池组系统的过压监视器和保护器。独立监控每节电池是否具有过压状态。为了实现更快速的产品线测试，BQ7718xy 器件可提供延迟时间大幅减少的客户测试模式 (CTM)。

在 BQ7718xy 器件中，当检测到任意电池上存在过压状态时，即会启动内部延迟计时器。在延迟计时器超时时，输出被触发进入其工作状态（根据配置的不同为高电平或低电平）。

器件信息表

器件型号	封装	封装尺寸（标称值）
BQ771800(1)	DPJ (8)	3.00mm × 4.00mm
BQ771800(2)	DGK (8)	3.00mm x 3.00mm（3.00mm x 5.00mm，含引线）

(1) 如需了解可用封装，请参阅数据表末尾的可订购产品附录和 节 5。
(2) 如需更多信息，请联系 TI。



简化版原理图

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision K (April 2021) to Revision L (June 2021) — **Page**

- Changed the BQ771825 device to Production Data.....3

Changes from Revision J (September 2020) to Revision K (June 2021) — **Page**

- Added the BQ771825 device to the *Device Comparison Table* 3

Changes from Revision I (July 2020) to Revision J (September 2020) — **Page**

- Added the BQ771824 device to the *Device Comparison Table* 3
- Added BQ771824 to the *DC Characteristics* 6
- Added BQ771824 delay settings.....7

Changes from Revision H (February 2020) to Revision I (July 2020) — **Page**

- 添加了“提供功能安全”特性.....1
- Added the BQ771823 device to the *Device Comparison Table* 3
- Added BQ771823 to the *DC Characteristics* 6
- Added BQ771823 delay settings to *节 7.6* 7

5 Device Comparison Table

T_A	Part Number	Package	Package Designator	OVP (V)	OV Hysteresis (V)	Output Delay	Output Drive	Tape and Reel (Large)	Tape and Reel (Small)
–40°C to 110°C	BQ771800	8-Pin QFN or 8-Pin MSOP	DPJ/DGK	4.300	0.300	4 s	CMOS Active High	BQ771800DPJR	BQ771800DPJT
	BQ771801			4.275	0.050	3 s	NCH Active Low, Open Drain	BQ771801DPJR	BQ771801DPJT
	BQ771802			4.225	0.300	1 s	NCH Active Low, Open Drain	BQ771802DPJR	BQ771802DPJT
	BQ771803			4.275	0.050	1 s	NCH Active Low, Open Drain	BQ771803DPJR	BQ771803DPJT
								BQ771803DGKR(2)	BQ771803DGKT(2)
	BQ771806			4.350	0.300	3 s	CMOS Active High	BQ771806DPJR	BQ771806DPJT
	BQ771807			4.450	0.300	3 s	CMOS Active High	BQ771807DPJR	BQ771807DPJT
	BQ771808			4.200	0.050	1 s	NCH Active Low, Open Drain	BQ771808DPJR	BQ771808DPJT
	BQ771809			4.200	0.050	1 s	CMOS Active High	BQ771809DPJR	BQ771809DPJT
	BQ771811			4.225	0.050	1 s	CMOS Active High	BQ771811DPJR	BQ771811DPJT
	BQ771815			4.225	0.050	1 s	NCH Active Low, Open Drain	BQ771815DPJR	BQ771815DPJT
	BQ771817			4.275	0.050	1 s	CMOS Active High	BQ771817DPJR	BQ771817DPJT
	BQ771818			4.300	0.300	1 s	CMOS Active High	BQ771818DPJR	BQ771818DPJT
								BQ771818DGKR	BQ771818DGKT
	BQ771823			4.275	0.300	3 s	NCH Active Low, Open Drain	BQ771823DPJR	—
	BQ771824			3.850	0.300	4 s	CMOS Active High	BQ771824DPJR	—
	BQ771825			3.950	0.050	3 s	NCH Active Low, Open Drain	BQ771825DPJR	BQ771825DPJT
								BQ771825DGKR(2)	BQ771825DGKT(2)
	BQ7718xy(1)			3.850 – 4.650	Latch, 0.05, 0.25, 0.3	1, 4, 3, 5.5 s	NCH, Active Low, Open Drain, CMOS Active High	BQ7718xyDPJR	BQ7718xyDPJT

(1) Future option. Contact TI for more information.
(2) Contact TI for more information.

6 Pin Configuration and Functions

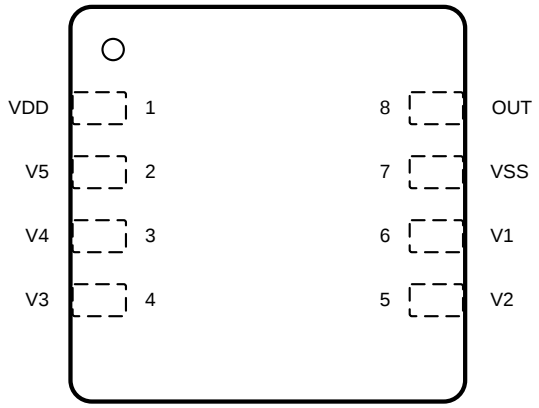


图 6-1. DPJ Package 8-Pin (WSON) Top View

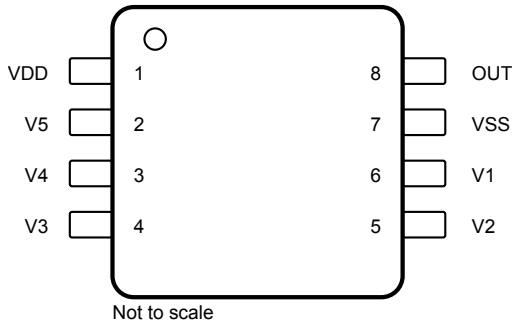


图 6-2. DGK Package 8-Pin (PDSO) Top View

表 6-1. Pin Functions

NO.	NAME	TYPE I/O	DESCRIPTION
1	VDD	P	Power supply
2	V5	I	Sense input for positive voltage of the fifth cell from the bottom of the stack
3	V4	I	Sense input for positive voltage of the fourth cell from the bottom of the stack
4	V3	I	Sense input for positive voltage of the third cell from the bottom of the stack
5	V2	I	Sense input for positive voltage of the second cell from the bottom of the stack
6	V1	I	Sense input for positive voltage of the lowest cell in the stack
7	VSS	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
8	OUT	O	Output drive for overvoltage fault signal
O = Output, I = Input, P = Power connection			

7 Specifications

7.1 Absolute Maximum Ratings

Over-operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	VDD – VSS	–0.3	30	V
Input voltage range	V5 – VSS or V4 – VSS or V3 – VSS or V2 – VSS or V1 – VSS	–0.3	30	V
Output voltage range	OUT – VSS	–0.3	30	V
Continuous total power dissipation, P_{TOT}		See 节 7.4.		
Functional temperature		–40	110	°C
Storage temperature range, T_{STG}		–65	150	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum–rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$ Rating	Electrostatic discharge	Human body model (HBM) ESD stress voltage(1)	±2000	V
		Charged device model (CDM) ESD stress voltage(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over-operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V_{DD} (1)		3	25	V
Input voltage range	V5 – V4 or V4 – V3 or V3 – V2 or V2 – V1 or V1 – VSS	0	5	V
Operating ambient temperature range, T_A		–40	110	°C

(1) See 节 9.2.

7.4 Thermal Information

THERMAL METRIC(1)		BQ7718xy DPJ (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	56.6	°C/W
$R_{\theta JCtop}$	Junction-to-case(top) thermal resistance	56.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	30.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.8	°C/W
$R_{\theta JCbot}$	Junction-to-case(bottom) thermal resistance	11.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 DC Characteristics

Typical values stated where T_A = 25°C and V_{DD} = 18 V, MIN/MAX values stated where T_A = –40°C to 110°C and V_{DD} = 3 V to 25 V (unless otherwise noted).

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Voltage Protection Threshold VCx						
V_{OV}	$V_{(PROTECT)}$ Overvoltage Detection	BQ771800		4.300		V
		BQ771801		4.275		V
		BQ771803		4.275		V
		BQ771802		4.225		V
		BQ771806		4.350		V
		BQ771807		4.450		V
		BQ771808		4.200		V
		BQ771809		4.200		V
		BQ771811		4.225		V
		BQ771815		4.225		V
		BQ771817		4.275		V
		BQ771818		4.300		V
		BQ771823		4.275		V
		BQ771824		3.850		V
V_{HYS}	OV Detection Hysteresis	BQ771800	250	300	400	mV
		BQ771801	0	50	100	mV
		BQ771802	250	300	400	mV
		BQ771803	0	50	100	mV
		BQ771806	250	300	400	mV
		BQ771807	250	300	400	mV
		BQ771808	0	50	100	mV
		BQ771809	0	50	100	mV
		BQ771811	0	50	100	mV
		BQ771815	0	50	100	mV
		BQ771817	0	50	100	mV
		BQ771818	250	300	400	mV
		BQ771823	250	300	400	mV
		BQ771824	250	300	400	mV
V_{OA}	OV Detection Accuracy	T_A = 25°C	–10		10	mV
$V_{OADRIFT}$	OV Detection Accuracy Across Temperature	T_A = –40°C	–40		44	mV
		T_A = 0°C	–20		20	mV
		T_A = 60°C	–24		24	mV
		T_A = 110°C	–54		54	mV
Supply and Leakage Current						
I_{CC}	Supply Current	(V5 – V4) = (V4 – V3) = (V3 – V2) = (V2 – V1) = (V1 – VSS) = 4 V (See 图 8-2.)		1	2	µA
I_{IN}	Input Current at Vx Pins	(V5 – V4) = (V4 – V3) = (V3 – V2) = (V2 – V1) = (V1 – VSS) = 4 V (See 图 8-2.)	–0.1		0.1	µA

Typical values stated where T_A = 25°C and V_{DD} = 18 V, MIN/MAX values stated where T_A = –40°C to 110°C and V_{DD} = 3 V to 25 V (unless otherwise noted).

SYMBOL	PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Output Drive OUT, CMOS Active HIGH Versions Only						
V_{OUT1}	Output Drive Voltage, Active High	(V5 – V4), (V4 – V3), (V3 – V2), (V2 – V1), or (V1 – VSS) > V_{OV}, VDD = 18 V, I_{OH} = 100 µA	6			V
		If three of four cells are short circuited and only one cell remains powered and > V_{OV}, VDD = Vx (cell voltage), I_{OH} = 100 µA		VDD – 0.3		V
		(V5 – V4), (V4 – V3), (V3 – V2), (V2 – V1), and (V1 – VSS) < V_{OV}, VDD = 18 V, I_{OL} = 100 µA measured into pin		250	400	mV
I_{OUTH1}	OUT Source Current (during OV)	(V5 – V4), (V4 – V3), (V3 – V2), (V2 – V1), or (V1 – VSS) > V_{OV}, VDD = 18 V. OUT = 0 V. Measured out of OUT pin			4.5	mA
I_{OUTL1}	OUT Sink Current (no OV)	(V5 – V4), (V4 – V3), (V3 – V2), (V2 – V1), and (V1 – VSS) < V_{OV}, VDD = 18 V, OUT = VDD. Measured into OUT pin	0.5		14	mA
Output Drive OUT, NCH Open Drain Active LOW Versions Only						
V_{OUT2}	Output Drive Voltage, Active Low	(V5 – V4), (V4 – V3), (V3 – V2), (V2 – V1), or (V1 – VSS) > V_{OV}, VDD = 18 V, I_{OL} = 100 µA measured into OUT pin		250	400	mV
I_{OUTH2}	OUT Sink Current (during OV)	(V5 – V4), (V4 – V3), (V3 – V2), (V2 – V1), or (V1 – VSS) > V_{OV}, VDD = 18 V. OUT = VDD. Measured into OUT pin	0.5		14	mA
I_{OUTL2}	OUT Source Current (no OV)	(V5 – V4), (V4 – V3), (V3 – V2), (V2 – V1), and (V1 – VSS) < V_{OV}, VDD = 18 V. OUT = VDD. Measured out of OUT pin			100	nA

7.6 Timing Requirements

			MIN	NOM	MAX	UNIT
Delay Timer						
t_{DELAY}	OV Delay Time	BQ771800, BQ771824	3.2	4	4.8	s
		BQ771801, BQ771807, BQ771823	2.4	3	3.6	s
		BQ771802, BQ771803, BQ771811, BQ771815, BQ771818	0.8	1	1.2	s
		Preview option only. Contact TI.	4.4	5.5	6.6	s
$X_{CTMDELAY}$	Fault Detection Delay Time during Customer Test Mode	See 节 8.4.3.		15		ms

7.7 Typical Characteristics

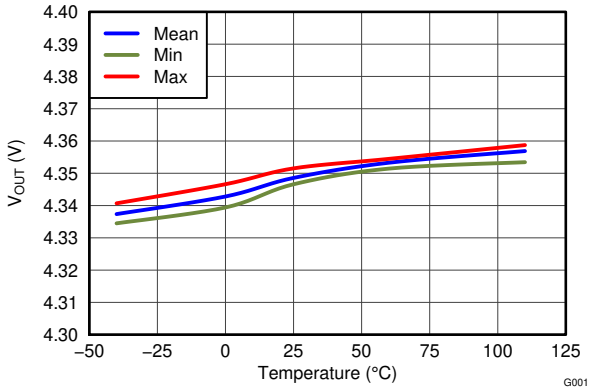


图 7-1. Overvoltage Threshold (OVT) vs. Temperature

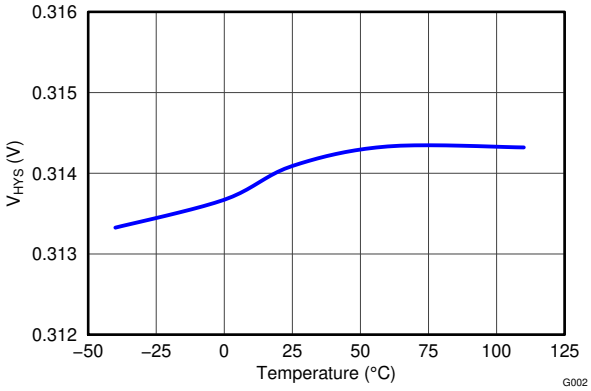


图 7-2. Hysteresis V_{HYS} vs. Temperature

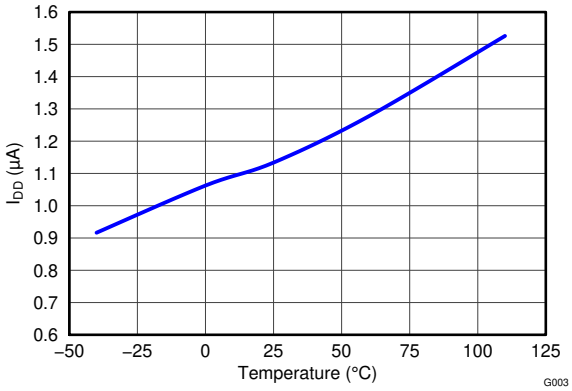


图 7-3. I_{DD} Current Consumption vs. Temperature at VDD = 16 V

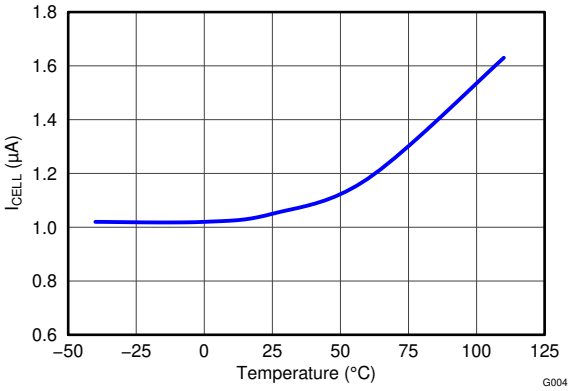


图 7-4. I_{CELL} vs. Temperature at V_{CELL}= 9.2 V

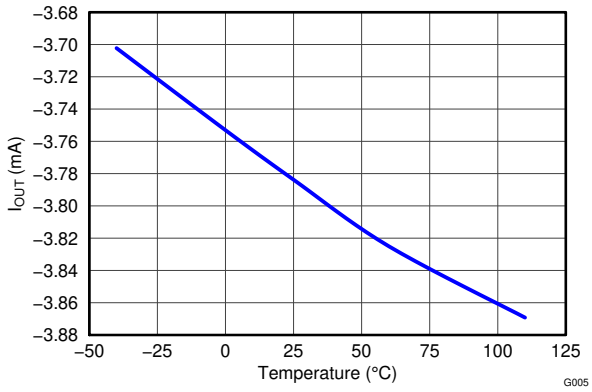


图 7-5. Output Current I_{OUT} vs. Temperature

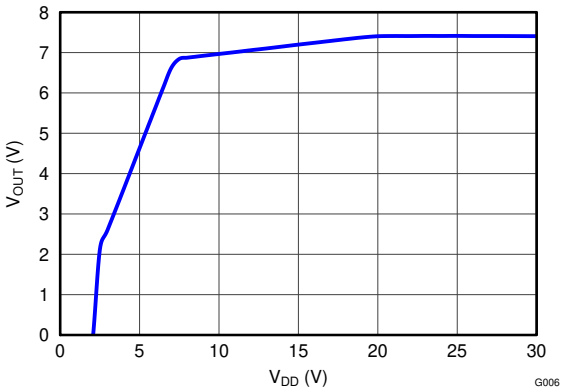


图 7-6. V_{OUT} vs. V_{DD}

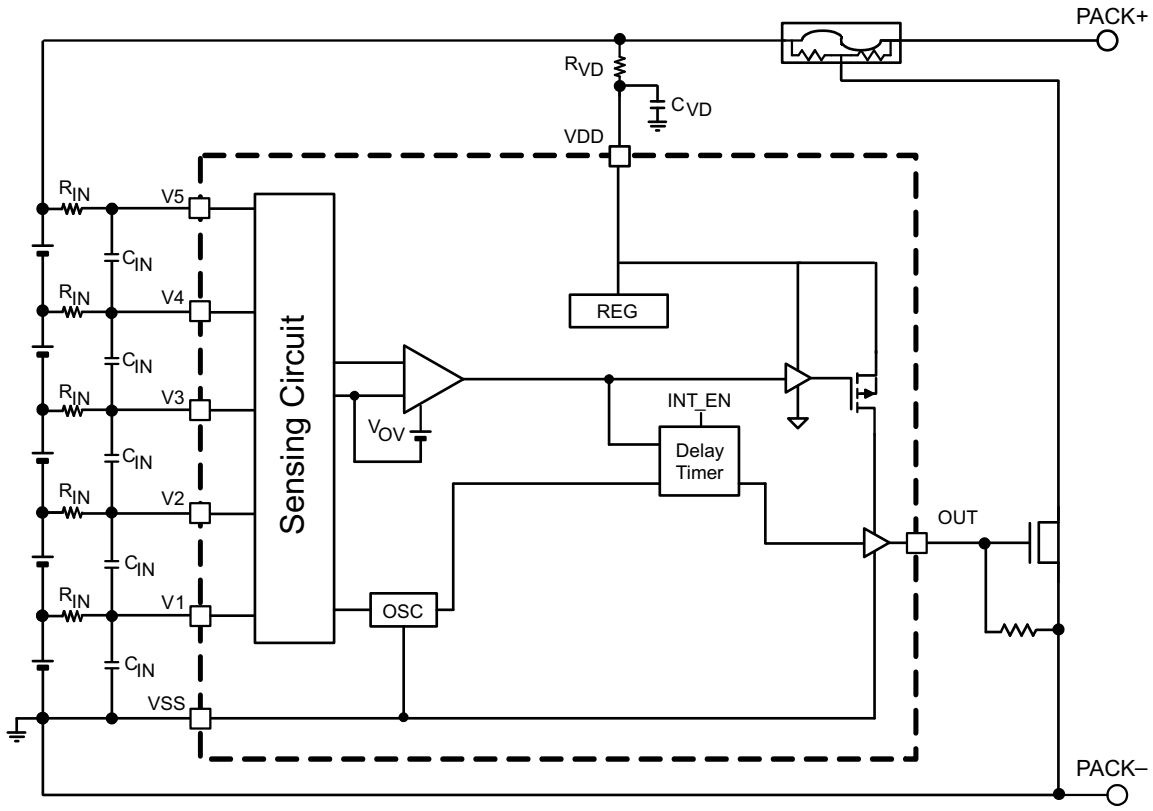
8 Detailed Description

8.1 Overview

In the BQ7718xy family of devices, each cell is monitored independently and an external delay timer is initiated if an overvoltage condition is detected on any cell.

For quicker production-line testing, the device provides a Customer Test Mode with greatly reduced delay time.

8.2 Functional Block Diagram



8.3 Feature Description

In the BQ7718xy device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference, V_{OV}. If any cell voltage exceeds the programmed OV value, a timer circuit is activated. When the timer expires, the OUT pin goes from inactive to active state.

For NCH Open Drain Active Low configurations, the OUT pin pulls down to VSS when active (OV present) and is high impedance when inactive (no OV).

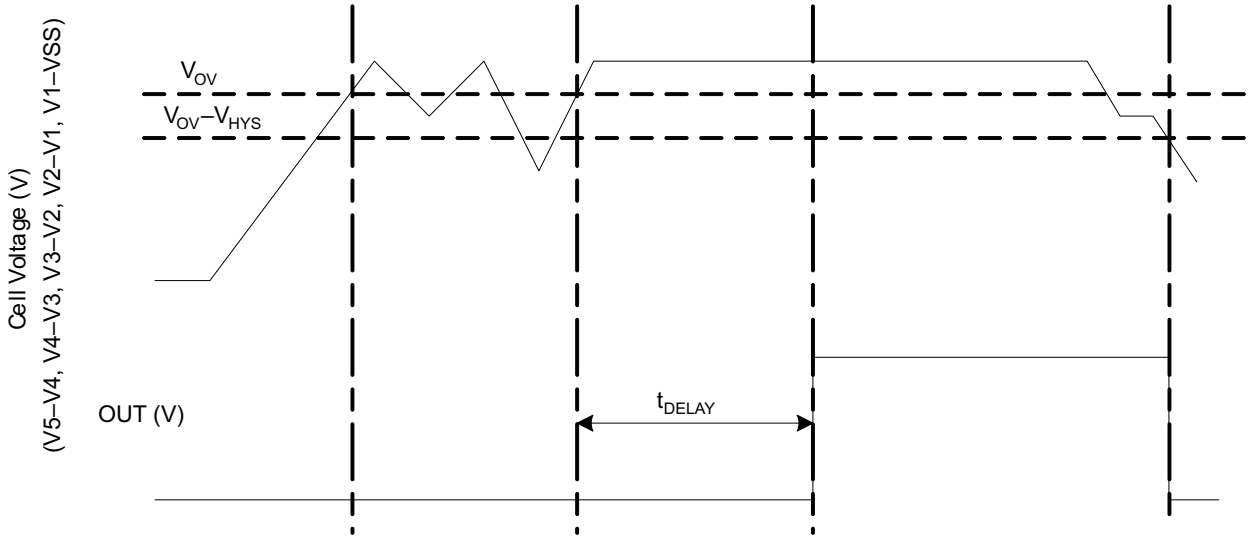


图 8-1. Timing for Overvoltage Sensing

8.3.1 Sense Positive Input for Vx

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

8.3.2 Output Drive, OUT

This pin serves as the fault signal output, and may be ordered in either active HIGH or LOW options.

8.3.3 Supply Input, VDD

This pin is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

8.4 Device Functional Modes

8.4.1 NORMAL Mode

When all of the cell voltages are below the overvoltage threshold, V_{OV}, the device operates in NORMAL mode. The device monitors the differential cell voltages connected across (V1 – VSS), (V2 – V1), (V3 – V2), (V4 – V3), and (VC4 – VC5). The OUT pin is inactive and if configured:

The OUT pin is inactive and if configured:

- Active high is low.
- Active low is being externally pulled up and is an open drain.

8.4.2 OVERVOLTAGE Mode

OVERVOLTAGE mode is detected if any of the cell voltages exceeds the overvoltage threshold, V_{OV} for configured OV delay time. The OUT pin is activated after a delay time set by the capacitance in the CD pin. The OUT pin will either pull high internally, if configured as active high, or will be pulled low internally, if configured as active low. When all of the cell voltages fall below the (V_{OV} – V_{HYS}), the device returns to NORMAL mode.

8.4.3 Customer Test Mode

Customer Test Mode (CTM) helps to reduce test time for checking the overvoltage delay timer parameter once the circuit is implemented in the battery pack. To enter CTM, VDD should be set to at least 10 V higher than V5 (see 图 8-2). The delay timer is greater than 10 ms, but considerably shorter than the timer delay in normal operation. To exit Customer Test Mode, remove the VDD to a V5 voltage differential of 10 V so that the decrease in this value automatically causes an exit.

CAUTION

Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V5 – V4), (V4 – V3), (V4 – V3), (V3 – V2), (V2 – V1), and (V1 – VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

图 8-2 shows the timing for the Customer Test Mode.

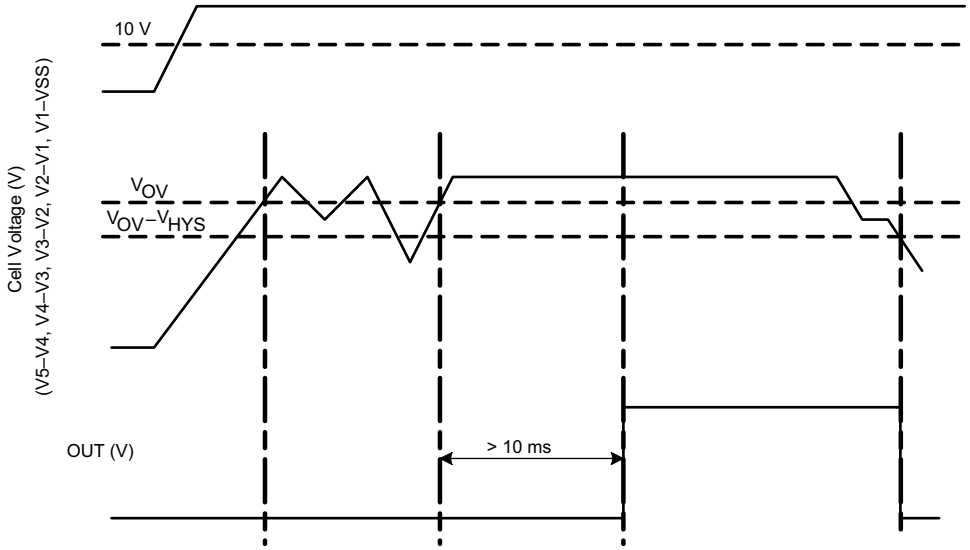


图 8-2. Timing for Customer Test Mode

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In the case of an Open Drain Active Low configuration, an external pull-up resistor is required on the OUT pin. Changes to the ranges stated in 表 9-1 will impact the accuracy of the cell measurements.

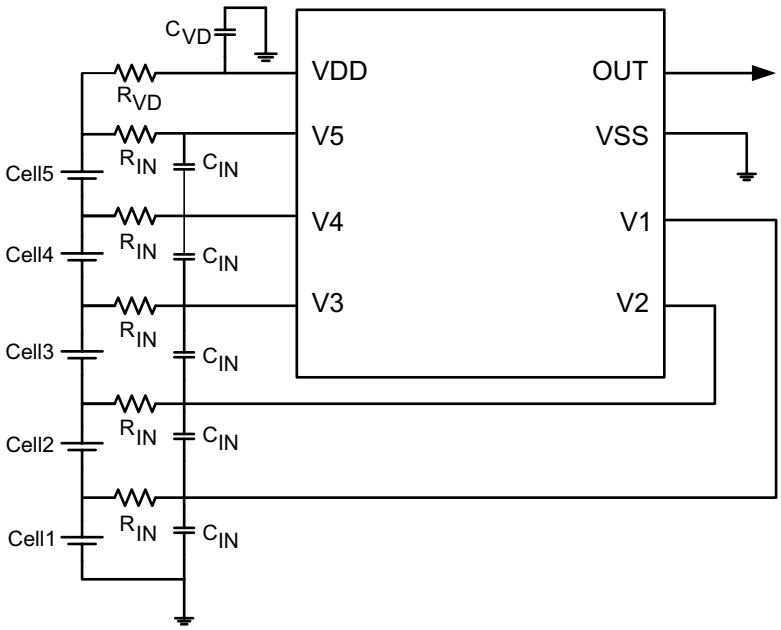


图 9-1. Application Configuration

9.1.1 Design Requirements

Changes to the ranges stated in 表 9-1 will impact the accuracy of the cell measurements. 图 9-1 shows each external component.

表 9-1. Parameters

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	R_{IN}	900	1000	1100	Ω
Voltage monitor filter capacitance	C_{IN}	0.01		0.1	µF
Supply voltage filter resistance	R_{VD}	100		1K	Ω
Supply voltage filter capacitance	C_{VD}		0.1		µF
CD external delay capacitance			0.1	1	µF
OUT Open drain version pull-up resistance to PACK+			100		kΩ

Note

The device is calibrated using an R_{IN} value = 1 kΩ. Using a value other than this recommended value changes the accuracy of the cell voltage measurements and V_{OV} trigger level.

9.1.2 Detailed Design Procedure

图 9-2 shows the measurement for current consumption for the product for both VDD and Vx.

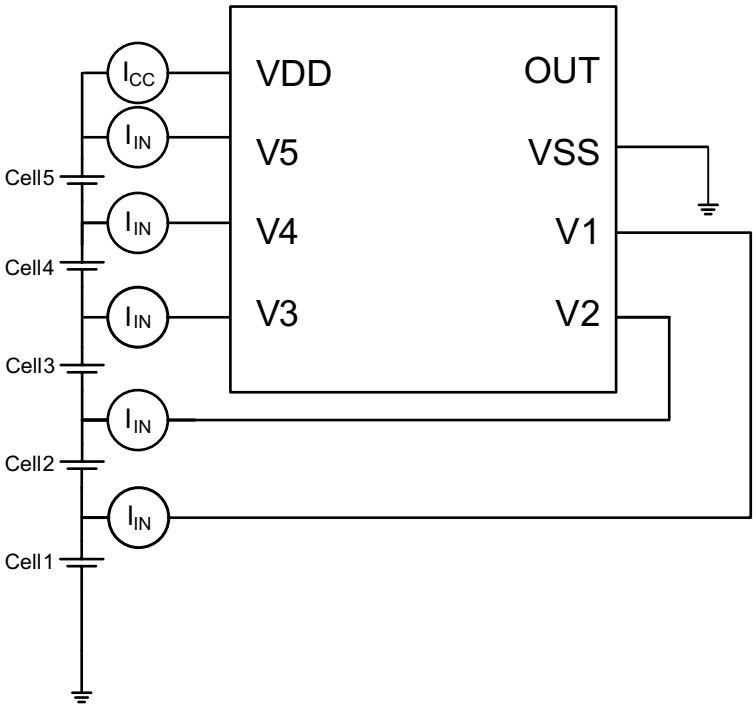


图 9-2. Configuration for IC Current Consumption Test

9.1.2.1 Application Curves

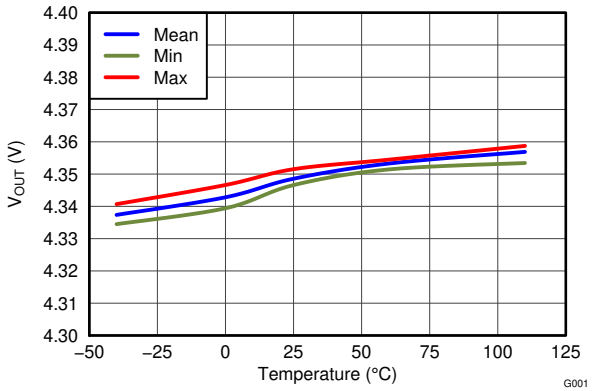


图 9-3. Overvoltage Threshold (OVT) vs. Temperature

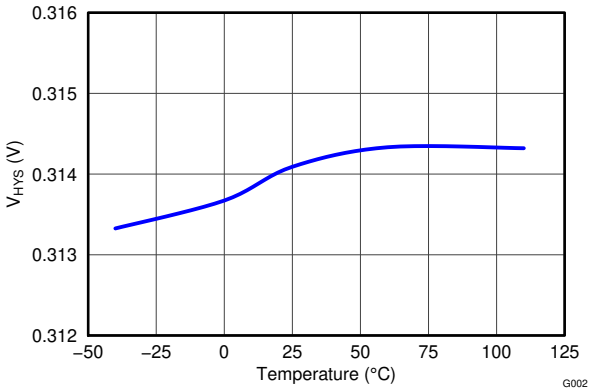


图 9-4. Hysteresis V_{HYS} vs. Temperature

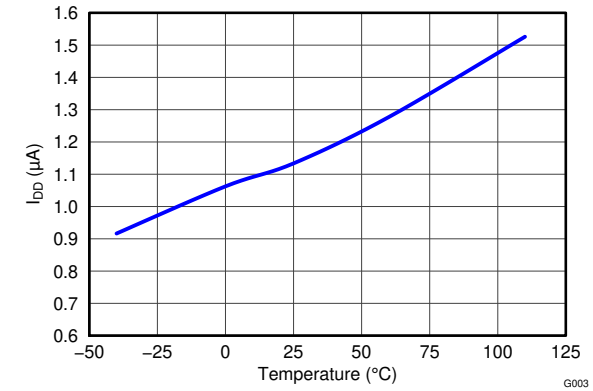


图 9-5. I_{DD} Current Consumption vs. Temperature at VDD = 16 V

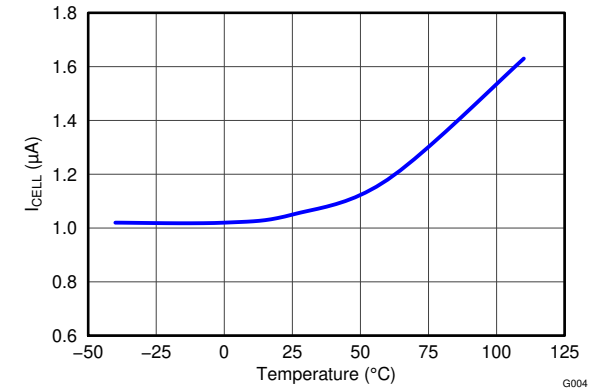


图 9-6. I_{CELL} vs. Temperature at V_{CELL}= 9.2 V

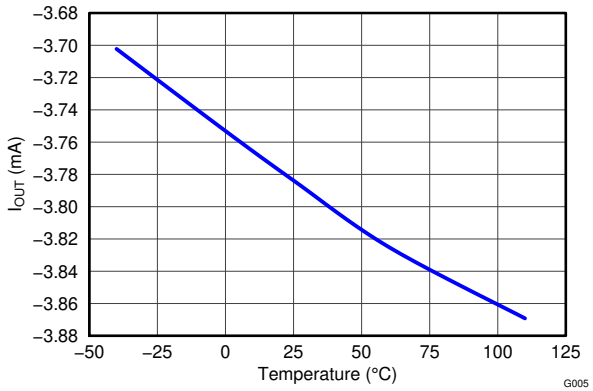


图 9-7. Output Current I_{OUT} vs. Temperature

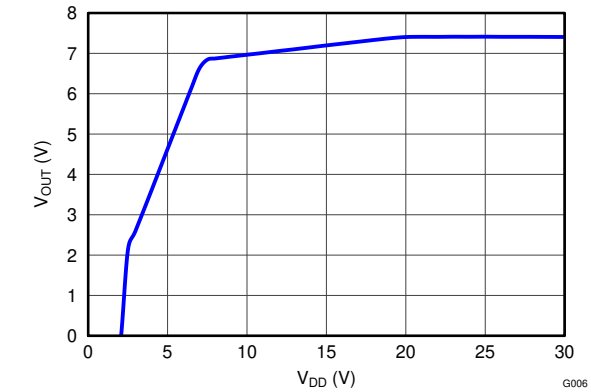


图 9-8. V_{OUT} vs. V_{DD}

9.2 Systems Examples

In these application examples, an external pull-up resistor is required on the OUT pin to configure for an Open Drain Active Low operation.

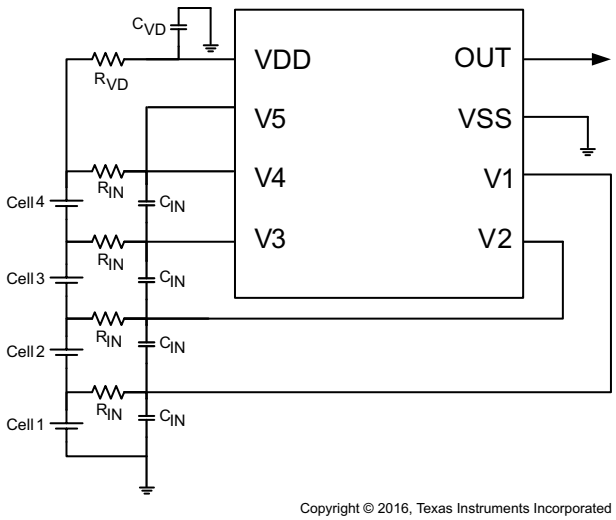


图 9-9. 4-Series Cell Configuration

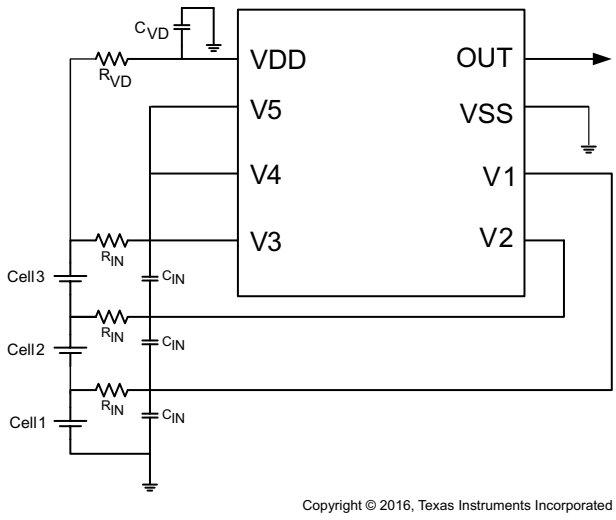


图 9-10. 3-Series Cell Configuration with Fixed Delay

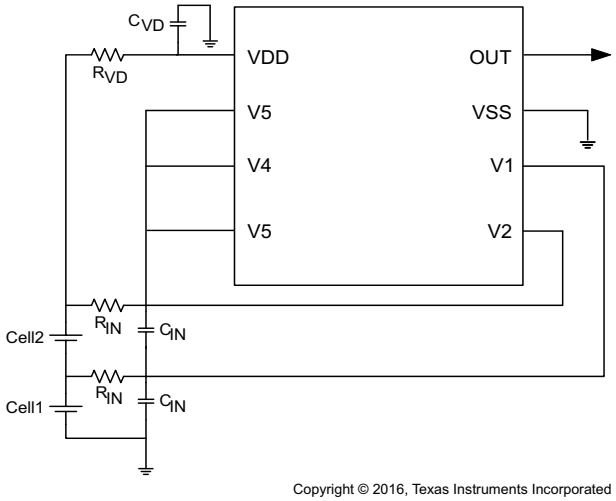


图 9-11. 2-Series Cell Configuration with Internal Fixed Delay

10 Power Supply Recommendations

The maximum power of this device is 25 V on VDD.

11 Layout

11.1 Layout Guidelines

- Ensure the RC filters for the V1 and VDD pins are placed as close as possible to the target terminal.
- The VSS pin should be routed to the CELL – terminal.

11.2 Layout Example

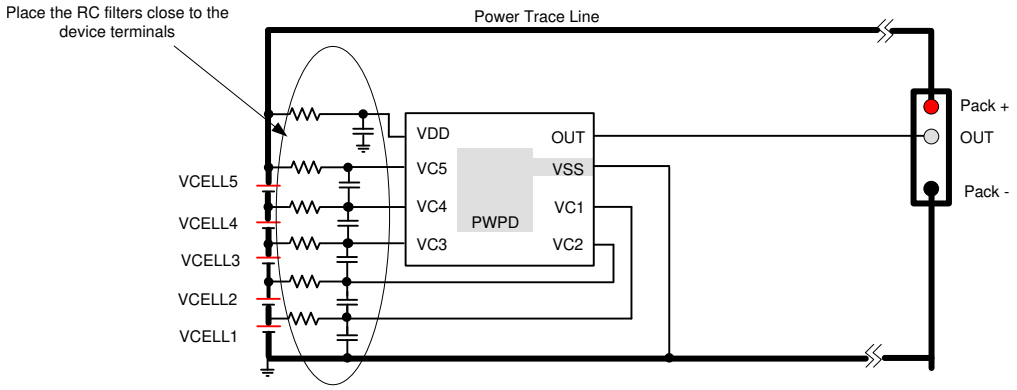


图 11-1. Example Layout

12 Device and Documentation Support

12.1 Documentation Support

For additional information, see the BQ7718 technical documentation, including the documentation available to aid functional safety system design.

12.2 第三方产品免责声明

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要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.5 Trademarks

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12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ771800DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771800	Samples
BQ771800DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771800	Samples
BQ771801DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771801	Samples
BQ771801DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771801	Samples
BQ771802DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771802	Samples
BQ771802DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771802	Samples
BQ771803DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771803	Samples
BQ771803DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771803	Samples
BQ771806DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771806	Samples
BQ771806DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771806	Samples
BQ771807DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771807	Samples
BQ771807DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771807	Samples
BQ771808DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771808	Samples
BQ771808DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771808	Samples
BQ771809DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771809	Samples
BQ771809DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771809	Samples
BQ771811DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771811	Samples
BQ771811DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771811	Samples
BQ771815DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771815	Samples
BQ771815DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771815	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ771817DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771817	Samples
BQ771817DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771817	Samples
BQ771818DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771818	Samples
BQ771818DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771818	Samples
BQ771823DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	771823	Samples
BQ771824DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 110	771824	Samples
BQ771825DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771825	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

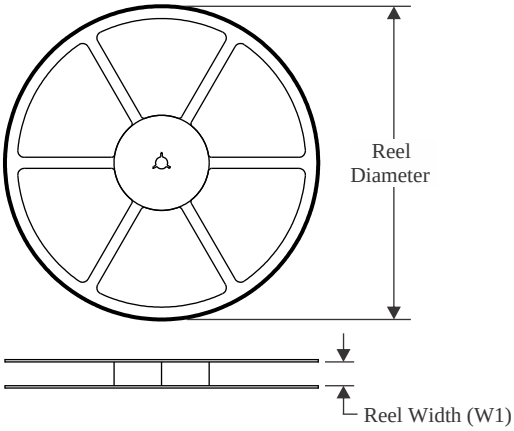
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

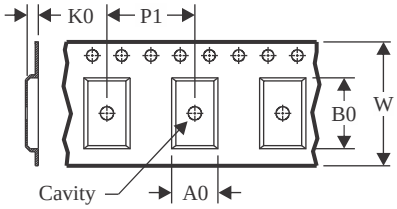
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

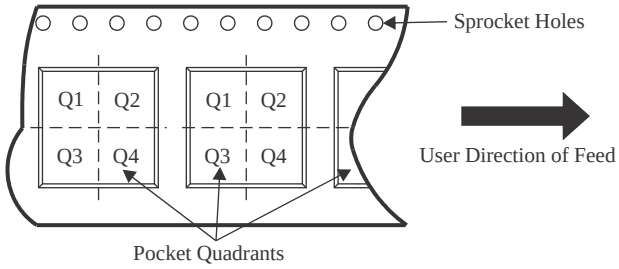


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

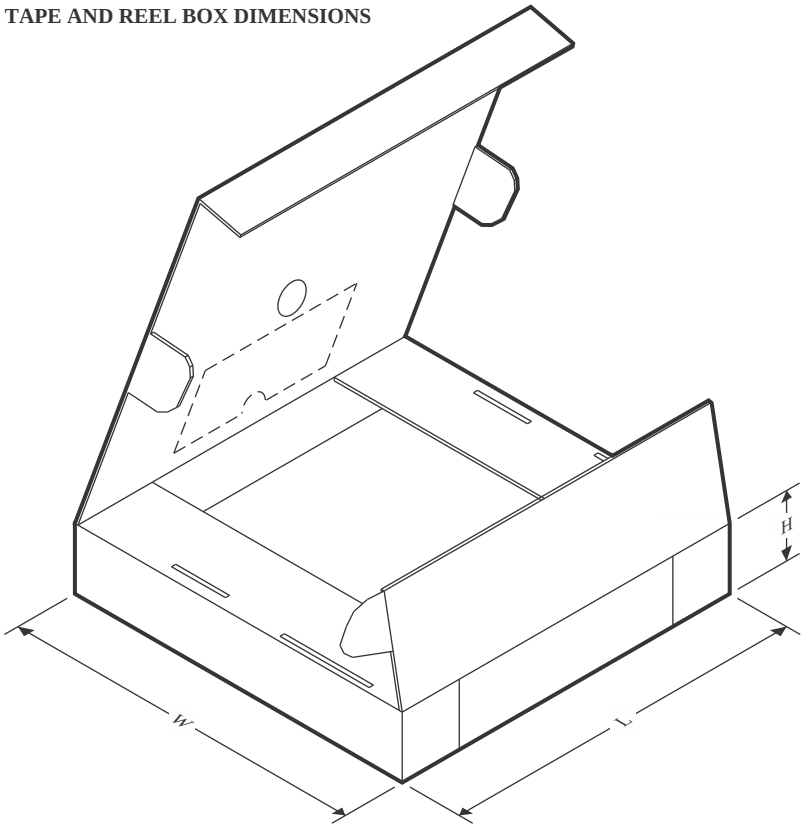


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ771800DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771800DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771801DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771801DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771802DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771802DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771803DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771803DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771806DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771806DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771807DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771807DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771808DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771808DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771809DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771809DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ771811DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771811DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771815DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771815DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771817DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771817DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771818DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771818DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771823DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771824DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771825DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



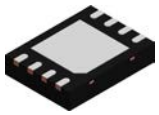
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ771800DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771800DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771801DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771801DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771802DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771802DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771803DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771803DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771806DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771806DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771807DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771807DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771808DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771808DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771809DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771809DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771811DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771811DPJT	WSON	DPJ	8	250	182.0	182.0	20.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ771815DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771815DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771817DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771817DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771818DPJR	WSON	DPJ	8	3000	346.0	346.0	33.0
BQ771818DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771823DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771824DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771825DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0

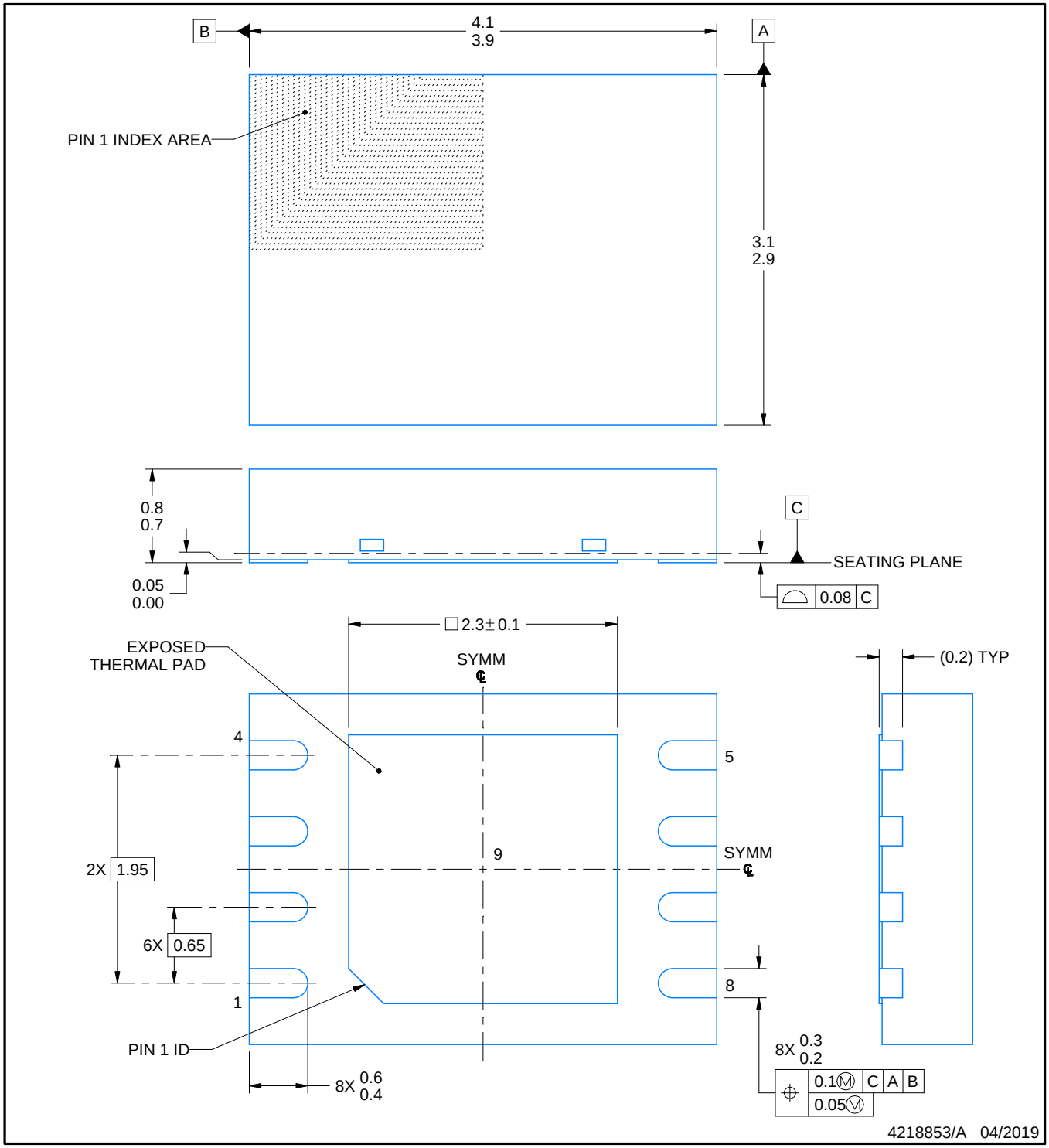
PACKAGE OUTLINE

DPJ0008A



WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

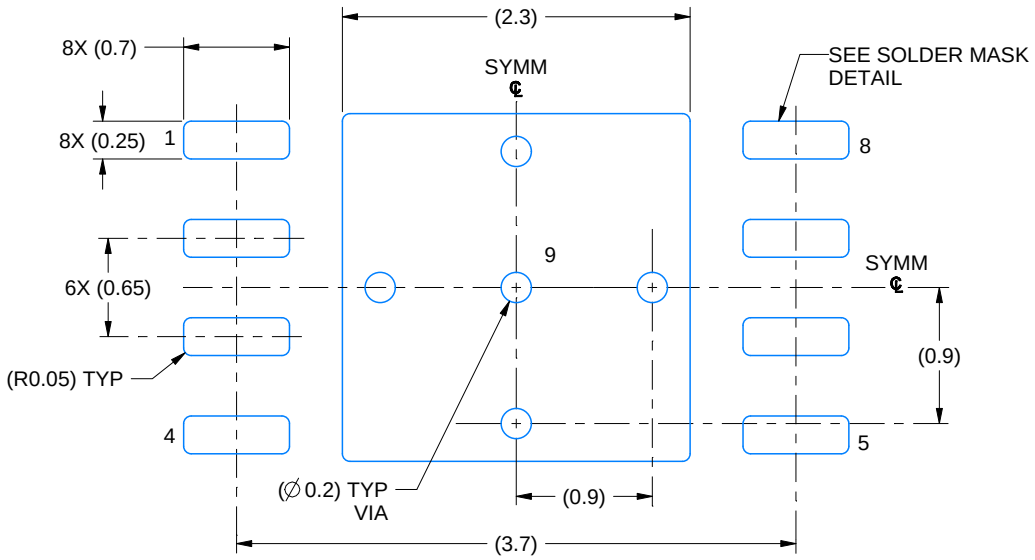
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

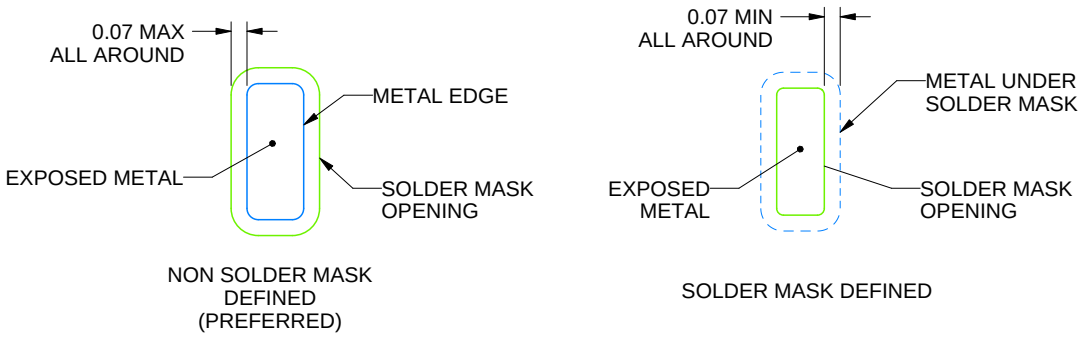
DPJ0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



SOLDER MASK DETAILS

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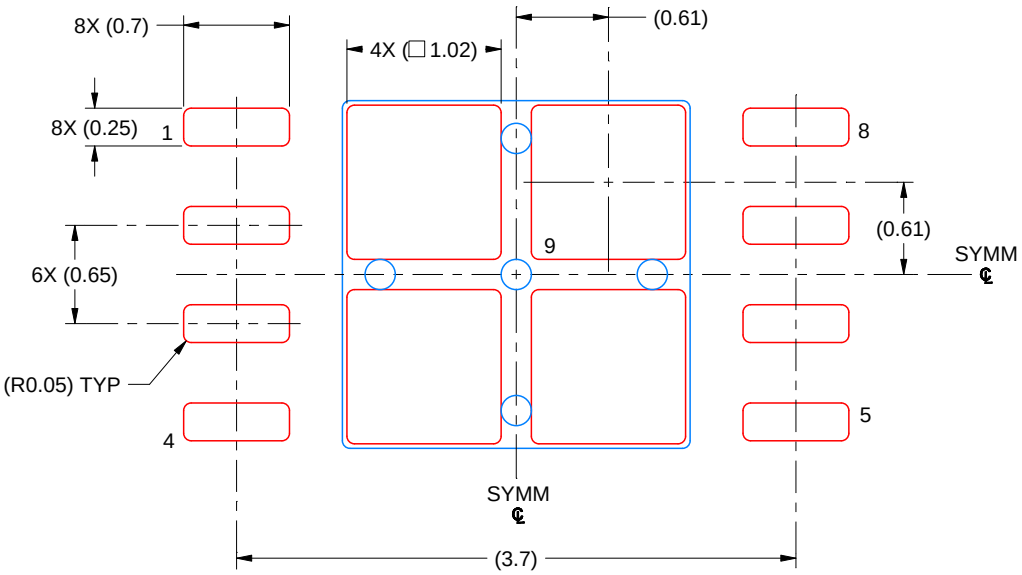
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 9
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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